

# *Conceptual Design of a $\Delta\Sigma$ -ADC*

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# Outline

- Introducing/ Proposing the Required System
  - Characterize  $\Delta\Sigma$ -Modulators
  - Behavioural Overview
- Deriving a Circuit Realization
- Proposals for IC Design
  - Deriving the Technology-Based Requirements
  - Overview of Proposed Circuitries

# Use-Case of Analog-Digital Converter

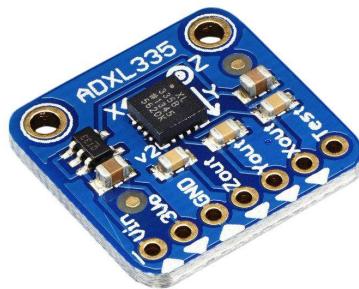


Fig.1: Accelerometer, ADXL335 [3]

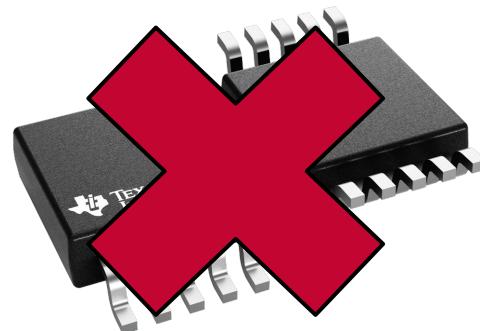


Fig.2: ADC, ADS1115 [2]

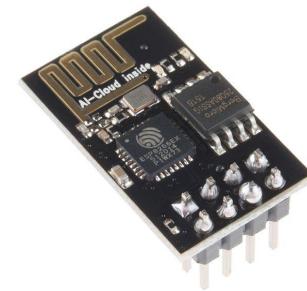


Fig.3: μC, ESP8266 [1]

# ADS1115

The **ADS1115** is a high-precision **16-bit Analog-to-Digital Converter (ADC)** produced by Texas Instruments. It's widely used to interface analog signals with digital systems, such as microcontrollers or communication modules. Some notable features include:

- **Resolution:** It provides 16-bit resolution, offering precise conversion of analog signals into digital form.
- **Input Channels:** The ADS1115 includes 4 channels, which can be configured for single-ended or differential input modes.
- **Data Rate:** It offers a configurable data rate of up to 860 samples per second (SPS), making it suitable for slow to medium-speed analog signals.
- **Low Power Consumption:** It's designed to be energy-efficient, which is ideal for battery-powered devices.
- **I<sup>2</sup>C Communication:** The ADS1115 communicates over the I<sup>2</sup>C bus, which is a simple and commonly used interface for connecting devices.
- **Programmable Gain Amplifier (PGA):** This feature allows you to amplify the input signal, which is useful for measuring weak signals with higher precision.

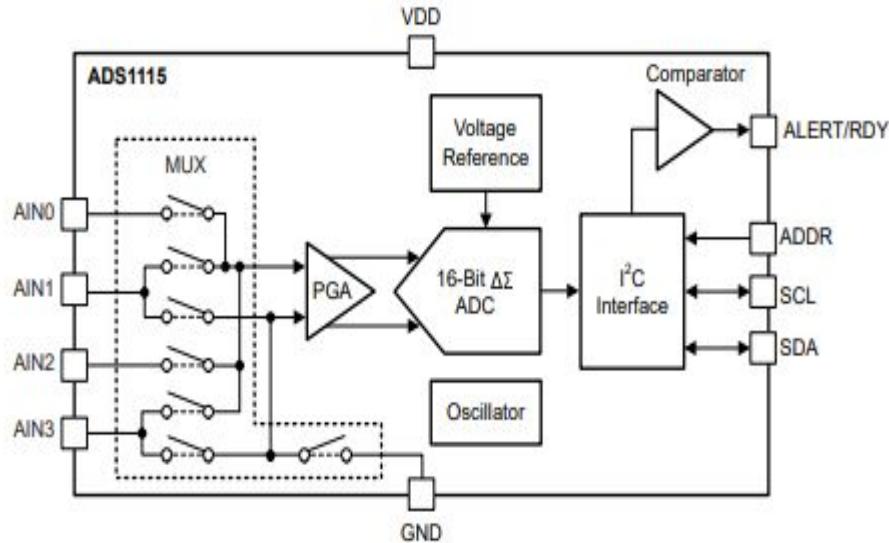


Fig:4 ADS1115 Block diagram

Parameter	Value
Voltage Supply ( $V_{DD}$ )	2V0 ~ 5V5
Abs.Max $V_{DD}$	-0.3V ~ 7V0
Measurement range	-300mV ~ Vdd+300mV
Interface	<u>I2C</u>
I2C rate	100kHz, 400kHz, 3.4MHz
Resolution	16 bits ( $\pm 15$ bits)
Data rate	8 ~ 860 SPS
Number of multiplexed inputs	4
Active current	$\sim 150\mu A$ (200 $\mu A$ max)
Power down current	0.5 $\mu A$ (2 $\mu A$ max)
Offset error [1]	$\pm 3$ LSB
Integral Non-Linearity (INL) [1]	1 LSB
Gain error [1],[2], @ 25°C	0.01% (typ) 0.15% (max)
I2C Addresses (selectable)	0x48, 0x49, 0x4a, 0x4b
Operating temperature	-40°C ~ 125°C

Table 1: ADS1115 Specifications

# ADXL335 Accelerometer

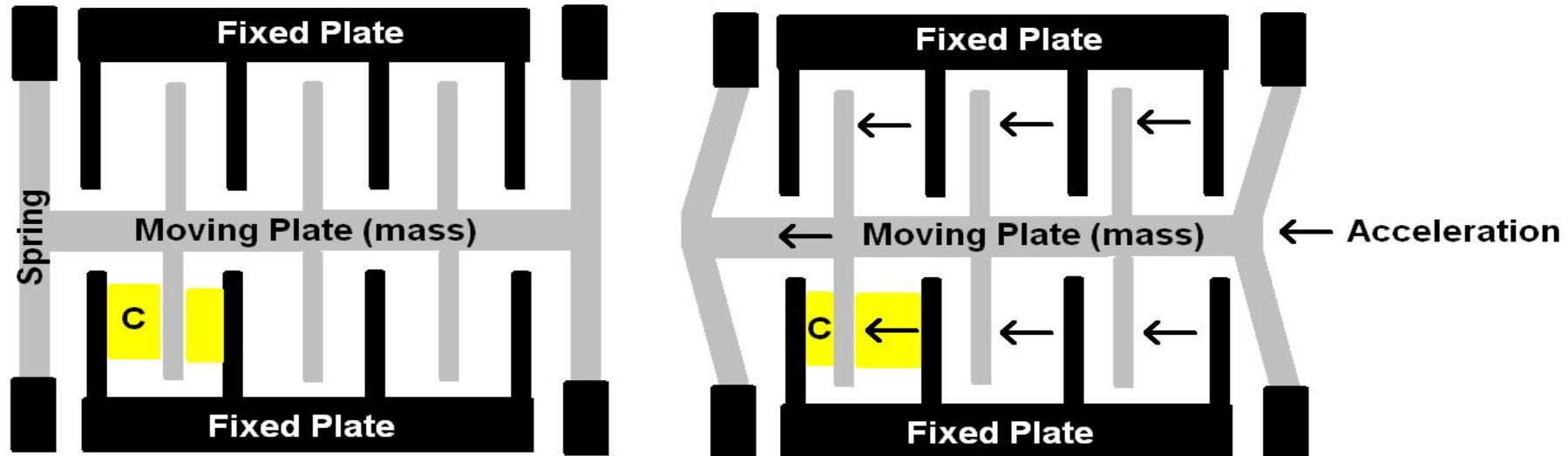
The **ADXL335** is a small, low-power, 3-axis accelerometer from Analog Devices, designed to measure acceleration along the **X**, **Y**, and **Z** axes. It's ideal for applications that require motion detection, tilt measurement, or vibration analysis.

## Key Specifications:

- **Acceleration Range:**  $\pm 3g$ , capable of measuring acceleration up to 3 times the force of gravity.
- **Output:** Provides analog signals for each of the three axes (X, Y, Z).
- **Supply Voltage:** Operates within a range of 1.8V to 3.6V.
- **Sensitivity:** 300mV per g of acceleration (a change of 1g results in a 300mV shift in output).
- **Low Power:** Consumes just about 350  $\mu A$  under typical conditions.
- **Compact Size:** Small form factor, suitable for embedded systems and space-constrained applications.

# Specification of ADXL335

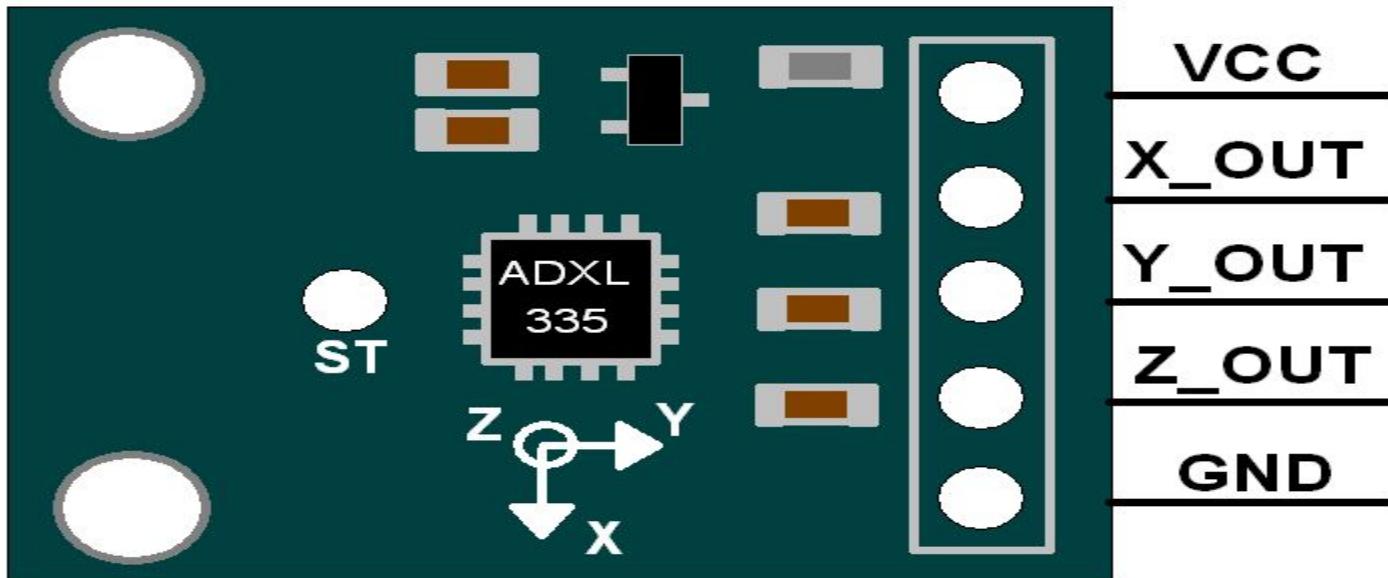
1. Supply Voltage: 2.8V to 3.6V
2. Current Consumption: 320uA
3. Sensitivity: 300mV/g
4. Bandwidth: 3Hz to 5kHz
5. Dynamic Range:  $\pm 3g$
6. Operating Temperature: -40°C to +85°C
7. Package Type: Surface Mount Plastic Package (LFCSP)
8. Pin Configuration: 5 Pin, 1.27mm Pitch
9. Output Type: Voltage Output
10. Interface: SPI/I2C
11. Output Range: 0V to Vcc
12. Storage Temperature: -65°C to +150°C



**Accelerometer Sensor MEM Mechanism**

ElectronicWings.com

Fig.5: Accelerometer Mechanism



ElectronicWings.com

Fig.6: ADXL Block diagram

# System-/ Behavioural Overview

# Oversampling ADCs

- Sampling with:  $f_s = OSR \cdot 2 \cdot f_B$ 
  - OSR := “*Oversampling Ratio*”
- Introduces ***Noise Shaping***:
  - Noise Transfer Function (*NTF*) as highpass
  - Shift given quantization noise out of signal band
    - Increasing SQNR ( $\sim$  OSR)

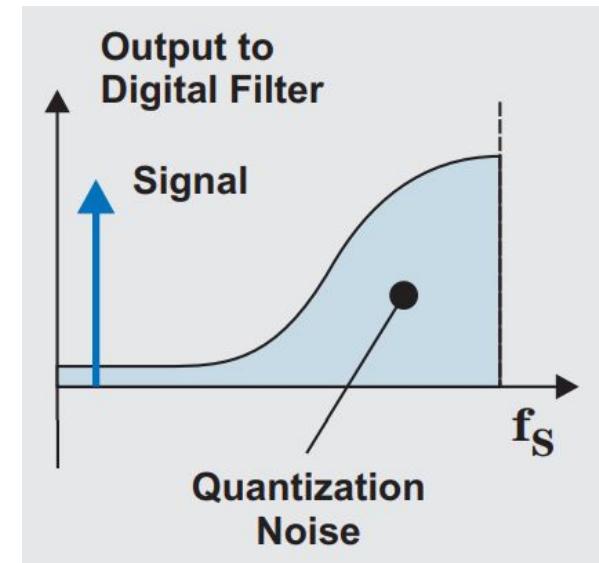


Fig. 7: Visualization of Noise Shaping [4]

# 1st- vs. 2nd Order Modulator

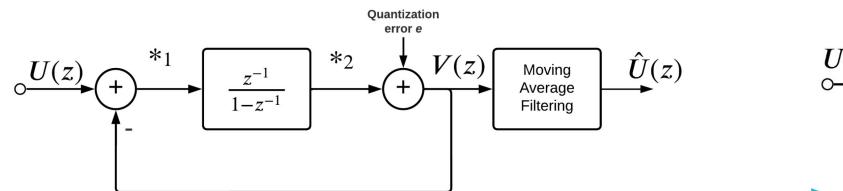


Fig. 8: Behavioural Model of MOD1

Insert MOD1 as  
Quantizer

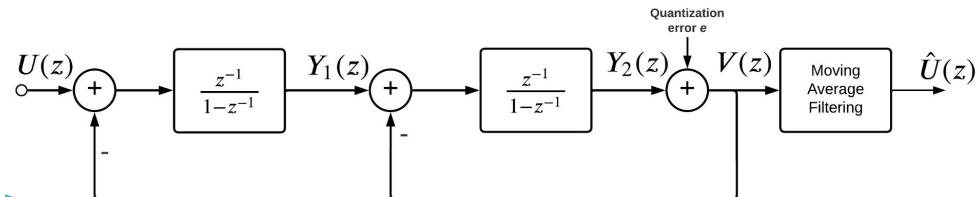


Fig. 9: Behavioural Model of MOD2

$$\begin{aligned} V(z) &= X(z) z^{-1} + E(z) (1 - z^{-1}) \\ &= X(z) STF_1(z) + E(z) NTF_1(z) \end{aligned}$$

$$\begin{aligned} V(z) &= X(z) z^{-1} + E(z) (1 - z^{-1})^2 \\ &= X(z) z^{-1} + E(z) - 2 \cdot E(z) z^{-1} + E(z) z^{-2} \\ &= X(z) STF_2(z) + E(z) NTF_2(z) \end{aligned}$$

# 1st- vs. 2nd Order Modulator

Table 2: Select few impacts of changing from L=1 to L=2

Aspect	Impact by changing from MOD1 to MOD2
Noise Shaping	40dB/decade (previous: 20dB/decade)
SQNR/OSR trade-off	Doubling OSR: <i>Noise Reduction:</i> From 9 dB To 15 dB <i>ENOB Improvement:</i> From $\approx 1.5$ bits to $\approx 2.5$ bits
Stability	Reduced stability insurance (BIBO requirement)
Complexity	Increase in circuit elements (+ stability concerns)

# Insights from MATLAB/ Validations

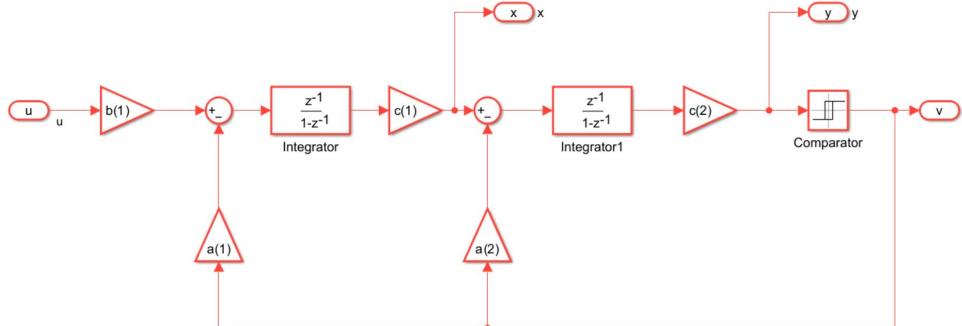


Fig. 10: Utilized MATLAB model for 2nd order analysis

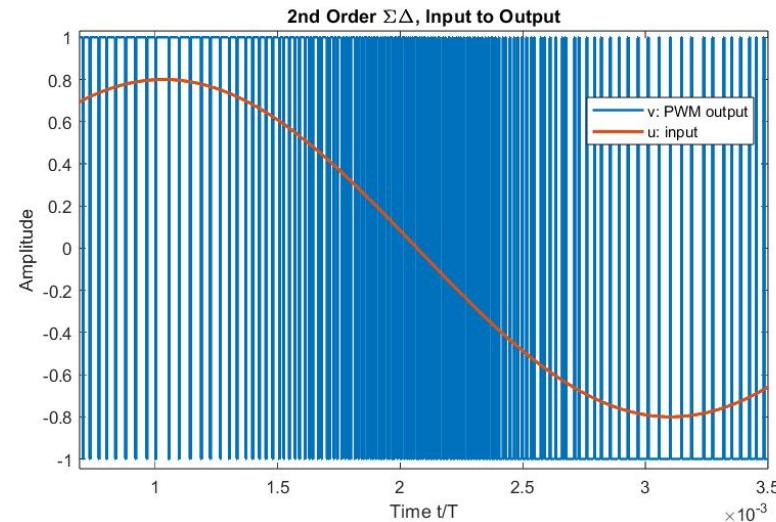


Fig. 11: I/O behaviour in time domain from MATLAB model

# Insights from MATLAB/ Validations

## Comparing PSDs of NTFs (normalized range)

- Expected NTF slopes visible
  - Attenuation for  $f/f_s \rightarrow 0$
  - Amplification for  $f/f_s \rightarrow 1$
  - Increased effect for higher order

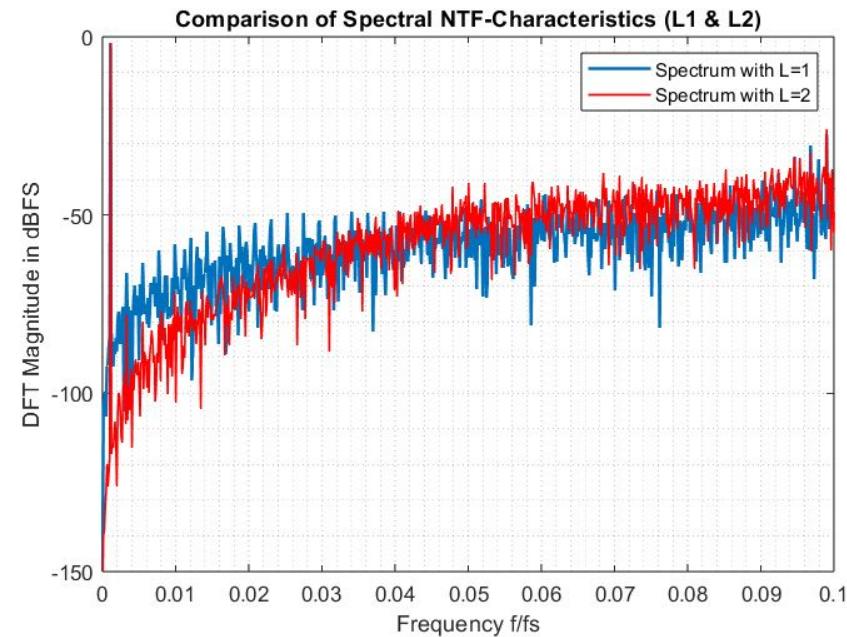


Fig. 12: Comparison of spectral outputs of MATLAB models

# Digital Filter

# Digital Filter

- Goal: high data rate -> low data rate
  - Optional goal: Keep signal quality
- Solution: Band limitation and decimation
- No information loss due to oversampling and Nyquist theorem
- Problem: High computational complexity

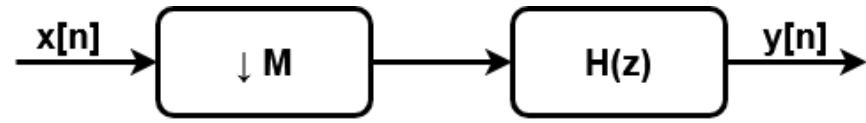


Fig. 13: Block diagram decimator

# Digital Filter

- output is very noisy
- IIR used instead of FIR
- more refined results  
not possible due to time issues
- Quant error variance  $\approx 6.9e-3$

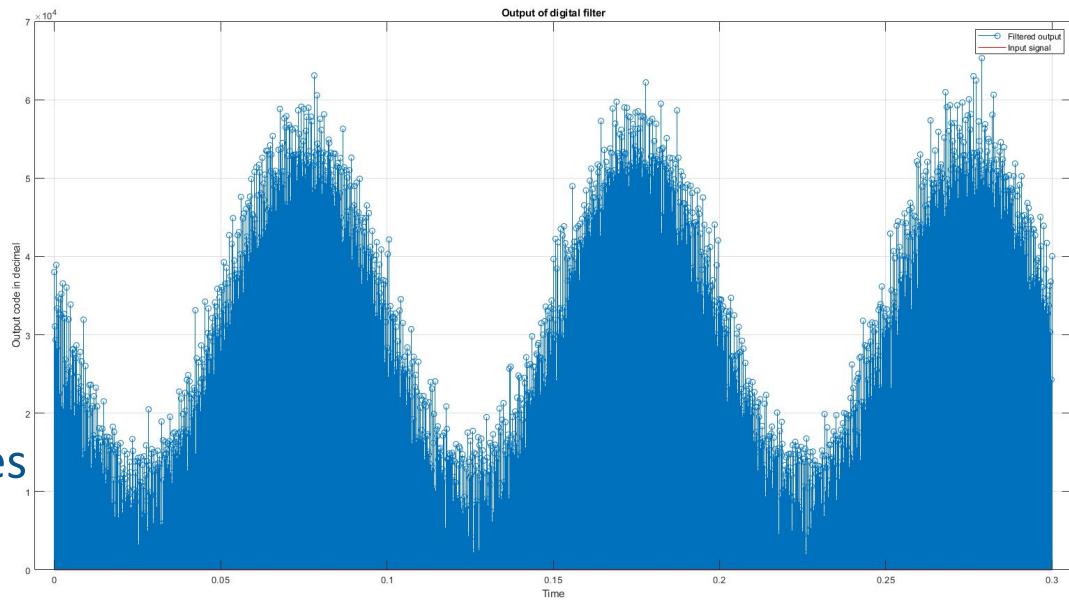


Fig. 14: Filtered output of second order  $\Delta\Sigma$  modulator

# Modulator as a Circuit

# System Implementation on Circuit Level

- idealized model
- mirrors behaviour
- second order  $\Delta\Sigma$  modulator

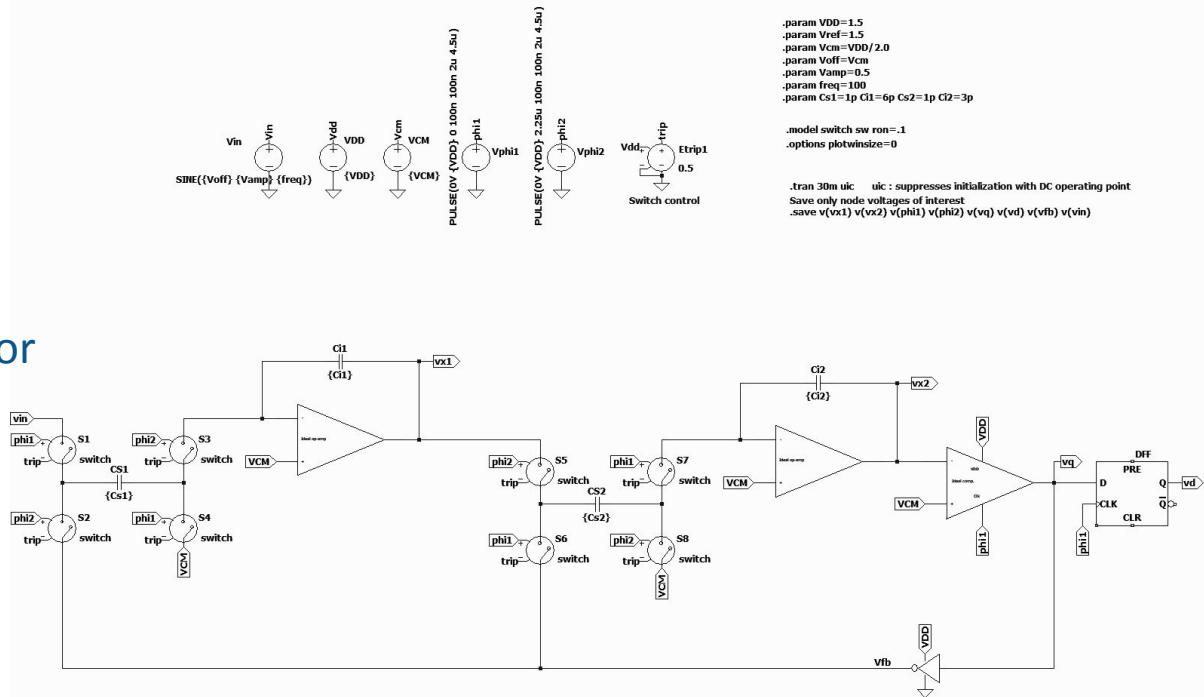


Fig. 15: LTspice Simulation of second order modulator

# LTspice Verification

- Low frequency input
- Noisy output after first integrator
- Lower noise magnitude after second integrator
- High speed PWM output

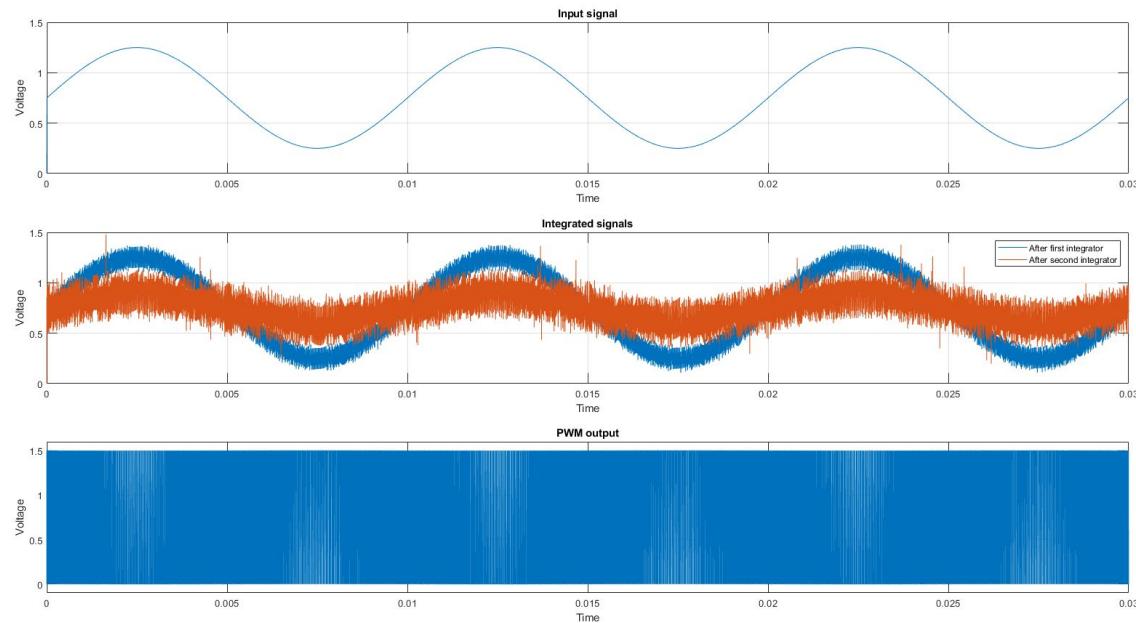


Fig. 16: Output of different stages of LTspice simulation

# Proposals for IC-Design

# Information regarding PDK

Table 3: Devices from IHP SG13G2 PDK [5]

Component	Device Name	Specifications
Low-voltage (LV) NMOS	<code>sg13_lv_nmos</code>	operating voltage (nom.) $\text{VDD} = 1.5 \text{ V}$ , $L_{\min} = 0.13 \mu\text{m}$ , $\text{Vth} \approx 0.5 \text{ V}$ ; isolated NMOS available
Low-voltage (LV) PMOS	<code>sg13_lv_pmos</code>	operating voltage (nom.) $\text{VDD} = 1.5 \text{ V}$ , $L_{\min} = 0.13 \mu\text{m}$ , $\text{Vth} \approx -0.47 \text{ V}$
High-voltage (HV) NMOS	<code>sg13_hv_nmos</code>	operating voltage (nom.) $\text{VDD} = 3.3 \text{ V}$ , $L_{\min} = 0.45 \mu\text{m}$ , $\text{Vth} \approx 0.7 \text{ V}$ ; isolated NMOS available
High-voltage (HV) PMOS	<code>sg13_hv_pmos</code>	operating voltage (nom.) $\text{VDD} = 3.3 \text{ V}$ , $L_{\min} = 0.45 \mu\text{m}$ , $\text{Vth} \approx -0.65 \text{ V}$
Silicided poly resistor	<code>r<sub>sil</sub></code>	$R_{\square} = 7 \Omega \pm 10\%$ , $\text{TC}_1 = 3100 \text{ ppm/K}$
Poly resistor	<code>r<sub>ppd</sub></code>	$R_{\square} = 260 \Omega \pm 10\%$ , $\text{TC}_1 = 170 \text{ ppm/K}$
Poly resistor high	<code>r<sub>high</sub></code>	$R_{\square} = 1360 \Omega \pm 15\%$ , $\text{TC}_1 = -2300 \text{ ppm/K}$
MIM capacitor	<code>cap_csim</code>	$C' = 1.5 \text{ fF}/\mu\text{m}^2 \pm 10\%$ , $\text{VC}_1 = -26 \text{ ppm/V}$ , $\text{TC}_1 = 3.6 \text{ ppm/K}$ , breakdown voltage > 15 V
MOM capacitor	n/a	The metal stack is well-suited for MOM capacitors due to 5 thin metal layers, but no primitive capacitor device is available at this point.

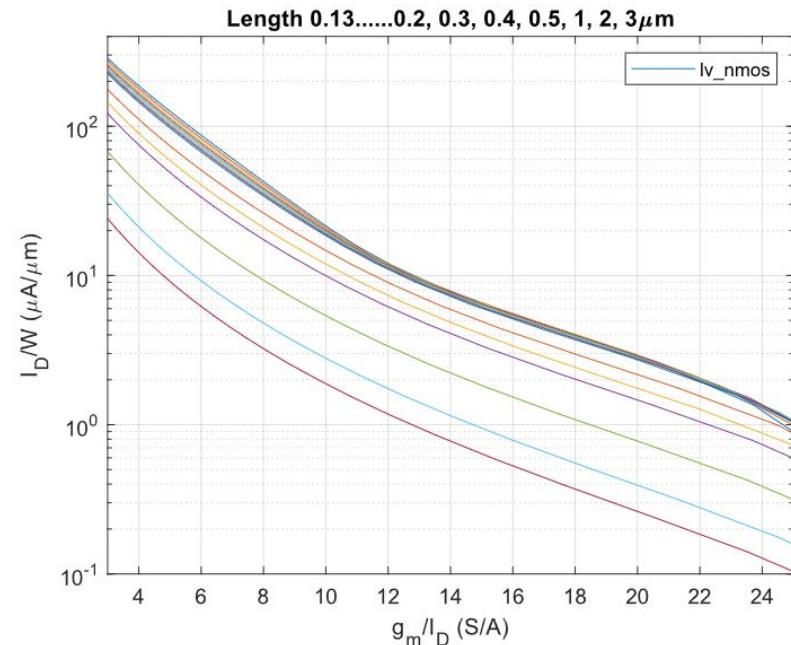


Fig. 17: Tech-Sweep for `sg13_lv_nmos`

# Proposed 5T-OTA

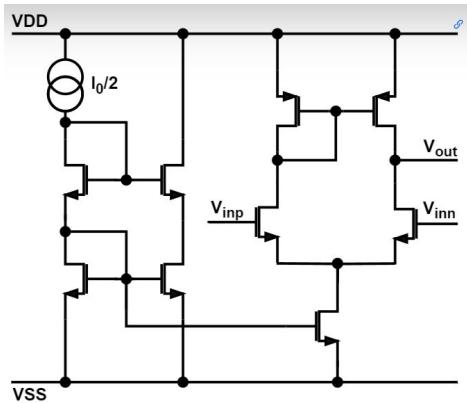


Fig. 18: Architecture of 5T-OTA-Circuit

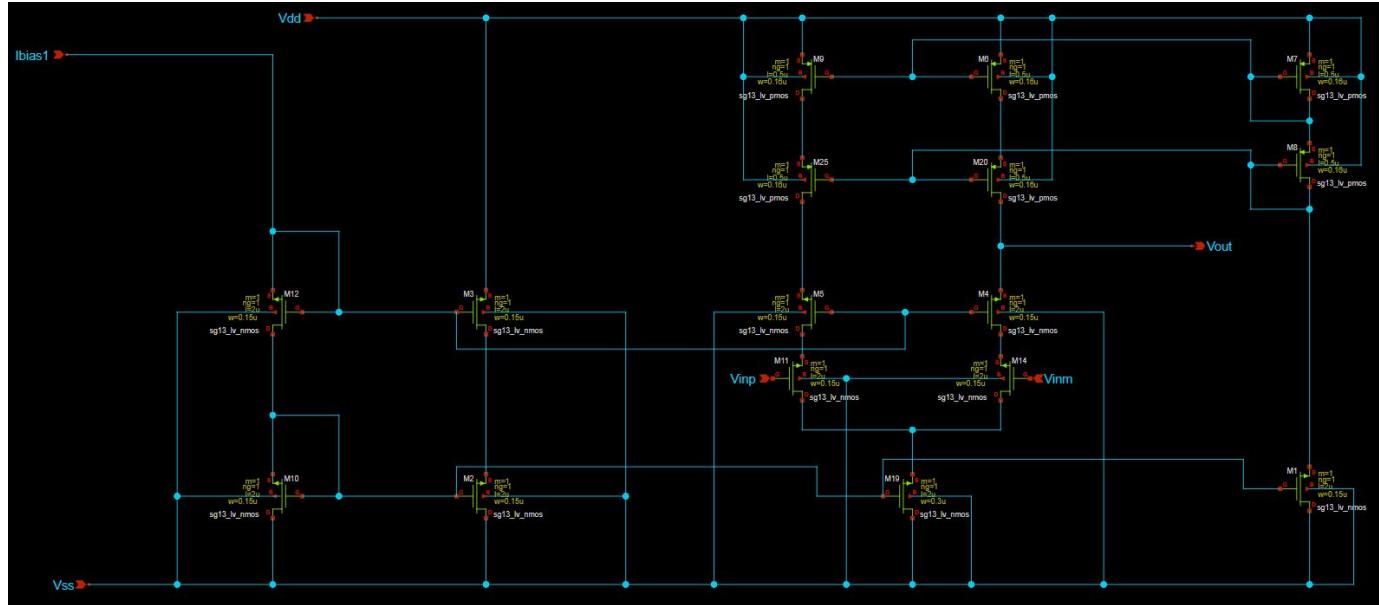


Fig.19: Xschem Circuit of OTA

# OTA Outputs

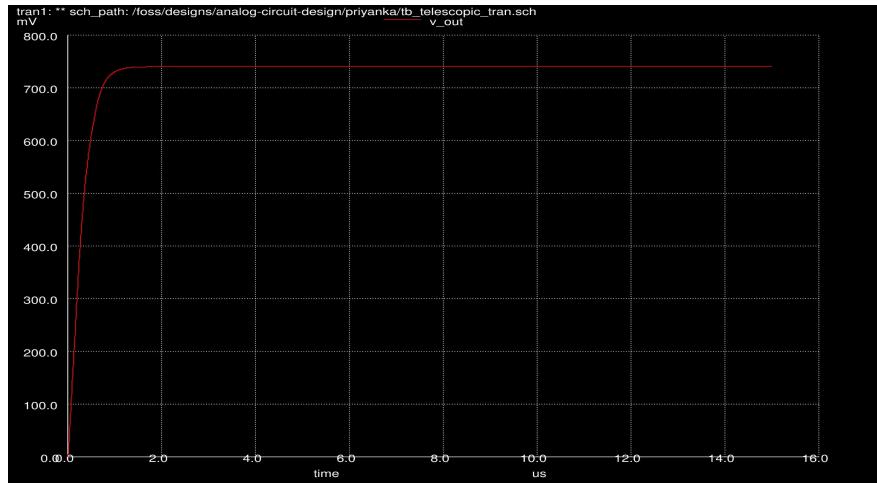


Fig. 20: OTA outputs (transient)

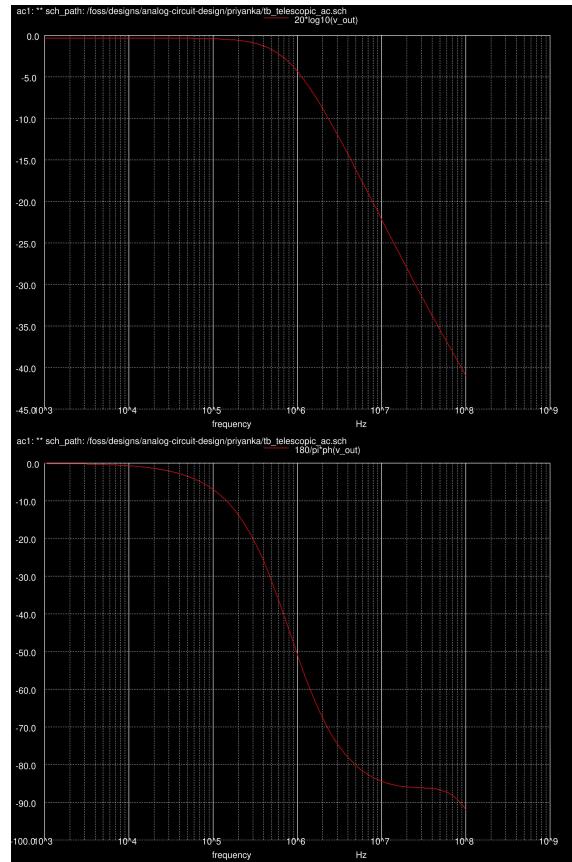


Fig. 21: OTA outputs (AC: magn. & phase)

# Circuit with Switched-Cap. Stages

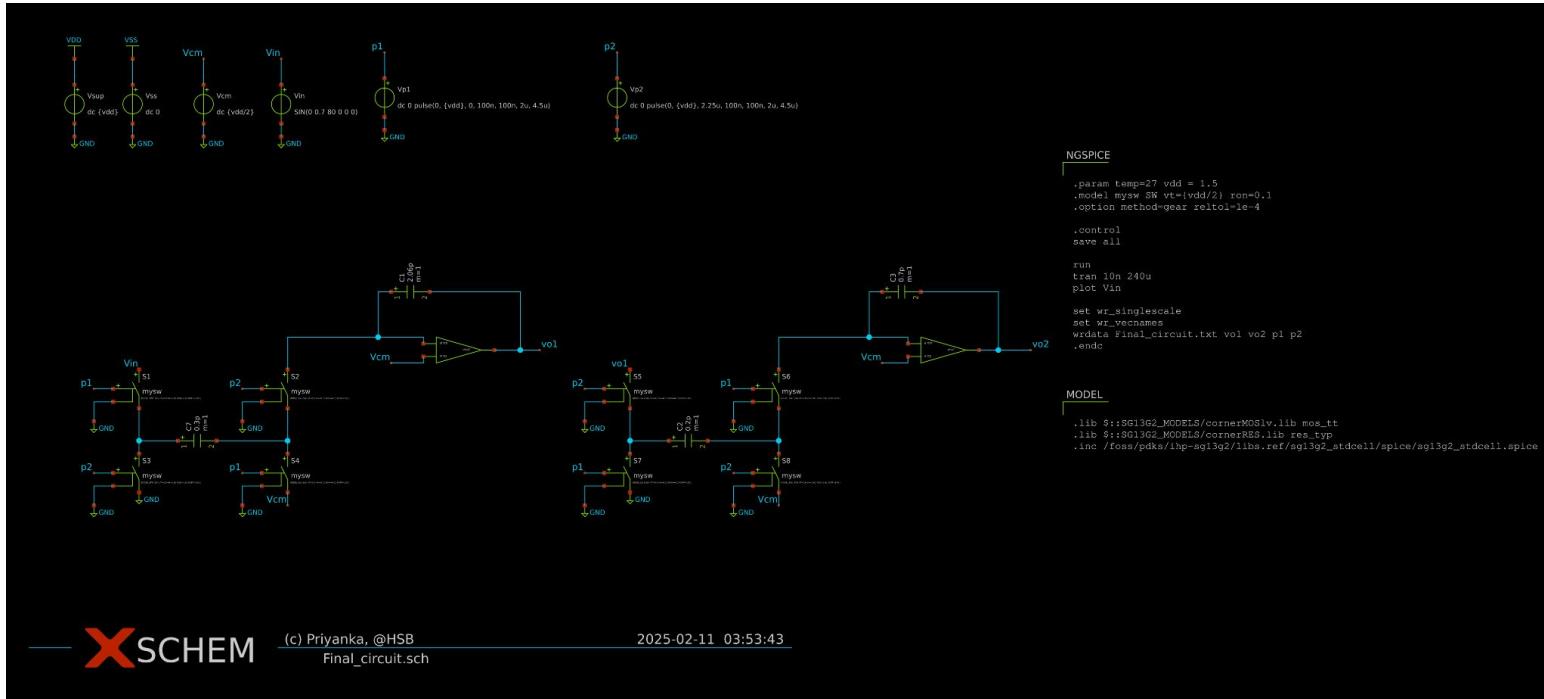


Fig. 22: Final Top Level Circuit Schematic

Final Presentation, CEMS, Gr.4, Speaker: Priyanka Toyni, @HSB

# Clock generator

- ensures no overlap
- controllable delay
- crucial for correct sampling

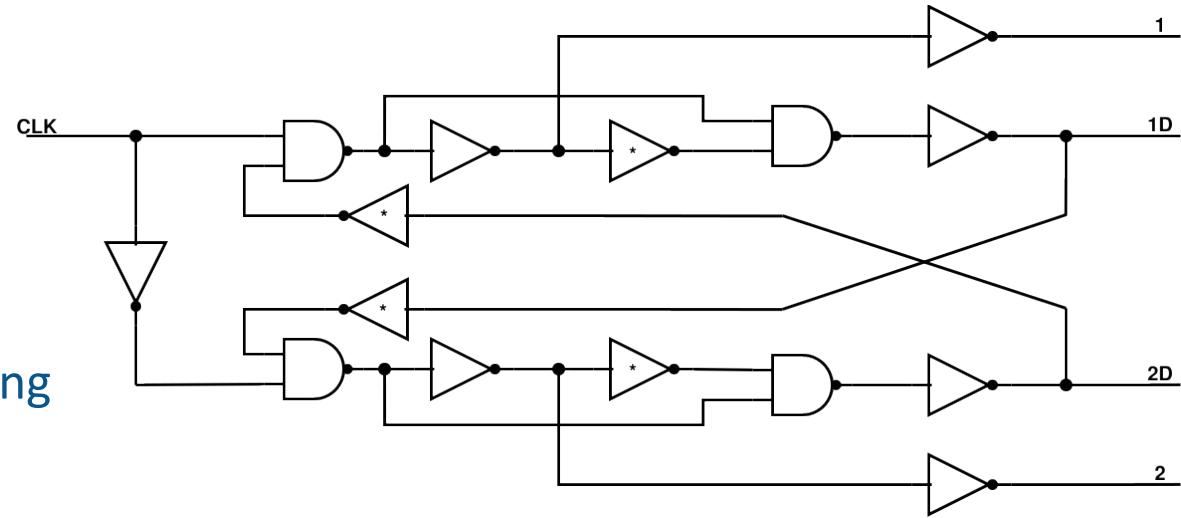


Fig.23: Concept for non-overlapping clock signals

# Clock generator

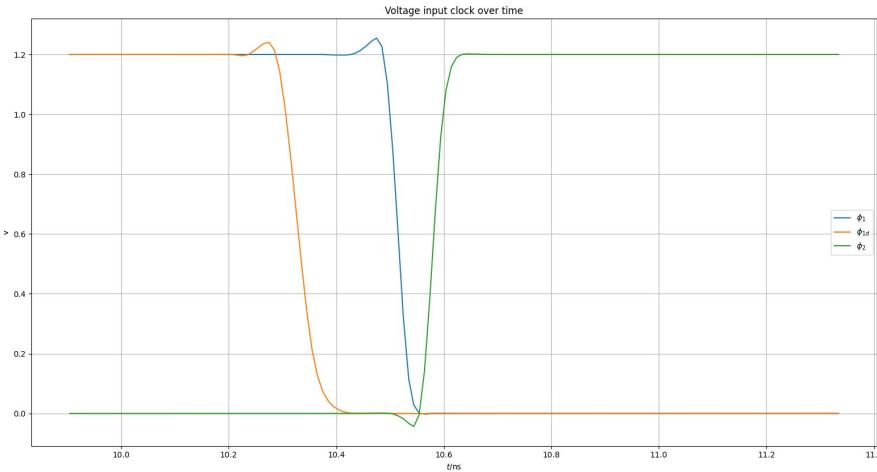


Fig. 24: Clock signals with poor delay

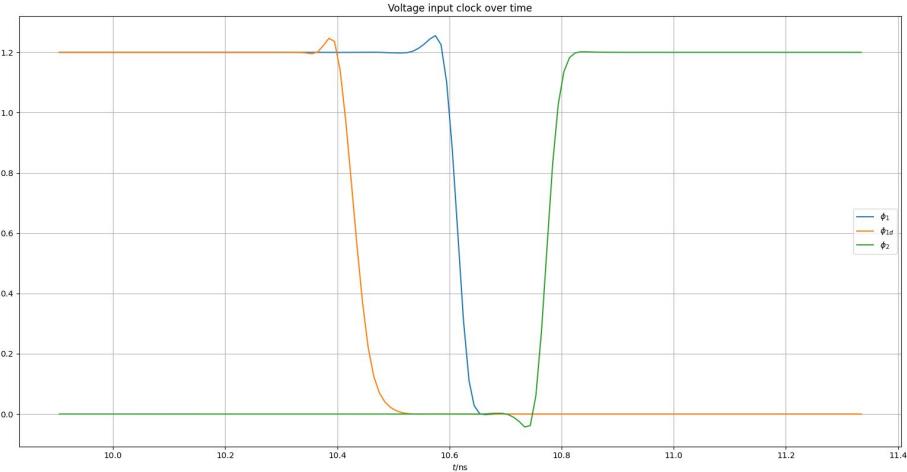


Fig. 25: Clock signals with better delay

# Comparator Design

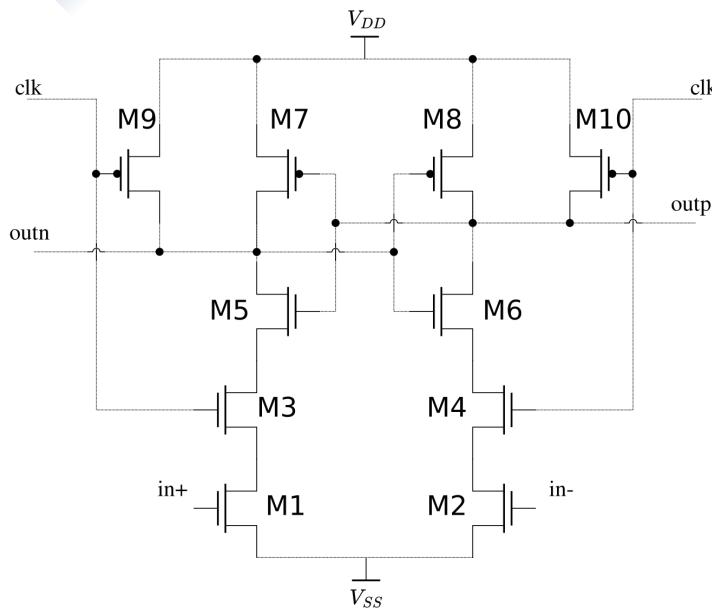


Fig. 26: Inverter-Based Comparator Architecture

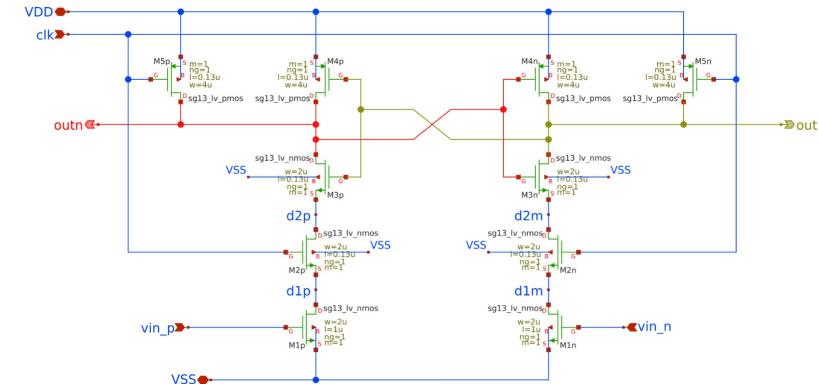


Fig. 28: Xschem Schematic for Comp.

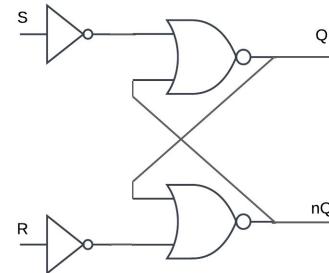


Fig. 27: SR-Latch after Comp.

- *Outp* → *S* & *Outn* → *R*
- SR-Latch output to D-flip-flop

# Comparator Design

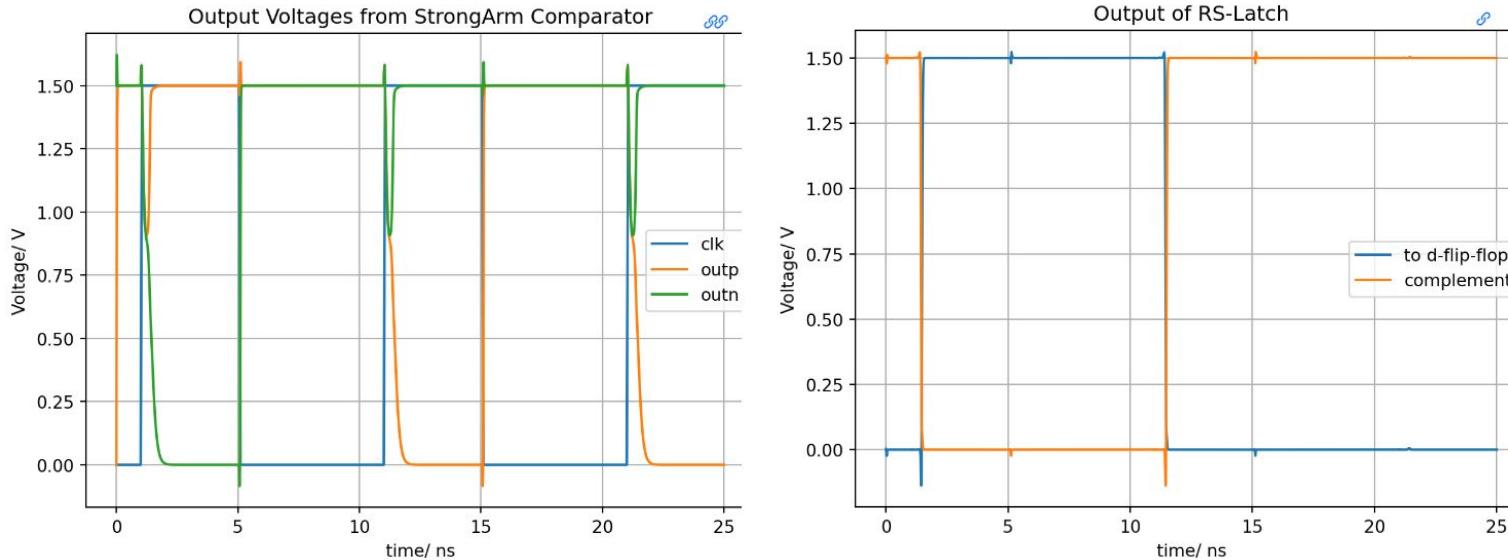


Fig. 29: Simulation Results of Comparator

- 0-8 ns:  $V_{in+} = V_{in-} + 10mV$
- 8.1-25 ns:  $V_{in-} = V_{in+} + 10mV$

# PCB Design

# PCB Design

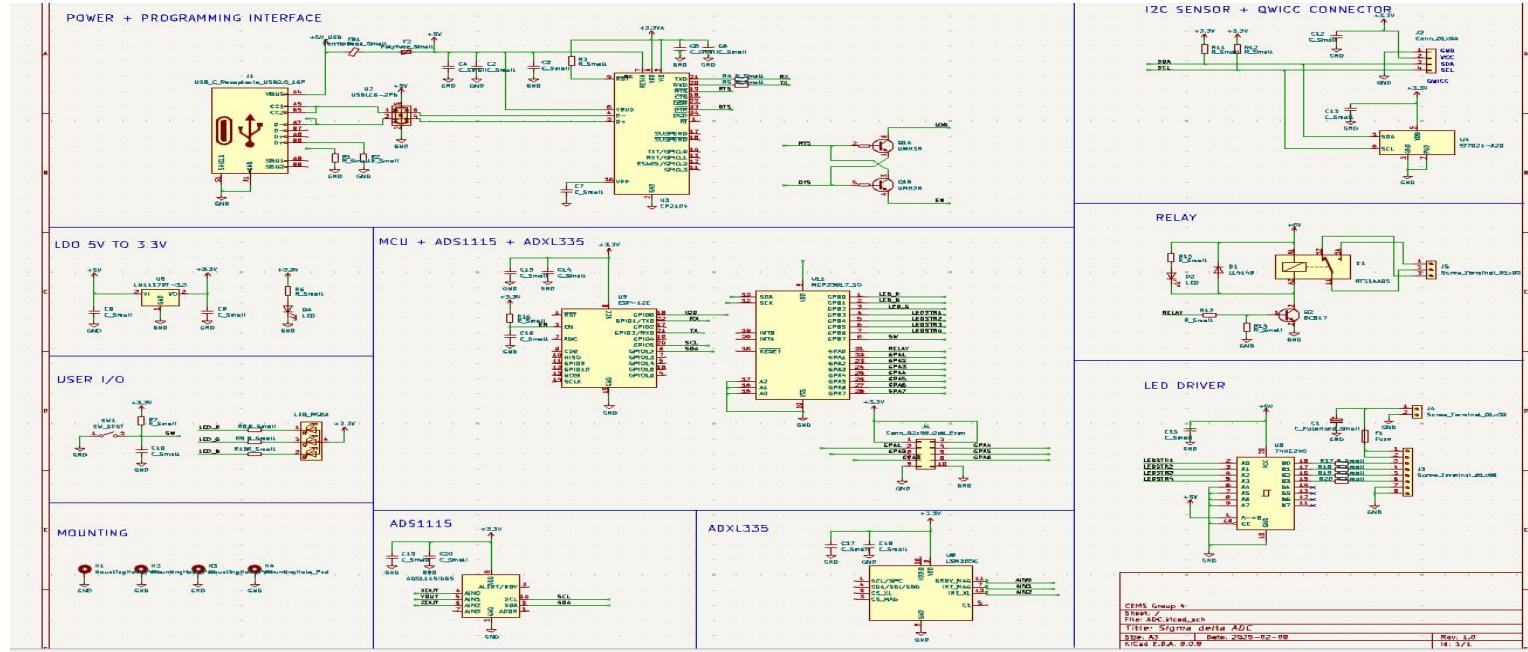


Fig. 30: Schematic Design of PCB

# PCB Physical Design

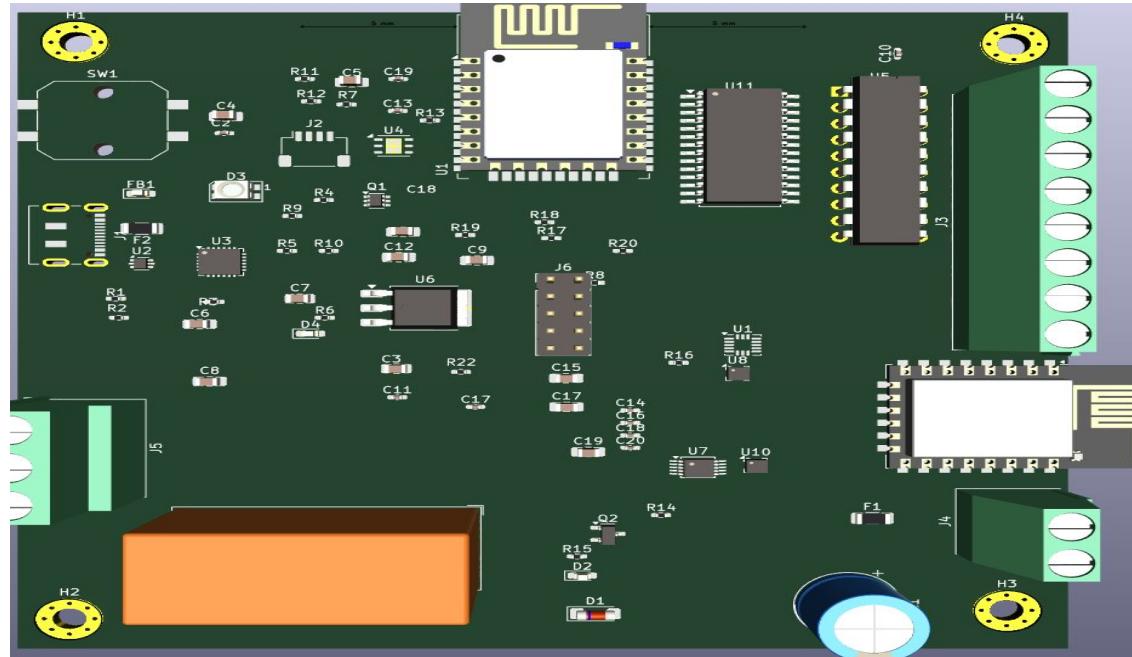


Fig. 31: PCB Design: Layout

# Source Material

[1] [https://micropython.org/download/ESP8266\\_GENERIC/](https://micropython.org/download/ESP8266_GENERIC/)

[2] <https://www.ti.com/product/ADS1115#design-development>

[3] <https://www.distrelec.de/de/achsen-beschleunigungsmesser-adxl335-adafruit-163/p/30129187>

[4] Bonnie Baker. How delta-sigma ADCs work, Part 1. Analog Application Journal (AAJ) SLYT423a, Texas Instruments Incorporation, 2011

[5] Harald Pretl, Michael Koefinger, and Simon Dorrer. Analog Circuit Design, December 2024.

*That's all folks!*