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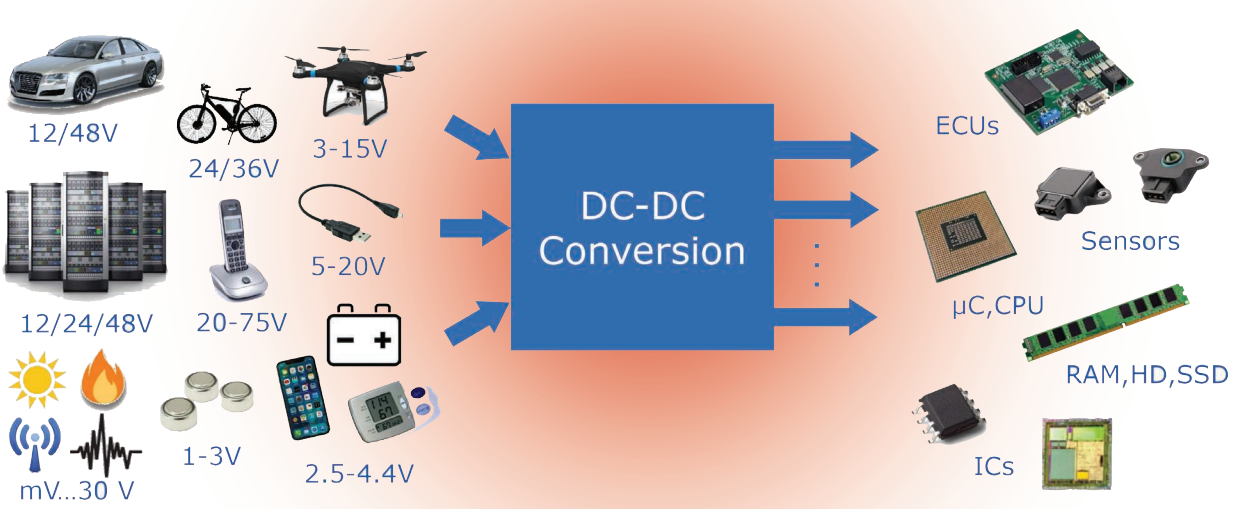
Analog Building Blocks of dc–dc Converters

Examining fundamental concepts



Dc–dc conversion plays the central part in the growing field of power management, which converts input voltages from various different energy sources into circuit-level voltages. At the system level, input voltages may range from a few millivolts (in the case of energy harvesting) to a few volts (in the case of low-voltage batteries). There is a trend toward higher voltages driven by the need to minimize dc–dc conversion losses. For this reason, servers in data centers utilize an intermediate voltage of 48 V [1]. Likewise, hybrid and electric cars are equipped with a 48-V battery in addition to the conventional 12-V board net and the ~400-V high-voltage battery that supplies the drive train [1]. Other applications with higher voltages include USB, e-bikes, or drones.

On the load side, also for reasons of power efficiency, there is an inverse trend for decreasing IC-level voltages toward 1 V and below. In addition, this voltage may vary during operation (dynamic voltage scaling) as does the load current (milliampere in stand-by to amps under full operation). Under all conditions, the dc–dc converter has to supply a stable IC-level voltage at the proper power level while utilizing the energy source at maximum efficiency. Besides efficiency, the size of power management solutions is more and more critical. The key concerns of dc–dc converters include noise immunity (due to switched-mode operation), electromagnetic compatibility, and overall cost.

Figure 1(a) shows the fundamental concept of a step-down dc–dc converter. Although there are many different concepts, such as switched-capacitor or hybrid (combined inductive-capacitive) converters, we will use the conventional inductive converter to derive the operating principle and required analog building blocks of dc–dc converters. The two switches implement the key concept of switched-mode conversion. If S1 is closed, we bring energy into the system. S2 is controlled in a way complementary to S1, which results in a pulsing switching-node voltage, as indicated in Figure 1(b). The passive L and C components

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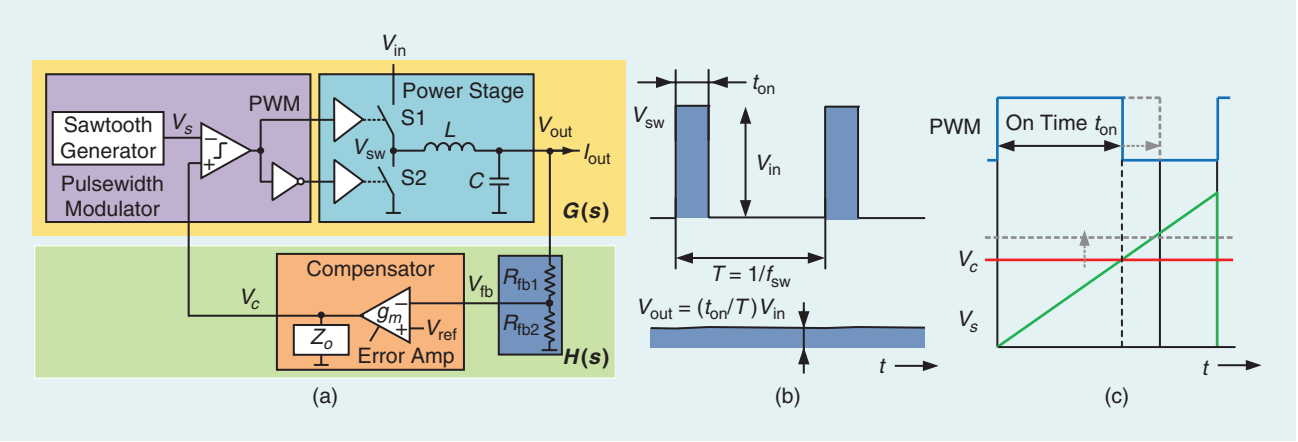

FIGURE 1: (a) A dc–dc converter with waveforms for (b) typical node voltages and (c) pulsewidth modulation (PWM) generation.

have two tasks: 1) they form a low-pass filter, which generates the dc–dc converter's output voltage as the average of the switching node voltage V_{sw}, and 2) they buffer the energy to supply the load while S1 is off. In the ideal case, the static on–off states of the switches are not associated with any losses. In reality, this kind of converter can still reach power efficiencies much higher than 90%. The output voltage can be controlled by varying the pulsewidth at the switching node, which points to pulsewidth modulation (PWM) as a key concept in dc–dc converters. High-switching frequencies f_{sw} result in smaller passives. Although state-of-the-art converters operate at a few megahertz, advanced designs reach 20–30 MHz and higher [1]. Challenges include high-speed circuits such as gate drivers and level-shifters as well increased switching losses and parasitic coupling.

The control loop in Figure 1(a) contains an error amplifier ("Error Amp") that compares the set point given by V_{ref} with a down-scaled value of V_{out}. Hence, its output voltage V_c is a measure of the output deviation (the error). The error amplifier is also referred to as the *compensator* because it shows the certain frequency behavior needed to keep the loop stable (set by Z_o). If S1 turns on for PWM = 1, a sawtooth generator gets activated [see Figure 1(c)]. As soon as the ramp voltage V_s exceeds the error voltage V_c, the PWM resets to zero. A load step at the output will pull down V_{out} slightly. Due to the inverting behavior of the compensator, V_c increases and causes V_s to cross at a later point in time. As the on time of the PWM pulse increases, S1 brings more energy

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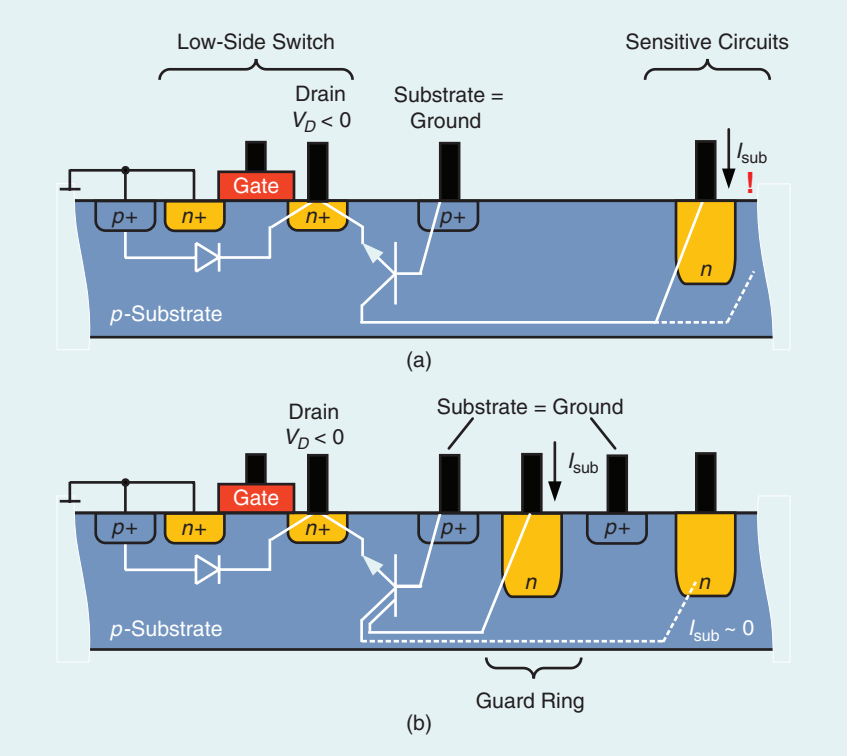

FIGURE 2: (a) A power switch cross section with parasitic junctions that forms a parasitic n-p-n transistor. (b) A surrounding guard ring prevents parasitic currents from propagating toward sensitive circuit blocks.

Active integrators allow for shifting the starting point and endpoints of the ramp such that they fit to the common-mode range at the error amplifier's output and the comparator's input.

into the system and counteracts the load step. Hence, a stable control is achieved by varying the duty cycle at the power stage. The ramp generator may be as simple as a current source that charges a capacitor. However, active integrators allow for shifting the starting point and endpoints of the ramp such that they fit to the common-mode range at the error amplifier's output and the comparator's input.

Any transistor can be utilized as a power switch (see S1 and S2 in Figure 1). Low-voltage transistors are well suited for forming a power device with fast switching behavior and a small layout area. Due to their lower on-resistance, most power switches are n-type devices. For higher voltages (>5 V), double-diffused MOS transistors and drain-extended devices are available in technologies with high-voltage capabilities. To achieve a low on-resistance, the drive voltage $V_{GS} = V_{drv}$ should be as large as possible, typically up to 5 V while the W/L ratio of the power transistor is scaled up accordingly. Because capacitive gate charging is associated with losses, proper switch-transistor sizing requires a tradeoff between on-resistance (static losses) and gate capacitance (dynamic losses).

As the switching node sees an inductive load, it may be pulled below ground potential during the dead time while S1 and S2 are off. This causes the parasitic body diode to become forward biased, as displayed in Figure 2(a). Any p-n-junction is associated with a parasitic bipolar transistor structure [2]. In this case, a parasitic n-p-n device is formed with the body diode as the base-emitter junction. Any nearby n-well, perhaps in sensitive analog circuit blocks, will act as a collector. To prevent any malfunction and even latch up, every NMOS transistor with its drain connected to a pin needs to be surrounded by guard-ring structures that act as the nearby collector, as shown in Figure 2(b) [2].

The actual power stage consists of a gate driver and a level shifter in addition to the power switch, as

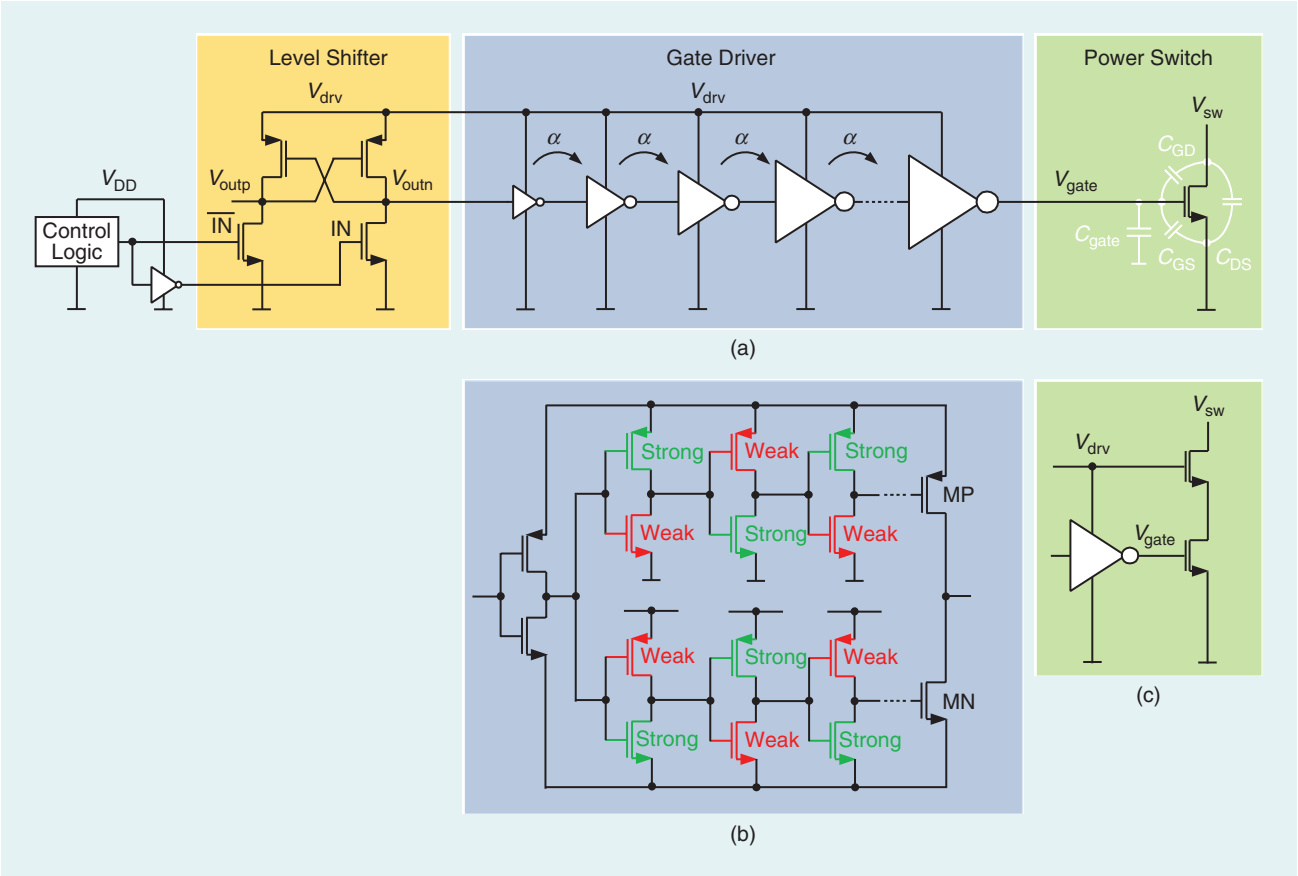

FIGURE 3: (a) A low-side power stage with a level shifter and gate driver, (b) a split-path gate driver that eliminates cross currents in the final driver stage, and (c) a stacking of low-voltage transistors.

depicted in Figure 3. The gate driver has to turn on the power transistor with sufficient gate overdrive voltage V_{drv}. For this, a simple CMOS inverter may be sufficient. For larger power devices, a cascaded driver approach will result in steeper edges and lower switching losses in the power stage. This is similar to driving capacitive off-chip loads. Each inverter stage increases by $\alpha \sim 3$–6 in driving strength. Low-power drivers aim to avoid a large number of stages (cross currents), which results in larger α. Figure 3(b) shows a split-path driver that prevents cross currents in the final stage; cross currents typically account for 50% of overall losses in the gate driver [3], [4]. The level shifter converts the driver control signal from the low-voltage domain into the driver-voltage domain. The cross-coupled type of driver shown in Figure 3 is widely used because it does not draw any dc current. As the two NMOS devices at the input are driven from the a low-voltage domain while the PMOS devices are controlled by V_{drv}, the NMOS transistors need to be strong enough to toggle to the level shifter. For $IN = 1$, V_{outn} is pulled to zero, which propagates through an odd number of driver stages to turn on the power switch. In advanced technologies, dc–dc converters can benefit significantly from low-voltage switch stacking in terms of both lower dynamic losses and area consumption [5], [6] [Figure 3(c)].

Due to their lower on-resistance, most power switches are n-type devices.

The high-side driver in Figure 4 has a similar structure. In the usual case of an n-type power switch, the driver may be referred to the switching node if V_{in} exceeds the maximum gate-source voltage of the power transistor. This way, low-voltage devices can be used in the gate driver because the maximum voltage is defined by V_{drv} and not by V_{in}. The driver comprises a resistor-based level shifter, which is the simplest but suffers from static current. It also needs a clamping diode to protect the maximum gate-source voltage at the driver input. If the high-side switch turns on, the switching node will approach V_{in}. Hence, the gate overdrive voltage needs to be greater than V_{in}.

In dc–dc converters, bootstrapping is the most common way to provide the high-side gate supply by means of a bootstrap capacitor C_{boot}, as displayed in Figure 4. C_{boot} is recharged from an internal supply via diode D when the low-side switch is on. As

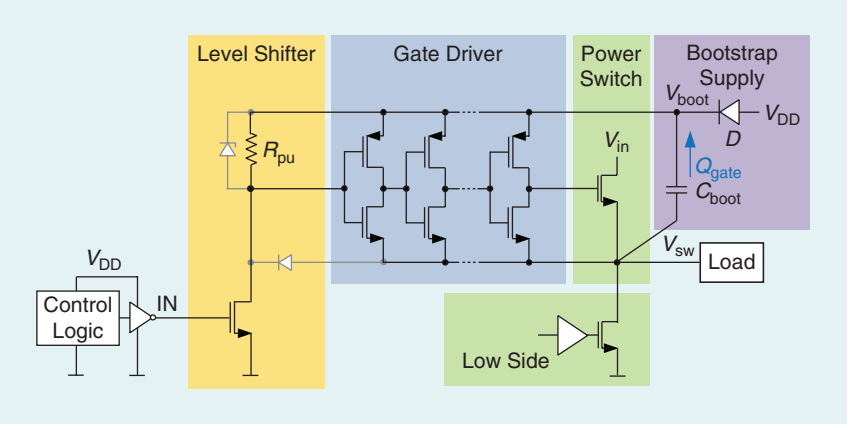

FIGURE 4: A high-side driver with bootstrap supply.

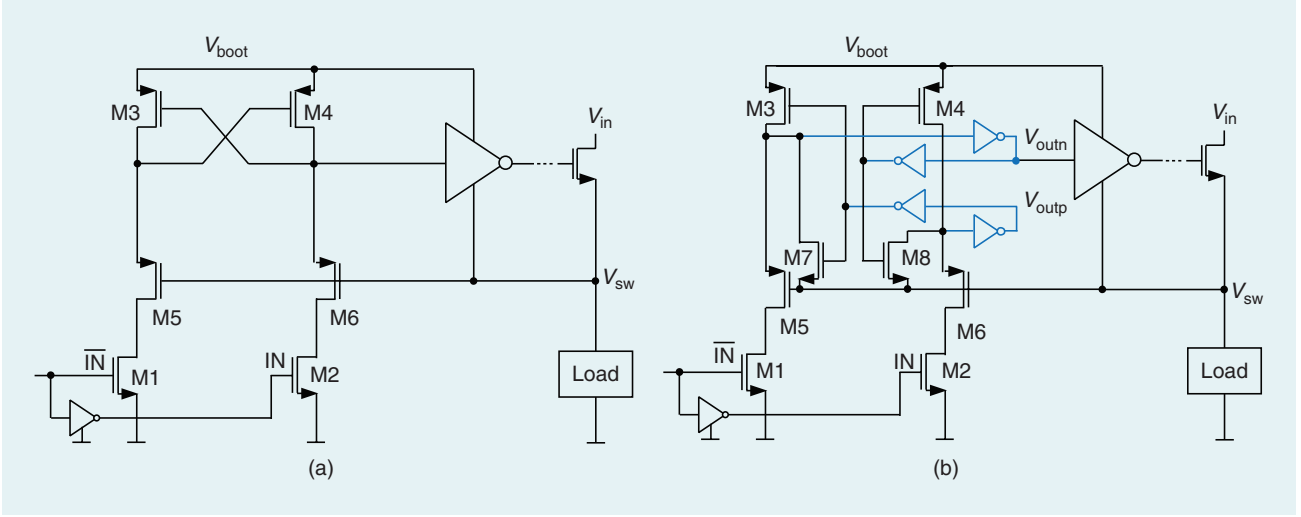

FIGURE 5: High-voltage versions of cross-coupled level shifters. (a) A basic circuit and (b) an extended version with M7 and M8 to ensure full swing at the gate-driver input.

For larger power devices, a cascaded driver approach will result in steeper edges and lower switching losses in the power stage.

soon as the high-side switch turns on, D blocks, and C_{boot} delivers the gate charge for the high-side switch in addition to leakage and dc currents in the attached circuits. Assuming C_{boot} needs to deliver a charge of 10 nC, we find that $C_{boot} > 100$ nF if its voltage drop is required to be below 0.1 V. Hence, C_{boot} is typically placed off-chip.

Figure 5 shows two high-voltage versions of a cross-coupled level shifter [7] to be used at the high side to avoid the disadvantages of the resistive-level shifter. Although the simple cross-coupled circuit of Figure 3(a) is restricted to the maximum source-gate voltage of the cross-coupled PMOS transistors (<5 V), high-voltage cascode devices M5 and M6 allow for much higher values of V_{in}. The source-gate voltages of M5 and M6 in Figure 5(a) prevent a zero level (which is equal to V_{sw}) at the gate-driver input and may cause cross currents. This is addressed by the extended version in Figure 5(b).

Coming back to the control loop, a folded cascode design or symmetrical operational amplifier is suitable for the error amplifier [see Figure 6(a)], as too much loop gain may impact stability. At start-up, the output capacitor C (see Figure 1) may be fully discharged and cause large in-rush currents, which result in component stress, disturbances, electromagnetic interference issues, and so on. This can be prevented by adding a soft-start circuit that bypasses the differential input stage, as shown in Figure 6(a). $C_s = 5$ pF and $I_s = 10$ nA result in a typical start-up slope within 1–10 V/ms [see Figure 6(b)]. Because I_s is very low, it

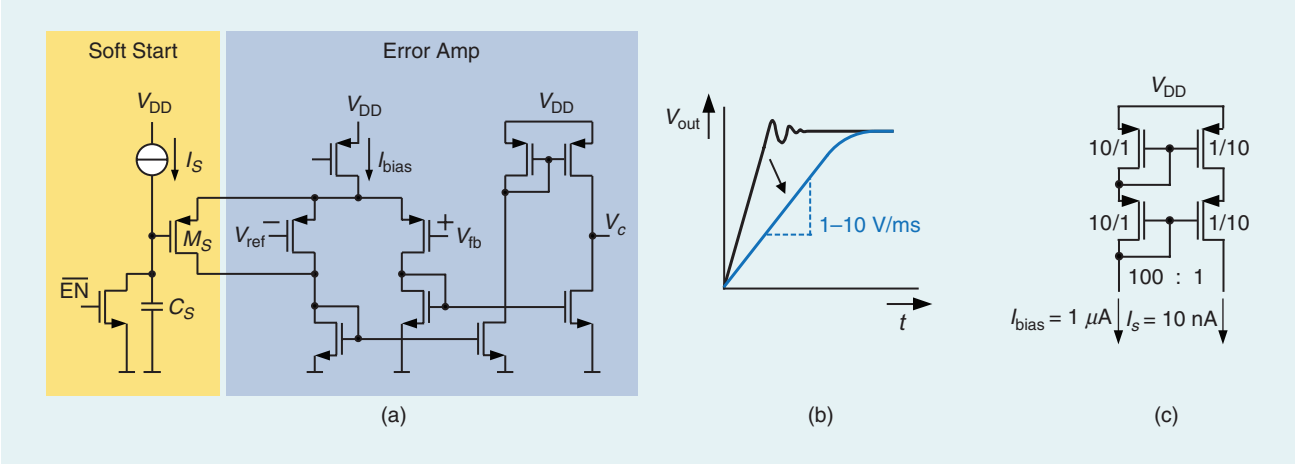

FIGURE 6: (a) An error amplifier with soft start, (b) a dc–dc converter output at start-up, and (c) the generation of the start-up current.

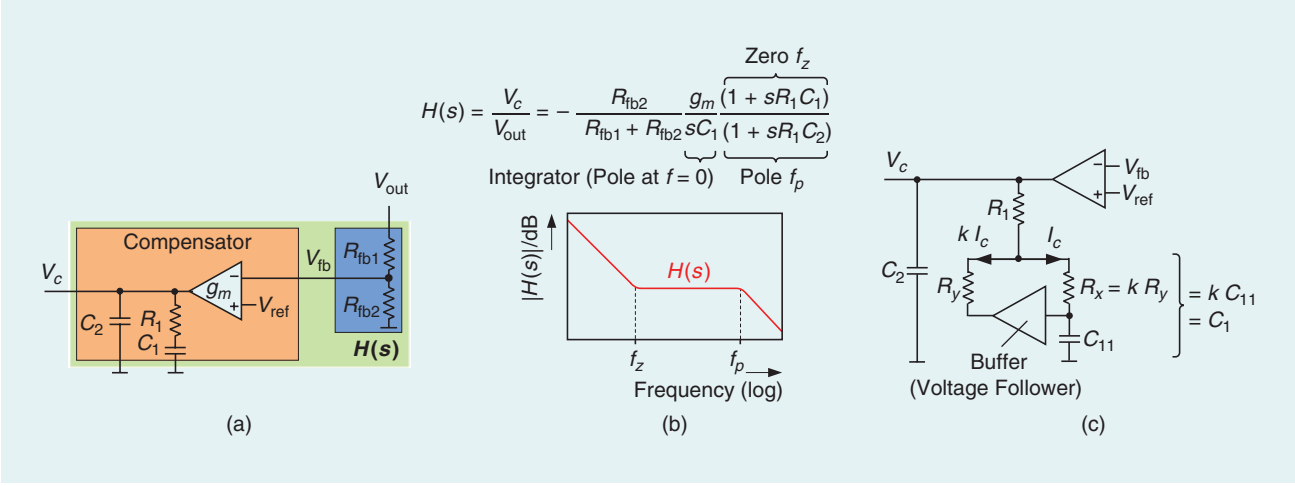

FIGURE 7: (a) A frequency compensator, (b) the transfer function H(s) and Bode plot, and (c) the capacitor multiplier.

can be generated by a current mirror [see Figure 6(c)], which violates any matching rule but gives sufficient accuracy for a soft start.

The plant, consisting of the power stage and pulsewidth modulator [see Figure 1(a)], forms a second-order transfer function $G(s)$ with a double pole at $1/\sqrt{2\pi LC}$. The compensator, which defines $H(s)$, needs to insert zeroes and poles (Z_o in Figure 1) such that the loop gain reaches 0 dB at 0.1–0.3 f_{sw} to prevent any in-band switching noise and maintain a sufficient phase margin of, typically, 60°. Figure 7(a) and (b) shows a compensator along with its transfer function. The crossover frequency of the loop gain $G(s)H(s)$ is aimed to be positioned at between f_z and f_p. For example, $f_z = 10\,\text{kHz}$ and $f_p = 87\,\text{kHz}$ result in $R_1 = 4\,\text{k}\Omega$, $C_1 = 4\,\text{nF}$, and $C_2 = 457\,\text{pF}$. Although all the passives are traditionally placed off-chip, more and more applications do not want to deal with loop compensation. This requires the passives to be fully integrated. Figure 7(c) illustrates a way to utilize a current-mode capacitor multiplier to implement C_1 [8], [9]. $C_{1.1} = 200\,\text{pF}$ and $k = 20$ emulate the behavior of a 20-times larger capacitor C_1. If R_x and R_y are transistors in the triode region, they can even be reconfigurable to adaptively adjust the dynamic behavior, i.e., in case of a load step.

Dc–dc converters may also include monitoring and protection circuits used for overtemperature, overvoltage/current, diagnostics for short circuit and open load cases, undervoltage lockout, and any kind of current sensing.

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About the Author

Bernhard Wicht (bernhard.wicht@ims.uni-hannover.de) received his Dipl.-Ing. degree from TU Dresden in 1996 and his Ph.D. degree from TU Munich in 2002. Between 2003 and 2010, he was with Texas Instruments, Freising, and was responsible for the design of automotive power management ICs. He has been a professor at Reutlingen University, and he is currently chair of the Mixed-Signal IC Design Department at Leibniz University Hannover, Germany. He was a corecipient of the 2015 ESSCIRC Best Paper Award and the *IEEE Journal of Emerging and Selected Topics in Power Electronics* 2019 First Prize Paper Award. In 2018, he received the teaching award of the Faculty for Electrical Engineering and Computer Science at the University of Hannover. He is currently an IEEE Solid-State Circuits Society Distinguished Lecturer and a member of the IEEE International Solid-State Circuits Conference Technical Program Committee.

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