# Philip Tracton

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*Southern California*
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## Experience

2010–Present **Instructor**, *UCLA Extension*, Westwood, CA.

- *Learning Python* – Taught an introduction to Python course that leads the students from installing Python to building their own weblog with a database backend. Taught class live and online.
- *Embedded Software 1* – This class introduces students to programming in C for an embedded ARM Cortex-M3 microprocessor.Students learn to write simple code to control hardware, handle interrupts and ultimately develop tasks running on FreeRTOS. Taught this class live and online.
- *Using FPGAs in Embedded Systems* – The class introduces the students to Verilog and developing modules and test benches. Students ultimately program the Digilent Nexys-2 board with designs to control a variety of peripherals including UART, LED, and memories. Taught this class live and online.

2013–Present **Principal. IC Design Engineer**, *Medtronic Neuromodulation*, Northridge, CA.

- *Pump Motor IC* – Digital IC developer on new electronics package for updating and enhancing the Synchromed II device.
- *Haptix* – Firmware developer on DARPA funded project for prosthetic hand. Implemented the low level signal processing algorithms, battery management and battery recharge code. Lead unit testing effort of the low level code. Managed a team of 3 contractors to accomplish this goal in time.
- *CoSimulation* – Developed new techniques for simulating multiple ICs together. This includes new simulation tools, RTL and firmware. This lead to simulating die stacks and then whole hybrids. This technique has saved significant time and money in reducing board debug, bring up time and respins. This environment became the verification platform for several firmware, IC stacks and board projects.
- *Hardware SubRoutines* – Continued as a developer on the primary MCU platform shared by Neuromodulation and Cardiac divisions. Debugged and repaired the hardware implemented mathematical operations.

2006–2013 **Sr. IC Design Engineer**, *Medtronic Neuromodulation*, Northridge, CA.

- *s0906a* – Installed and configured 2 IP blocks (DMA and SPI). Implemented 2 custom blocks, a hardware based firmware task scheduler and MAD to AHB Bridge.
- *s0905a* – Lead firmware engineer for new ARM Cortex-M3 based System On Chip. Created CMSIS compliant proto-type device drivers, boot $\mu$COS II, developed test applications, and boot ROM with symbolic linking all in simulation. Developed large demo application once silicon arrived.
- *D452* – Project lead for porting a pre-existing design from 0.6$\mu$ AMI/ON to 0.25$\mu$ TSMC. Replaced the memory and clock tree, added in ECC detection and control logic, significant power reduction while mantaining the same pad foot print.
- *D281* – Member of the team to design and implement the next generation digital ASIC for implantable devices. Responsible for implementing and testing DSP algorithms, 32 bit ALU, Timers, I2C core and power analysis in 0.25 micron technology.
- *Common Platform FPGA* – Lead the team that is implementing the prototype to a new ASIC on a custom made Spartan 3 FPGA development board. Design includes a CPU, interfacing to memory, ADC and other custom hardware. Developed test benches, real time test software and boot code.

2002–2006 **Embedded Software Engineer**, *Medtronic Diabetes*, Northridge, CA.

- *Vascular Glucose Monitoring System* – Implemented and debugged the software for a new glucose calculation and new sensor recalibration algorithm. All embedded code was in assembly. Created a new testing architecture to allow automated testing of embedded code.
- *2007 Implantable Pump Software* – Maintained and enhanced existing product software. Supported devices in the field and laboratory.

2000–2002 **Embedded Software Engineer**, *Zuma Networks*, West Hills, CA.

- *Fatal Error* – Upon the crash of one of the embedded boards this program would collect information about the operating system, including a stack trace of the crashed task, capture the current state of the CPU and board, store the information to flash and reboot the system.
- *Live Test* – Developed an active task running at all times to confirm that the system is in an operational state. Upon detection of an error condition or a hot swap of certain cards this task reconfigures the hardware to compensate for the change.
- *Self Test* – Maintained and enhanced power on self test. At power on this task would go through the system to confirm that all parts are working. If a component failed, the failure and possible causes would be reported.
- *Frame Generator* – Designed, developed, and debugged traffic generating program. This program can dynamically change the relevant parameters for custom traffic needs.
- *Device Drivers* – Developed, implemented and debugged device drivers to custom ASICS and FPGAs

1998–2000 **Software Engineer**, *Teradyne*, Agoura Hills, CA.

- *Scan Data Memory API* – Responsibilities included design, documenting, planning, scheduling, implementing and leading the team of engineers to create a new APU to the Scan Data Memory embedded on the Scan Path Option Board. Implemented the whole project in C/C++ on Solaris and finished ahead of schedule.

## Computer Skills

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|---|---|
| Languages | C, Python, Perl, Assembly (ColdFire, x86, PPC, Cortex-M3/M4), Verilog, VHDL |
| Operating Systems | Linux, FreeBSD, OpenBSD, Microsoft Windows (98/NT/ 2000/XP/7/10), ATI Nucleus Plus, $\mu$COS-II, FreeRTOS |

Tools Xilinx ISE/Vivado, Modelsim, Simvision, NCVerilog, Altera Quartus, SVN, Git, LaTeX

## Education

2002–2005 **Master of Science in Electrical Engineering**, *California State University Northridge*, Northridge, CA.

Project The Dynamic Burnin of the forward and inverse 2D Discrete Cosine Transform on a XC2V3000

Advisor Professor Ramin Roosta

1993–1998 **Bachelor of Science in Electrical Engineering**, *University of Maryland*, College Park, MD.

## Publications

MAPLD 2004 **A Re-Programmable Platform for Dynamic Burn-in Test of Xilinx VirtexII 3000 FPGA for Military and Aerospace Applications**.

Conference `http://www.klabs.org/mapld04/index.html`

Paper `http://klabs.org/mapld04/papers/p/p108_roosta_p.doc`

Presentation `http://klabs.org/mapld04/presentations/session_p/p108_roosta_s.ppt`

## References

**Availabe upon request**.