Parameterized FIFO in Verilog

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2.1 Parameters

- **dw** is the data width. This is used to size the internal memory of the FIFO and the $data_{in}$ and $data_{out}$ parameters. It should specify the exact size of the data since internally 1 is subtracted to zero the size. For example set this to 32 for 32 bits and $data_{in}$ and $data_{out}$ will be [31:0].
- **depth** is the number of samples stored in the FIFO.

2.2 Signals

Signal Name	Direction	Size	Behavior
wb clk	Input	1	Clock for synchronous behavior
wb rst	Input	1	Synchronous reset
push	Input	1	Signal to write data into FIFO
pop	Input	1	Signal to read next data from FIFO
data in	Input	dw	Data that push writes into the FIFO
data out	Output	dw	The current output value of the FIFO
empty	Output	1	Goes high if there is no data in the FIFO
full	Output	1	Goes high if the FIFO has all locations populated
number samples	Output	based on depth	The current number of samples in the FIFO

2.3 Writing

2.4 Reading

3 FIFO Testing

3.1 Run Simulations