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## Introduction

This board allows designers to quickly evaluate the performance of Xilinx's 64-bit / 66 MHz PCI core including data throughput capabilities across the PCI bus to an on-board SDRAM SODIMM module. In addition it serves as a prototyping platform for PCI and different system applications.

Expansion capability is provided through an interface standard known as DIME. Two DIME module sites are present on the PCI card providing users with the ability to build custom systems from a variety of solutions provided by this royalty free, open module standard.

# Ballyinx PCI64 PCI Prototyping Board

Data Sheet

## **Features**

- Fully compliant universal PCI Slot Card
- Automatically adjusts I/O buffers to match V<sub>IO</sub> using auto-sensing circuitry
- PCI 2.2 compliant
- Supports 32 & 64 bit PCI in frequencies up to 66 MHz
- Expansion capability for additional functionality through 2 DIME Module Sites
- Requires only a 5V supply from the host motherboard
- Configured over SelectMap Interface from Flash memory via 95144XL CPLD
- Flash memory reconfigured via Xilinx MultiLINX download cable
- Sub-10 ms configuration time compliant with 64-bit PCI specification requirements
  - 50Mbytes per second configuration rate
- Direct SelectMAP Virtex configuration using MultiLINX download cable
- PCI & SDRAM demonstration bitstream
- Demonstration software
- 4M x 64 (32Mbytes) SDRAM in SODIMM socket
- 12 LEDs showing:
- Power good for 5V, 3.3V, 2.5V & 1.8V
- V<sub>IO</sub> level and 3.3V or 5V bitstream loaded
- FPGA DONE pin
- Three user LEDs Expandable to 23 LEDs
- 50MHz and programmable oscillator



Figure 1: Ballyinx PCI64 Prototyping Board

## **General Description**

The Nallatech PCI64 Prototyping Card is provided with the Xilinx PCI64/66 Design Kit, available from Xilinx. This card allows designers to quickly evaluate the performance of the Xilinx PCI64/66 LogiCORE design in their system. Moreover, it serves as a prototyping platform for custom PCI and system applications. The firmware and software provided clearly demonstrate the capabilities of the LogiCORE design along with the performance enhancements that the Virtex offers for SDRAM applications.

Further, the Nallatech PCI64 board demonstrates how to build a universal PCI card. A universal PCI interface requires the inclusion of diode clamps to 3.3 V for a 3.3 V signaling environment, and the exclusion of these in a 5 V signaling environment. To accomplish this, the Virtex FPGA must load different bitstreams depending on the signalling environment. This card demonstrates one way of achieving this.

The Xilinx PCI64 Design Kit provides the user with a PCI design example. This includes a demonstration bitstream with:

- Xilinx Real 64/66 PCI interface
- Xilinx PCI Bridge interface core
- Xilinx SDRAM Interface core

The SDRAM and PCI Bridge reference designs used for the demonstration bitstream are available from Xilinx to registered users of the PCI core.

The block diagram, seen in Figure 2, shows the basic interconnectivity of the various interfaces to the Virtex FPGA.

Two pieces of software demonstrate the performance of the PCI bus and the SDRAM interface capabilities of the Virtex FPGA.

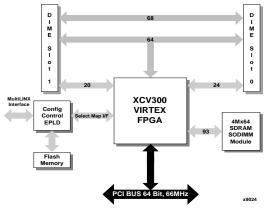


Figure 2: PCI64 Card Block Diagram

The Virtex FPGA is configured at power on over its Select Map interface from an high speed Flash memory. An XC95144 CPLD controls the Flash and the transfer of data to the FPGAs Select Map port. This data is transferred over the selectmap port at 50MBytes/Sec, thus allowing the FPGA to be configured in under 10 milliseconds. This is a 50x improvement over the fast serial mode transfer rate.

Two DIME Module sites provide the user with access to an ever growing variety of interfaces and data processing nodes. In fact, full system solutions can be developed with just this card and one or two DIME modules. Therefore the user often need not bother with the development of custom PCBs for a solution to their system problem. For more details on available DIME modules and more information on the standard, go to the Nallatech web site,

http://www.nallatech.com

## Configuration

The FPGA must be configured in less than 100 mS in order for the PCI interface to detect the PCI bus width (32- or 64bits). In order to achieve this the Select Map configuration mode is utilized together with an Intel Fast Flash memory. An XC95144 CPLD is used to control the booting process.

The Flash memory can be erased and reprogrammed with new bitstreams using the Xilinx MultiLINX Download Cable. The CPLD, under the control of either the PCI signalling voltage (Vio) or the MultiLINX cable, if connected, will enter one of several modes:

#### Default Mode (no MultiLINX cable connected)

- Load 3.3 V PCI bitstream from Flash Memory
- Load 5 V PCI bitstream from Flash Memory

#### Program Mode (MultiLINX cable connected)

- Erase 3.3 V PCI bitstream
- Erase 5 V PCI bitstream
- Program 3.3 V PCI bitstream
- Program 5 V PCI bitstream
- · Pass-through mode for direct programming of Virtex

The default mode demonstrates how a universal PCI card can be built. The Program mode gives the user control over the flash chip.

Alternatively, Nallatech provides a product that can be added to a user's PCI interface that allows the Flash Configuration Memory to be reprogrammed directly over the PCI interface using a software Utility. This allows users of the PCI logicore to easily integrate Firmware Field upgrades into their products.

## Software

Two software programs are included, one demonstrating the performance of the PCI bus and the SDRAM interface capabilities of the Virtex FPGA and the other allows the user to program the flash and FPGA via the MultiLINX cable.

### **Device Driver Program**

This demonstration program, shown in Figure 3 and Figure 4, provides a GUI interface to the PCI Bridge Design part of the PCI LogiCORE. The SDRAM is connected to the back of this bridge and DMA transfers to and from this memory can be performed and the transfer rate is displayed. This interface also provides the user with the basic operation of the Xilinx PCI Bridge Design.

This programs also allows the user to download an image to the SDRAM memory and retrieve it. Any errors in the transfer will be recorded and graphically displayed on the GUI. For more details on the inner working of the FPGA design, refer to the *Bridge Design for the Ballyinx PCI64 Prototyping Board* data sheet, available in the PCI64 lounge.

Virtex Card (PCI Bridge) T Help	est Harness - 32 bit 33MHz	Slot
MA Control Registers Spe	cial Functions Image Transfers	Logging
Original Image	Returned Image	569.552032 : Wrote 0x00400000 to CONTROL         569.682512 : Read 0x0042058B from COUNTER         569.682625 : Read 0x0060000 from CONTROL         569.682632 : Wrote 0x00400000 to CONTROL         569.68263 : Wrote 0x00400000 to CONTROL         569.68263 : Wrote 0x00400000 to CONTROL         569.791866 : Read 0x0036F368 from COUNTER         569.791927 : ***Reading All Registers***         569.792021 : Read 0x0000000 from XFER_LEN         569.792117 : Read 0x00000000 from XFER_LADR         569.792214 : Read 0x00000000 from CONTROL         569.792213 : Read 0x00000000 from CONTROL         569.792413 : Read 0x00000000 from CONTROL         569.792413 : Read 0x00000000 from CONTROL         569.792619 : Read 0x00000000 from MASTER         569.792619 : Read 0x00000000 from MASTER         569.792622 : Read 0xA0080000 to XFER_LADR         569.792922 : Wrote 0xA0080000 to CONTROL         569.792922 : Wrote 0x40004000 to CONTROL         569.793024 : Wrote 0x40000400 to CONTROL
C 1 line C 32 lines	Returned Image	
<ul> <li>Get lines</li> </ul>	C Arith. Difference	Clear Save
C 128 lines	C Different Pixels	

Figure 3: ImageTransfer Demonstration

Virtex Card (PCI Bridge) Test Harness - 32 bit 33MHz Slot				
le <u>H</u> elp				
DMA Control       Registers       Special Functions       Image Transfers         DMA Control       Direction         Transfer Length       128       Direction         Local Address       Image Transfer       Image Transfer         Use Interrupt       Image Transfer       Image Transfer         View Buffer       Go       Image Transfer         DMA Performance       Number of DMA Transfers       0         Last Transfer       Image Transfer       Image Transfer         # of PCI Bus Cycles       N/A       Image Transfer         # of Bytes       N/A       Image Transfer         # of Disconnects       N/A       Image Transfer         # of Master Cycles       N/A       Image Transfer	Logging 569.552032 : Wrote 0x00400000 to CONTROL 569.682512 : Read 0x0042058B from COUNTER 569.682663 : Kernel LoadedVersion = 1.42 569.682663 : Wrote 0x00400000 to CONTROL 569.791866 : Read 0x0036F368 from COUNTER 569.791027 : ***Reading All Registers*** 569.792011 : Read 0x0000000 from XFER_LEN 569.792011 : Read 0x0000000 from XFER_LADR 569.792117 : Read 0x0000000 from XFER_LADR 569.792117 : Read 0x0000000 from CONTROL 569.7921317 : Read 0x0000000 from XFER_LADR 569.792508 : Read 0x0000000 from MASTER 569.792508 : Read 0x0000000 from MASTER 569.792619 : Read 0x0000000 from XFER_LADR 569.792619 : Read 0x0000000 from XFER_LADR 569.792212 : Read 0x0000000 from XFER_LADR 569.79222 : Read 0x0000000 from XFER_LADR 569.792024 : Wrote 0x40000400 to CONTROL 569.793024 : Wrote 0x4000400 to CONTROL 569.793024 : Wrote 0x40000400 to CONTROL 560.793024 : Wrote 0x40000400 to CONTROL 560.79302			

Figure 4: Block Mode DMATransfer Demonstration

#### **MultiLINX Access**

The MultiLINX access program, as seen here in Figure 5, provides a means for the user to erase and program the 3.3 V and 5 V bitstreams in the on-board flash device, and to directly program the FPGA via a pass-through mode in the CPLD. The CPLD handles the details of programming the flash device, accepting data from the MultiLINX cable via the SelectMAP interface.

Allatech download via XILINX MultiLI Eile Help Connected at 38400 baud Baud Rate     O Auto     O 9600     O 19200     O 19200     O COM3 ♥     OCM4 ♥	Flash Memory Operations  Flash Memory Bank  5 Volt  3.3 Volt  Erase  Program
Progress 0% complete Ready	Program Onboard Virtex Program

Figure 5: MultiLINX Access Program

# **Options**

All options are available directly from Nallatech.

- · Additional Ballyinx boards
- Ballyinx boards with Virtex V800 FPGA
- JTAG FPGA Configuration Software (for FPGAs on DIME Modules)
- Reprogram Bitstream in Boot Flash Via PCI Interface (for easy field upgrades)
- Ballyvision NTSC/PAL Video Capture and Display DIME Module
- Ballyblue Dual V1000 Virtex FPGA DIME Module for over 2 Million Gates
- Ballytest DIME Connector Breakout Module
- Ballydiff Low Voltage Differential Signalling, LVDS, DIME Module
- Custom DIME Module Design Service is Available

For the latest information on new DIME modules, visit the Nallatech web site:

http://www.nallatech.com

# **Ordering Information**

The PCI64 board is available from Xilinx as part of the PCI64 Design Kit.

The Design Kit includes:

- Xilinx Real 64/66 PCI LogiCORE Interface
- Ballyinx PCI64 Prototyping board
- Compuware Driver Bundle with SoftICE - Includes Full Production License
- MultiLINX Download cable
- MultiLINX Ballyinx connectors
- Printed documentation

The part numbers are:

- DO-DI-PCI64-DK
- DX-DI-PCI64-DK

Contact your local Xilinx sales office to purchase these parts.

Note: The part DX-DI-PCI64-DK requires the user to have already purchased either a DO-DI-PCI64 or DO-DI-PCI64-DK.