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Questions:

1.
Timeout Period = (1/clock frequency) * (1 or 16) * (PS + 1) * (REF + 1)
Timeout Period = (1/80MHz) * (1) * (80 + 1) * (1699 + 1) = 1.721ms
The delay would be 1.721ms instead of 1.7ms, which is in error of 1.22%.

2.
a. MCU_RSTIN_b
b. Active Low, so that a logic 1 corresponds to an electrical low signal, and vice versa.
c. This signal is connected to pin 141, which is called !RSTIN_B.
d. Primary reset input to the device. Asserting RSTI immediately resets the CPU and peripherals.

3.
a. PB1_SW
b. It is connected to pin 93, which is called IC0/OC0/PWM1.
c. The primary function is GPT0, the tertiary function is PWM1, and the quaternary function is PTA0.
d. The port is TA.
e. SW1 is connected to pin 0 of port TA.
f. We first have to program the port TA Pin Assignment Register (PTAPAR)
g. MCF_GPIO_PTAPAR &= ~3;
h. This GPIO register is called the Port Data Direction Register (DDRTA)
i. MCF_GPIO_DDRTA &= ~1;
j. The GPIO register we would need to access is called the Port Pin Set Data Register (SETTA).
int sw1 = MCF_GPIO_SETTA & 1;