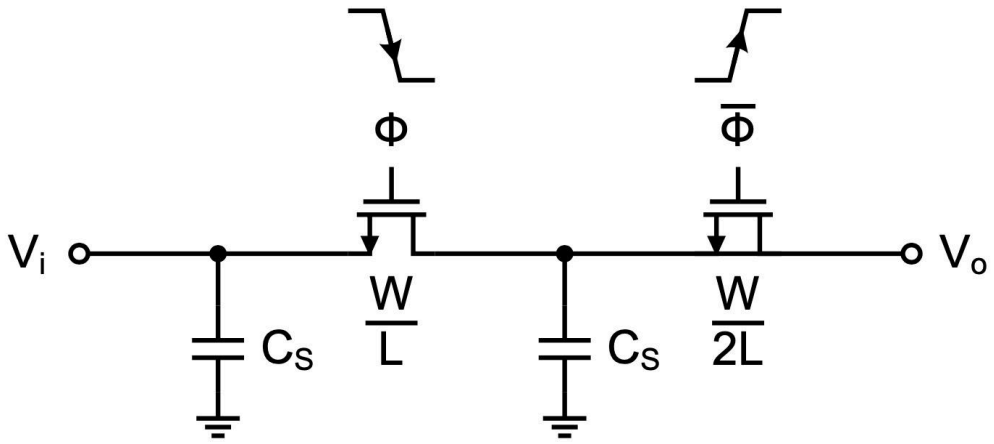
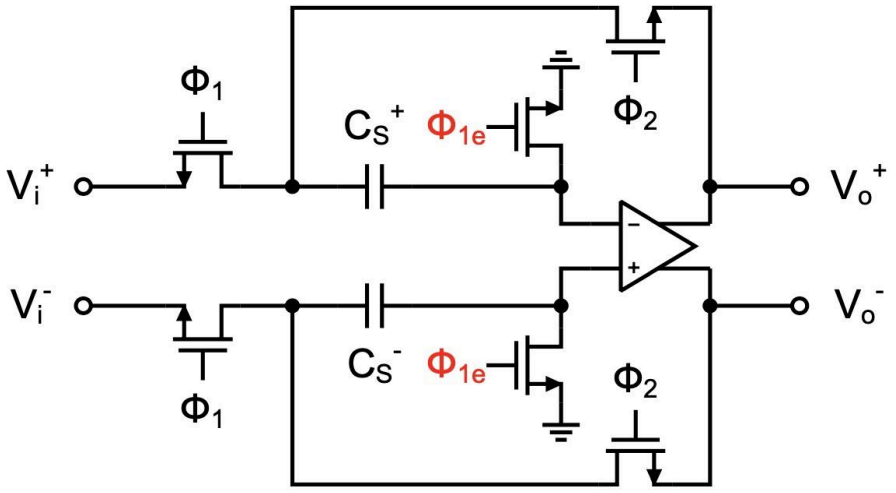
ADC Stage by Stage Schematics

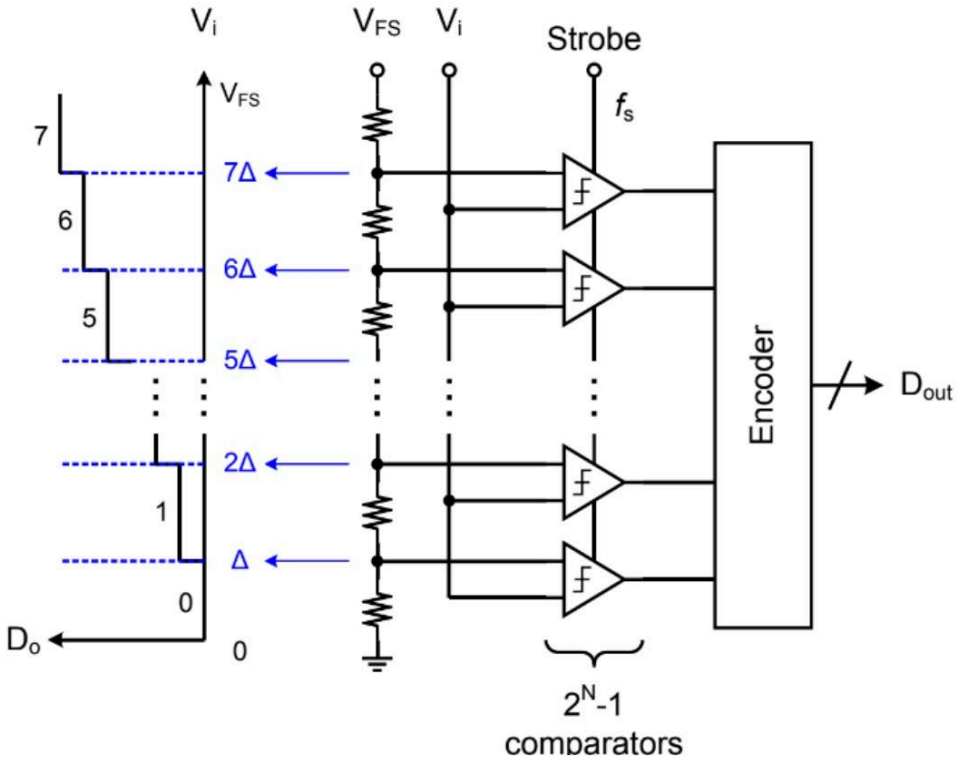
Sample and hold stage:



Better implementation of the sample and hold stage:



ADC architecture:



Level shifters from comparator array to encoder inputs:

Priority Encoder 8:3 (implemented on FPGA with LSB tied to logic 1)