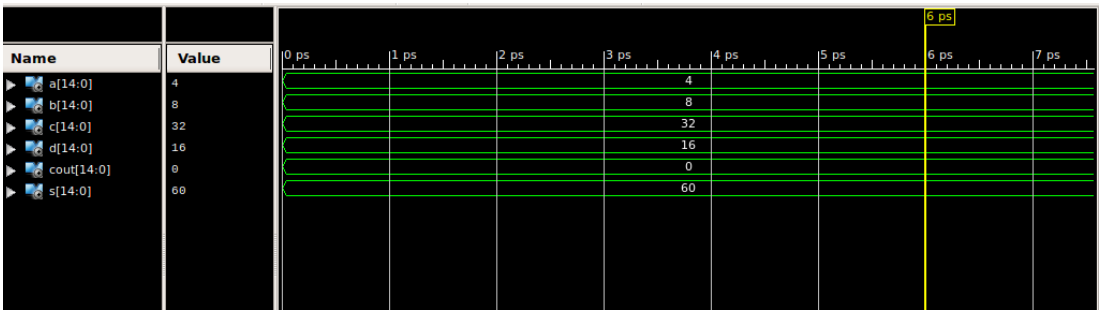
Yuan Zhang – 387552 Shan Kuan - 387516

LAB Assignment 2 - Moving Average Filter

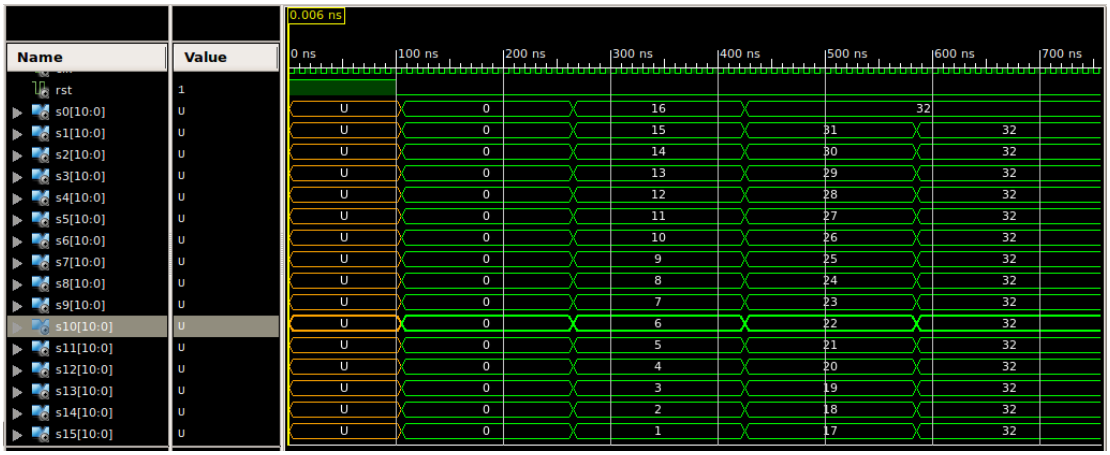
Simulation Results

- Wave forms

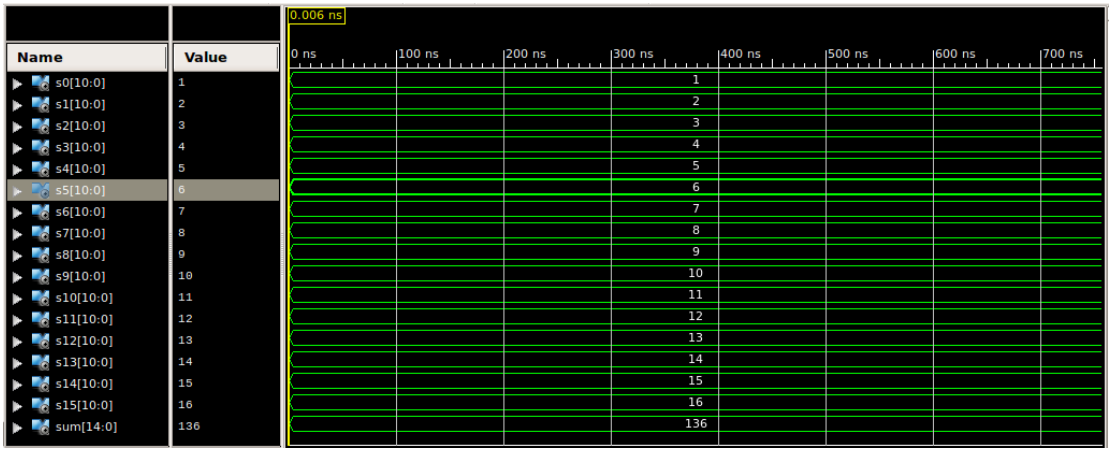
1. Carry Save Adder



2. Input Registers

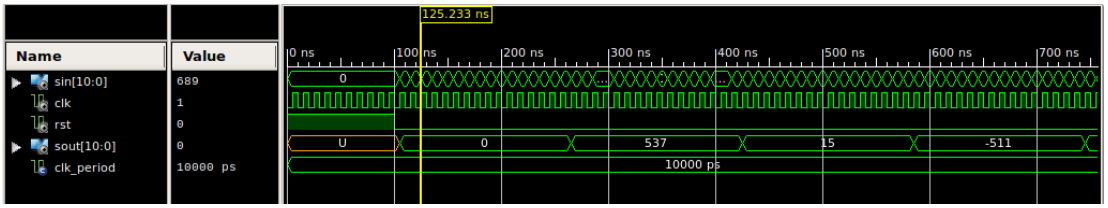


3. 16 Operand Adder

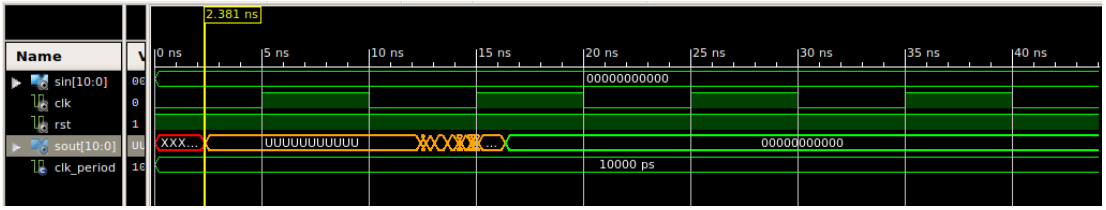


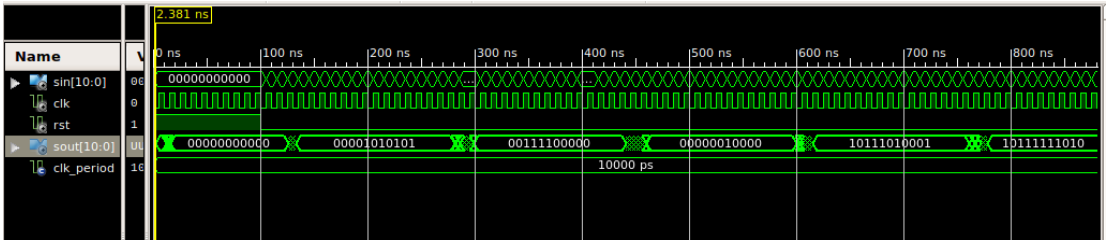
4. Moving Average Filter

Behavioral

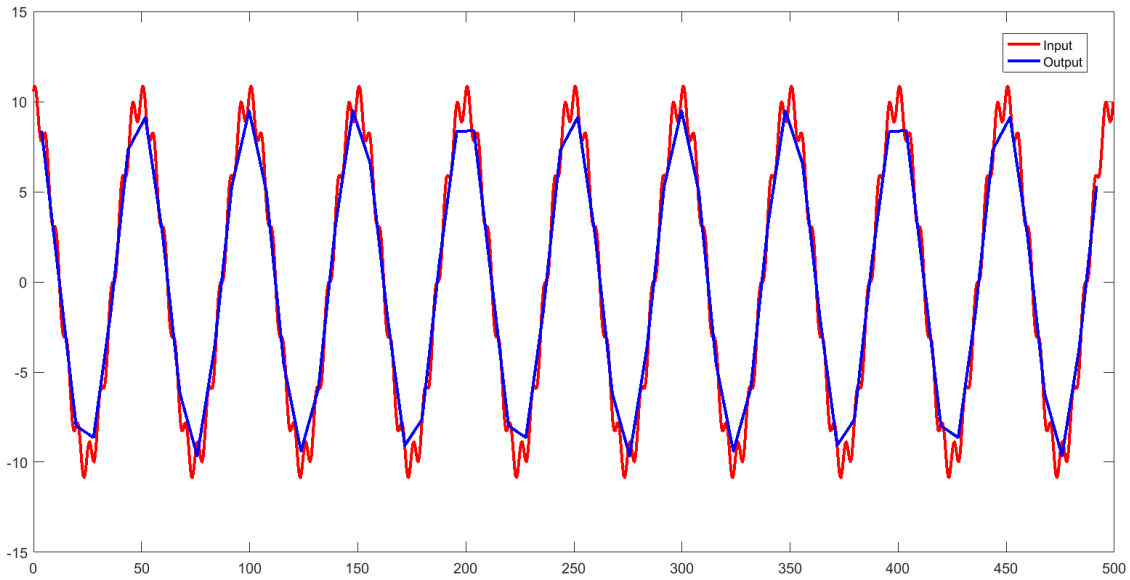


Post-Route





- Moving Average Filter Response



Frequency Analysis

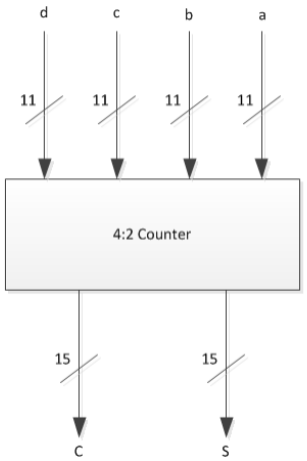
```
Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 2.289ns (Maximum Frequency: 436.862MHz)
   Minimum input arrival time before clock: 1.731ns
   Maximum output required time after clock: 24.017ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 2.289ns (frequency: 436.862MHz)
  Total number of paths / destination ports: 175 / 169
-------------------------------------------------------------------------
Delay:               2.289ns (Levels of Logic = 1)
  Source:            u1/count_0 (FF)
  Destination:       u1/count_0 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: u1/count_0 to u1/count_0
                              Gate     Net
```

As we can see in the timing report above, the calculation delay of the critical path is **2.289ns**, so the calculation frequency is **436.862MHz**.

Considering we use shift registers which takes a few clocks, the total time from the input to output is **24.017ns**, so the final calculation frequency is **41.637MHz**.

The calculation frequency is higher than the clock frequency (10MHz), so it fulfill the timing constraint.

Design Modification



We change the bit of input of CSA above from 11 bits to 15 bits.