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LAB Assignment 3 - Multiplicative Divider

- **Simulation Results – Multiplier**

  Test Bench:

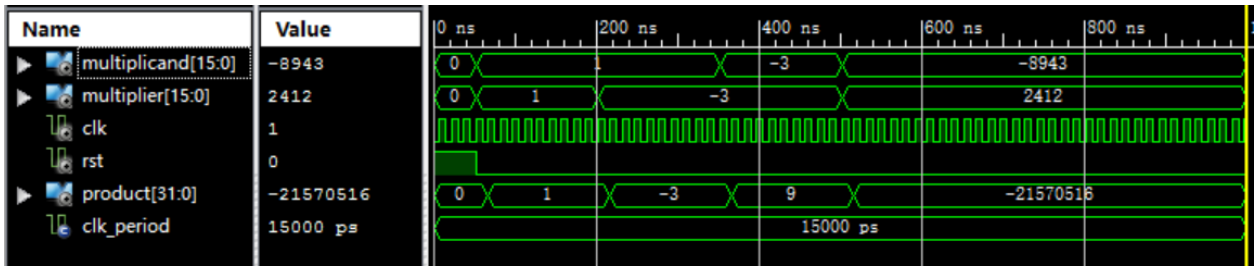
  1x1=1

  1x-3=-3

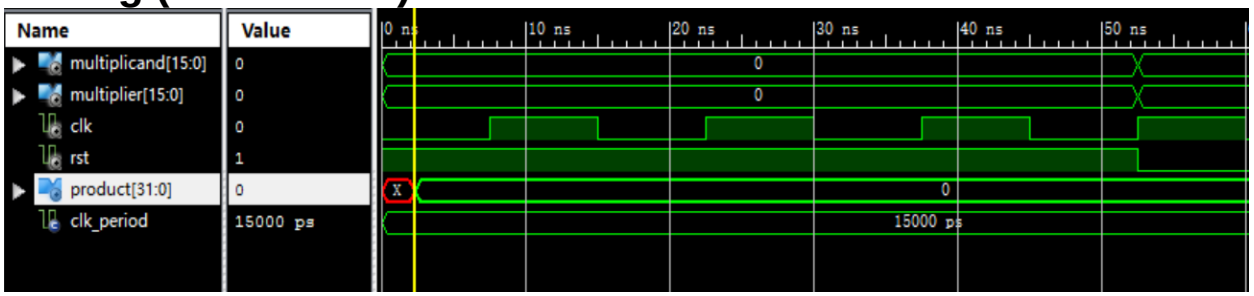
  -3x-3=9

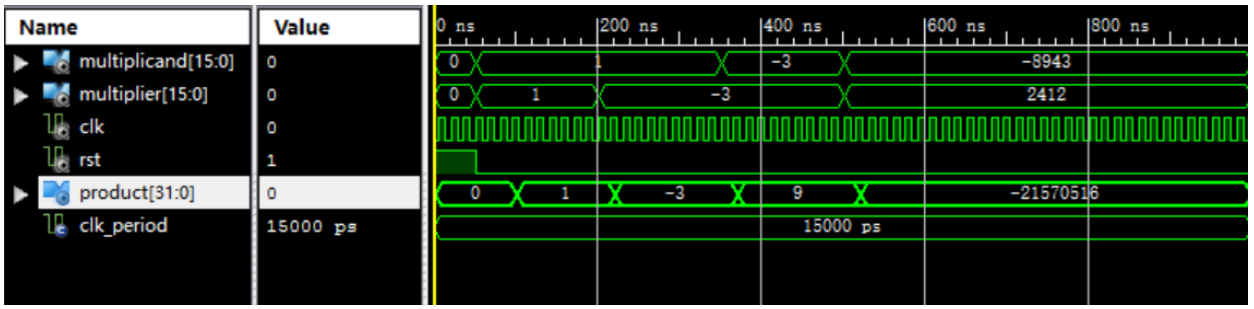
  -8943x2412 = -21570516

  - **Behavior**



  - **Timing (Post-Route)**





Simulation Results – Divider

Test Bench:

Run in 6 cycles to get the final result of quotient

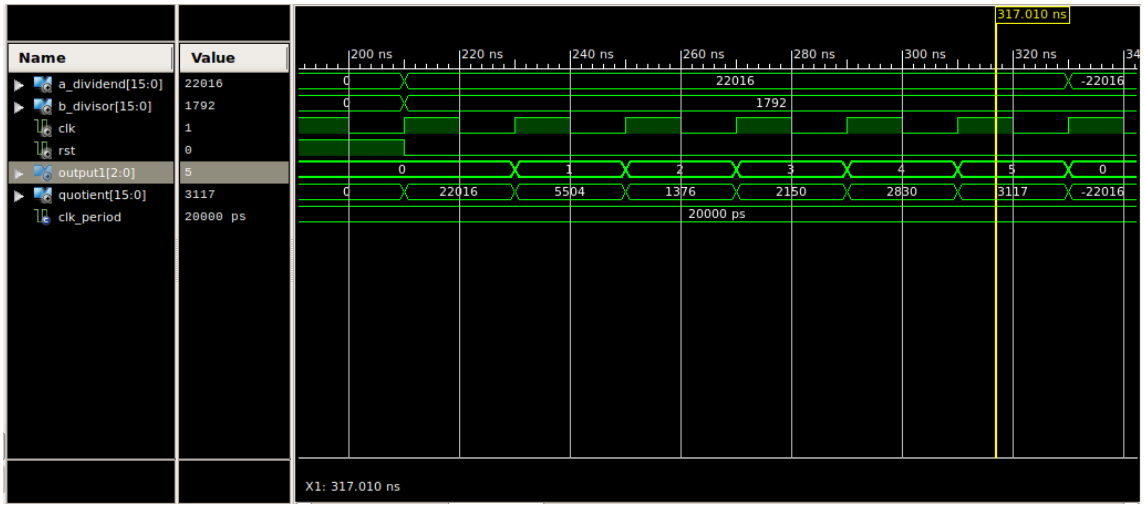
Test1:

Dividend = 0101011000000000_2 = 86_{10}

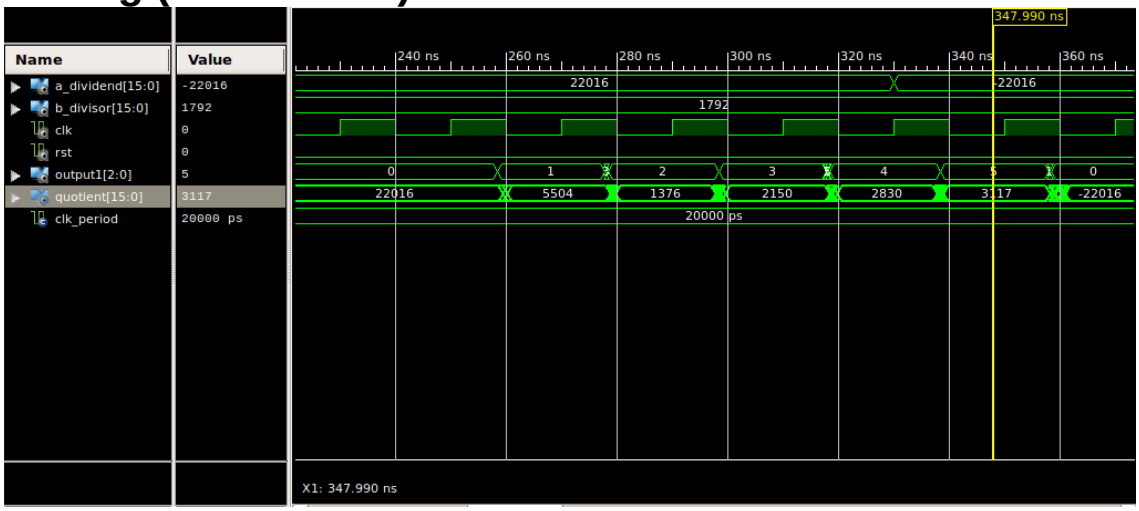
Divisor = 0000011100000000_2 = 7_{10}

Quotient $\cong 12.175_{10}$

- **Behavior**



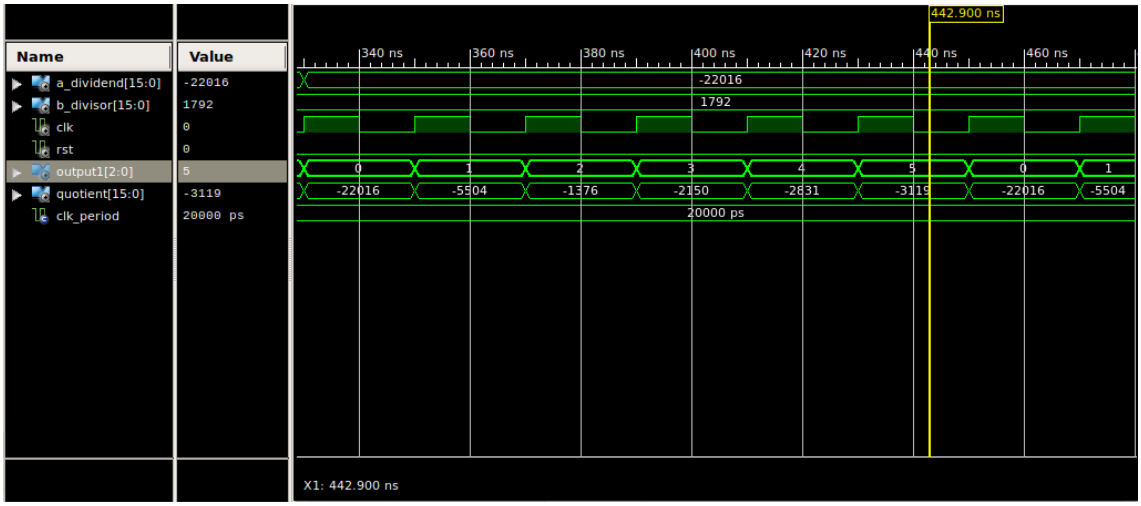
- **Timing (Post-Route)**



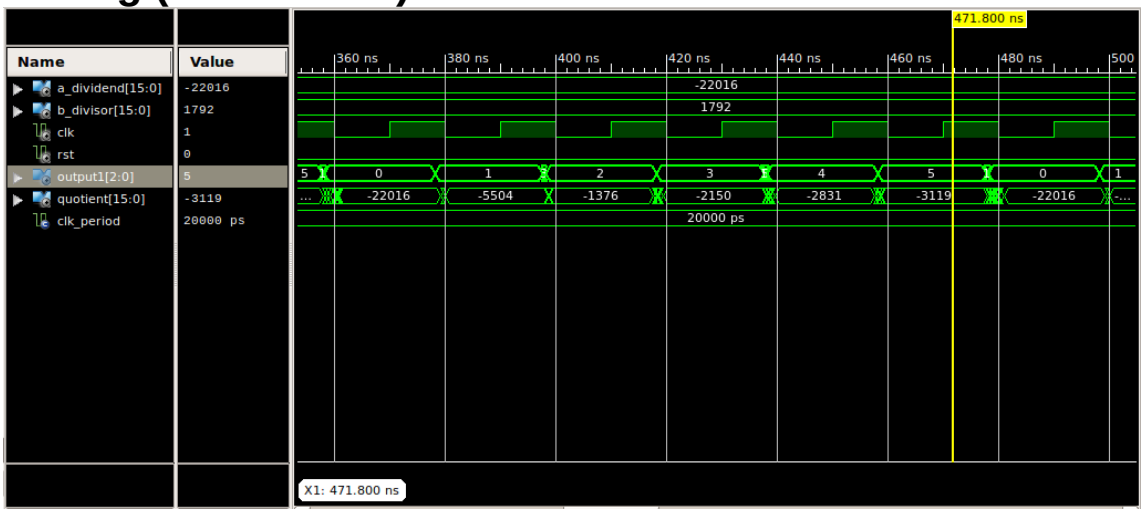
Test2:

Dividend = $1010101000000000_2 = -86_{10}$
Divisor = $0000011100000000_2 = 7_{10}$
Quotient $\cong -12.183_{10}$

- **Behavior**

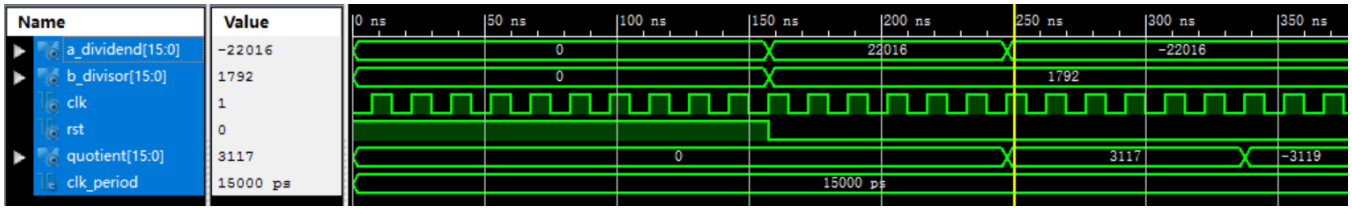


- **Timing (Post-Route)**

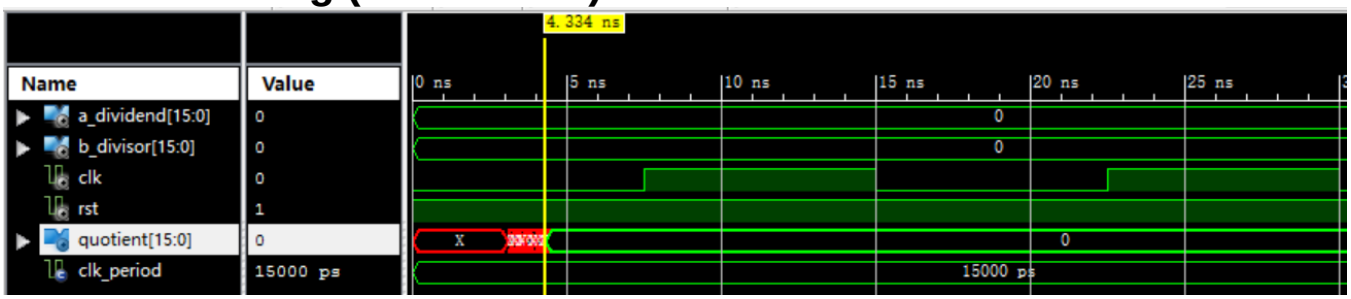


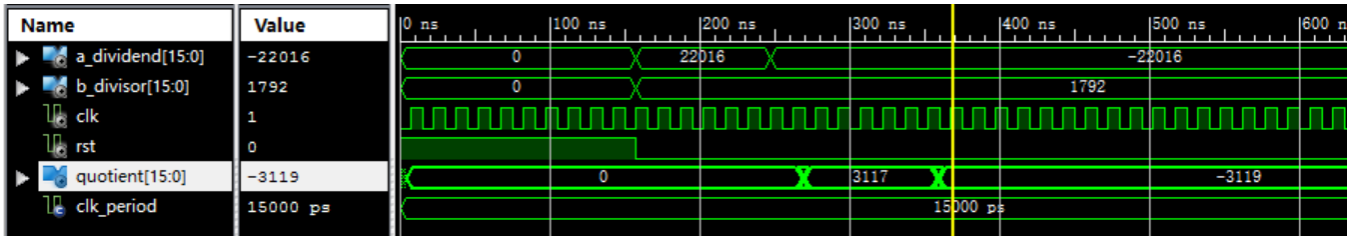
Final version without showing calculate state (output1) and intermediate values.

- **Behavior**



- Timing (Post-Route)





- **Frequency analysis:**

```
Timing Summary:
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Speed Grade: -5

   Minimum period: 14.839ns (Maximum Frequency: 67.392MHz)
   Minimum input arrival time before clock: 16.197ns
   Maximum output required time after clock: 7.603ns
   Maximum combinational path delay: 6.353ns

Timing Detail:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 14.839ns (frequency: 67.392MHz)
  Total number of paths / destination ports: 4200400 / 40
-------------------------------------------------------------------------
Delay:               14.839ns (Levels of Logic = 16)
  Source:            control/output_2 (FF)
  Destination:       nMultif/product_23 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: control/output_2 to nMultif/product_23
                                Gate     Net
```

According to the report of synthesis, the critical path delay is 14.839ns and the related frequency is 67.392MHz (Maximum Frequency)

The total time from the input to output is 7.603ns, so the final calculation frequency is 131.52MHz.

Conclusion:

The division result of behavior and post-route simulation is correct, however we find out that our execution time of post-route is around 10 to 15 mins which confused us.

Besides, as our critical path delay is 14.839, the value of clk in our simulation need to be at least 15ns.