Design note and assumptions

- Logic states and switches are included only for simulation purpose.
- This is not a bidirectional port design. Separate 8-bit port used for inputs and 16-bit port used for output
- This is a level trigger design
- Assume gates ics' are ideal and there are no gate delays, propagation delays.
- Assume there are no noise voltages and there are no intermediate states other than logic 1 and logic 0.

b) Write a simple program in C to read a value from and write a value to your interface

```c
#include <stdio.h>
#include <unistd.h>
#include <sys/io.h>
#include <asm/io.h>

#define ADDR 0x210 //base address from the address lines

void main(){
    //check for port access
    if (ioperm(ADDR, 1, 1)){
        fprintf(stderr, "Access denied to %x\n", ADDR),
        exit(1);
    }

    //write operation
    unsigned int value = 270;
    unsigned char lower_byte = value;
    unsigned char higher_byte = value >> 8;
    outb(lower_byte, ADDR);
    outb(higher_byte, ADDR + 1);

    // read operation
    unsigned char byte_read = inb(ADDR);
    printf("%lu", byte_read);

}
```

c) Briefly explain the importance of using nIOW, nIOR, AENs line in an ISA bus based interface design.

The main purpose of having nIOW, nIOR, AENs signals are to work them as control signals of the interface. nIOW, nIOR signals are used to set the transaction process between read and write expected to be done.

There are some advantages of having active low signals for read, write signals. It is easier to pull down the signal. Therefore, having active low signals would much easier for the designer. Also active low always helps eliminate indeterminate states due to improper supply voltages.

Sometimes the DAM controller mastering the ISA bus in order to complete data transferring between peripherals and memory. At that time the CPU cannot use the bus to do IO operations. The AEN is used by the controlling signals to indicate which is the master of the bus at the particular instance.

If AEN=1 DMA is the bus master.