## <https://www.linkedin.com/in/markamcd> [mark@bluelakeconsultinginc.com](mailto:mark@bluelakeconsultinginc.com?subject=Your%20resume)

B.Sc. Physics, Honors

University of Victoria

Graduate studies Particle Physics UVic at Stanford

Physicist, Experimental Group C Stanford Linear Accelerator

### Deep Learning – a personal history

1993 Analog and Digital Neural Networks for Pattern Recognition.

1994 Adaptive Logic Network (ALN), a Learning Boolean Tree.

1994 *Pattern Recognition in a Tracking Chamber using Adaptive Tree Networks (ALNs)****,*** ByMark Alden McDougald, University of Victoria at Stanford. Self Learning and Classification, 1994. 14pp.

1995 A Digital Neural Network for OCR. Property address recognition in random street images.

1995 Adaptive Logic Network in hardware for sub s ion chamber self triggering on cosmic rays.

1995 Triple Transform Facial imprinting.

1995 Neural Classification of Facial imprints as a spectral decomposition.

1995 Distributed Computing in an IBM networked cluster.

1995 Adaptive Logic Network for Breast Tumor Classification from Mammograms.

2002 A Neural Algorithm with gate level Hardware Acceleration for Low Latency Trading.

2005 Neural Algorithms in DSP and GPU - pipelining and vectorizing performance.

2013 A Neural Algorithm with Hardware Acceleration for Low Latency Trading revisited in a SoC.

2014 NLP and a neural engine for context recognition.

2015 Conversational NLP. Interaction with an expert system.

### Mathematics

Multivariate Calculus, Vector Calculus, Linear Algebra, Complex Variables, Time Series Analysis, Ordinary Differential Equations, Partial Differential Equations, Real Analysis, Complex Analysis, Statistical Analysis, Mathematics for Physics, Theory of Calculus, Multivariate modeling.

### Machine Learning

Deep neural models: 22 years in Machine Learning, Natural Language Processing, Sparse Distributed Memory, Deep Neural Learning, Associative Memory, Reinforcement. Practical Applications executed.

**Papers**: Adaptive Logic methods in Pattern Recognition, A Neural Algorithm with Hardware Acceleration for Low Latency Trading.

**Studies**: Time Series Analysis and Stock Price Prediction, High Energy Physics Particle Tracking and Identification, Mammogram Image Analysis and Classification.

### Computing Science

C, C++, Python Languages, Computer Architecture, Software Architecture, Numerical Analysis, Assembly and Machine Language, TCP/IP, UDP. Strong OO and coding skills in popular languages: C#, C, C++ , intrinsics and assembly language

### Performance

Heterogenous Distributed Computing, Symmetric Multicpu, Asymmetric Multicpu, Threading Optimization. Algorithm optimization for performance in SIMD and VLIW architectures. NEON, Altivec, SSEx, MMX, TI DSP, Gpu, FPGA.

### Algorithms

Novel and complex algorithm design, modeling and integration – including DSP prototypes in software and programmable hardware (hough, radar, fft, fir, bpn, gnn, and aln). Algorithm partitioning for asymmetric multiple cpu and dsp architectures such as TI OMAP, DaVinci. Spectral analysis and spectral deconvolution; time series analysis

#### Education

***BSc. Physics 1993*** University of Victoria, with honors.

***Graduate Work in Particle Physics 1993-1995*** University of Victoria (at Stanford Linear Accelerator).

#### Security Clearances

***Secret*** Energy ***DOE***, Defense ***DOD***, Treasury ***BEP***.

### Inventions

***Finance*** Adaptive Neural Network for classification and optimal pricing of equities. Neural fabric can be synthesized in verilog and programmed into an FPGA. Prototyped in FPGA hardware.

***Metrology*** Invented an innovative electro-optical metrological method of sub-m measurement of the diameter and surface quality of fine wire products used in ionizing gas tracking devices. Prototype developed.

***Cytometry*** Invented a laser optical and analog electronic feedback loop to control the inter-drop spacing during drop delay flow cytometry. Full Mathcad models of Fourier Optics, detector geometry, and ASP and DSP algorithms. Prototyped optical system.

***Mammography*** A neural adaptive pattern recognition algorithm to identify and classify micro-calcification structures in mammograms. Full Mathcad model. Prototyped against UCSF mammogram database.

***Optical Character Recognition*** A Digital Neural Network for OCR. Algorithm to identify and classify character and numeric structures in common scenes. Full Mathcad model. Full verilog translation for hardware.

### Expertise

***Hardware*** Microprocessor and bus design. FPGA design. Vector units.

***Software*** Verilog, C/C++/C#, Java.

***Operating Systems*** Windows, Linux, VxWorks, QNX, VMS, Solaris, SunOS, AIX, MacOS, Rtems.

***Architectures*** ARM, x86, MIPS, Sparc, Not limited.

### Systems

>20 years of systems design experience with a proven and innovative track record. Architectural design studies – requirements and functional analysis, cost/performance tradeoff, COTS and custom integration, and general strategies for failure avoidance and recovery from upset. 20 years experience with popular RTOSs, such as VxWorks, and the compilers, profilers, and emulators in their tool chains; rock solid understanding of the toughest problems of synchronization, interrupt handling, context switching and reentrancy. QNX, VxWorks, Linux, and Windows bsps, drivers and applications. System verification, hardware bringup, RTOS board support (BSPs), custom driver design, compiler internals, software runtime error checking, and diagnostics for POST and runtime.

Windows device drivers with custom memory allocation handling for extremely high performance, and multi cpu and multi-threaded architecture. Programmable logic, FPGA system design. Altera, Xilinx. Soft and hard processors. x86 BIOS for embedded medical instrumentation. EFI/UEFI implementations. Knowledge of popular bus and microprocessor architectures; programmable digital design. Deeply embedded multi-processor experience; distributed computing and OS architectures. Expert in internet communication and security protocols from MAC through application layers. Extensive control, triggering, and embedded data acquisition for high energy physics and medicine. Extensive physical modeling and prototyping of complex detector and data acquisition systems.

### Corporate Engagements

* **Machine Learning**
  + Stanford Linear Accelerator Center https://media.licdn.com/media/p/5/000/1fe/341/3930b5b.png
  + Dell EMC https://media.licdn.com/media/AAEAAQAAAAAAAAiLAAAAJDc3ZjJiODM3LTNjZWMtNGQwYi1hNTFjLWRhN2FjNTExODExYg.png
  + BLCI
* **Satellite systems**
  + NASA https://media.licdn.com/media/p/2/000/01c/0a9/2ca5211.png, Stanfordhttps://media.licdn.com/media/AAEAAQAAAAAAAAdcAAAAJDg1NzcyYjU1LTY1OTctNDk4Ny1iODFkLWJlNjE2Yjc0NzhiNA.png - FERMI space telescope
  + Skybox Imaging https://media.licdn.com/media/AAEAAQAAAAAAAAZjAAAAJDk0YTAwYzFjLTBkZjEtNDc4MS04NDE1LTlmMjJjZWU1MWI4OA.png
* **Video**
  + RGB Networks https://media.licdn.com/media/p/2/000/022/249/208929e.png
* **Interactive Television, Set Top Box**
  + Liberate Technologies
  + Microsoft Corporation https://media.licdn.com/media/AAEAAQAAAAAAAAmJAAAAJDE5ZTBlNDYxLTlhZTItNDA1MS04MjFiLTJjNDRhYmYwMWQyOQ.png
* **Robotics**
  + Jibo https://media.licdn.com/media/AAEAAQAAAAAAAAH_AAAAJDg5YTRhYTdlLWJmOTctNGEzNS1iNTEwLTY2YzRmMzNiOWQ0Zg.png
* **Metro Edge Aggregation - Switching and Routing - Final Mile fiber - FTTH, (G)EPON**
  + GigaLabs
  + Cisco Systems https://media.licdn.com/media/AAEAAQAAAAAAAAl_AAAAJDZjNGQ5YzMyLWJiMTYtNDNjNS1hNDI4LWFkZjAxOTdmZmI3MQ.png
  + Mayan Networks
  + Cosine Communications
  + Softcom Microsystems
  + McData
  + Brocade https://media.licdn.com/media/AAEAAQAAAAAAAAInAAAAJDU5OWVhN2ZhLWQyMWEtNDYxMC05YjUwLTE4Yjk3MTc5MmJmMA.png
  + Salira Systems https://media.licdn.com/media/p/3/000/01b/1ec/37d13ae.png
* **Cryptography, Security, Firewalling**
  + SonicWall https://media.licdn.com/media/AAEAAQAAAAAAAAj1AAAAJDU5ODEwYmEzLTY5NzItNDczYS1hNmIzLTcwMTEwYjE0OGU3Mg.png
  + Cabot Security Materials https://media.licdn.com/media/p/6/000/218/10d/27f4b31.png
* **Medical, Bioscience**
  + Sony Life Electronics https://media.licdn.com/media/p/7/005/03b/2c1/29777f5.png
  + Becton Dickenson Biosciences https://media.licdn.com/media/AAEAAQAAAAAAAATQAAAAJDMxM2E4ODllLTRiYTUtNDBiYy04YmMyLTU5YjY1YzVkZDViZQ.png
  + Systemix
  + NovaBay Pharmaceuticals https://media.licdn.com/media/p/1/000/0a0/0ed/27a2e8d.png

#### Engagement History

**President and Principal Engineer**

**Blue Lake Consulting Inc., Gilroy, CA., 2001- Present.**  Owner, president, and principal engineer of Blue Lake Consulting Incorporated. Blue Lake Consulting Inc. was incorporated in 1/ 2001 to provide system and software consulting services for a wide client base, including Silicon Valley laboratories and companies. An outline of services provided to date follow, roughly in reverse chronological order.

**SLAC National Accelerator Laboratory , Stanford, CA.**

Jan 2017 – July 2017

Design and development for LCLS-II experiment dataflow and processing. LCLS-II is a free electron laser capable of 1MHz rep rates. The LCLS-II data rate in 2019 will approach 1TB per second. Architectural review and recommendation. Large scale heterogenous parallel processing. (Py, C, C++, Verilog)

**Microsoft Corporation, Mountain View, CA.**

March 2016 – December 2016

SoC verification for Xbox cpu. Simulation and Emulation. Verilog and C programming for verification. Scripting for verification purposes. Pre and Post silicon validation (Py, Yaml, json, C, C++, Verilog)

**Dell Inc., Santa Clara, CA.**

June 2015 – December 2016

Natural Language Processing and Machine Learning. Methods in AI for NLP. Modeling of Neural Dynamics and mammalian cerebral organization. Aural and vision system prototyping. Speech tagging and categorization. Neural models for "deep" learning. Conversational NLP (Py). Sparse Distributed Memory.

**Jibo Inc., San Francisco, CA.**

September 2014 – May 2015 (9 months)

Collaborative partner in robotic engineering. Language processing. Operating system and platform software, linux device drivers for video and audio. Camera and microphone array bringup. Audio and vision system prototyping and verification (C, C++). Device driver (C) and hardware abstraction layers. Embedded board architecture and design. System verification.

**PeerNova, San Jose, CA.**

April 2014 – June 2014 (3 months)

Linux kernel configuration and linux kernel drivers for PetaHash, a 1st generation bitcoin mining and secure transaction computing platform. Design verification.

**Sony Life Electronics, San Jose, CA.**

November 2012 – September 2013 (11 months)

Architecture modifications for research flow cytometer platforms and cell sorters. Hardware (Verilog), software (C#) and firmware (C) optimization. Altera SOC FPGA data acquisition (C, C++) and windows .NET control and display software (C#). NIOS II soft processor and iniche ethernet stack modifications for cytometer control. Ethernet triple speed device driver (C). Embedded board architecture and design. Whole system verification.

**Broadcom, Sunnyvale, CA.**

June 2012 – November 2012 (6 months)

Firmware (C++, C) development for mobile device SOC ASIC subsystem verification. Stress testing on emulator and test board architectures using ThreadX OS and Android. System verification.

**Cabot Security Materials Inc, Mountain View, CA.**

April 2011 – October 2012 (1 year 7 months)

Architect and specify high speed "classification" system for Raman Spectroscopy. Multi parametric fitting of spectroscopic data. Simulation and implementation. Rapid prototyping. Configuration of QNX kernel and bsp. Full device driver development (C++, C). Embedded architecture and system partitioning and specification. Threaded realtime multi cpu data acquisition (C++) and processing application (C++, C). SOAP over Ethernet to PC gui application (C++, C#) for display of waveform and algorithm data for verification and configuration. Port to multiple platforms: Android, Linux, QNX.

**Becton Dickinson Biosciences, San Jose, CA.**

March 2007 – August 2010 (3 years 6 months)

Real time operating system and data application support (C++, C, C#) for flow cytometer products. x86 BIOS for embedded medical instrumentation. EFI/UEFI port to instrument platform to help with PCIe race condition on boot. VxWorks real time operating system port (board support) for FACS%CD4 project; included 3 bsps supporting variations in architecture. System debug and problem resolution for FACSCantoII flow cytometer product data acquisition. VxWorks board support and application port for VME based FACSAria flow cytometer and cell sorting product.

FACS Array cytometer product redesign of digital electronics. New TMS320 dsp processor and Ethernet device, and update of software OS and support for TMS320 dsp processor including optimization of boot code and ethernet device driver (TI asm, C++, C, C#). Throughput increased by 3 times over older design due mostly to software optimization. Zero defect release to production.

New cytometer design as a member of a multi-disciplined team of engineers developing a new generation of laboratory and portable flow cytometers. Translation of operational requirements to hardware and firmware specification to meet data throughput. Algorithm manipulation for mathematical compensation of multi-channel data path using vectorizing SIMD hardware (SSE, C, C#). Specification and implementation of data acquisition subsystem. Windows XPe driver and application code for data acquisition system (C, C#). Full diagnostic suites in .NET and WPF, including three applications and firmware (C++, C, C#).

**NovaBay Pharmaceuticals Inc, Emeryville, CA.**

Algorithm and firmware design and implementation for a micro controlled contact lens cleaning device (C, TI asm).

**Skybox Imaging Inc, Mountain View, CA.**

April 2011 – December 2011 (9 months)

Xilinx Virtex-6 FPGA design and programming for space based earth imaging satellite using camera link data acquisition and JPEG2000 compression. MicroBlaze soft ip cpu for communication with satellite control processor and for control of image processing stream (Verilog, C). Compact flash ip and software driver and control (C). Simulation and implementation. Configuration of Xilkernel multi threaded kernel. Command line interface for system (C).

**RGB Networks, Sunnyvale, CA.**

December 2010 – May 2011 (6 months)

Hardware bringup, diagnostics and verification (C++, C). Network and video hardware for stream grooming. CentOS Linux kernel and application work for support of NPM2 and AMP products for the current video processing product line.

**Stanford Linear Accelerator Center, Stanford, CA.**

April 2008 – November 2008 (8 months)

Control system development for MARX power delivery system for the International Linear Collider (ILC). RTEMS board support and port for Arcturus 5282 Coldfire processor. EPICS based monitoring and control. Tcl/Tk windowing GUI for human interface to control and monitoring.

**McData Corporation and Brocade, Santa Clara, CA.**

Diagnostics and verification for Eclipse 3610 SAN switch and extender product. CLI and VxWorks rtos shell dynamics for bringup and manufacturing diagnostics. FPGA verification for DioneIV, BigMac, and Whopper system control, framer, encryption, and compression FPGAs (C).

**Stanford Linear Accelerator Center, Stanford, CA.**

April 2002 – July 2005 (3 years 4 months)

Defined system design for a satellite payload instrument simulator for GLAST, the Gamma Ray Large Area Space Telescope, now the FERMI space telescope. Specified COTS hardware platform and OS. Authored firmware for instrument (AHDL, VHDL): VxWorks and Linux BSPs and drivers (C) for network, disks, and custom FPGAs. Brought up custom hardware and integrated firmware. Designed and built several test stands for GLAST hardware and firmware verification (C, C++, Verilog).

**Salira Systems Inc., Santa Clara, CA.**

July 2006 – December 2006 (6 months)

Hardware bringup for 3520 platform chassis, ATCA based GEPON switch. VxWorks Board Support Package (BSP) for 3520 command card, MPC8270 cpu, Broadcom 5696 switch, Teknovis TK3921 PON interface (x7), I2C, flash, rtc, and all support subsystems. Muxed software interrupt layer for linecard operation (VxWorks) (C). Consulted on board level problems on other platforms. Persistent exception handling for debugging system instability. Ongoing consulting on all system issues.

**H.L. Yoh Company and SonicWall Inc., Sunnyvale, CA.**

July 2001 – January 2002 (1 year 6 months)

Modified compilers to provide custom runtime error checking. Authored VxWorks Board Support Package (BSP) for, and ported firewall applications to XPRS2 platform – Toshiba SOC (C). Developed drivers for cryptographic hardware for XPRS2 and ProVx platforms (C). Consulted on board level problems on other platforms.

**Stanford Linear Accelerator Center, Stanford, CA.**

Winter 1998

Engineered and delivered a flexible boot system for an i960RP target embedded in VME DAQ Readout Module (C++). Booting was under the control of a host embedded PowerPC processor running VxWorks and included dynamic image selection. i960RP processor setup and generation of custom runtime images – both debug and optimized (C, C++, PPC asm, i960 asm).

**Independent Consultant, Systems and Software**

**H.L. Yoh Company, Silicon Valley, CA., 1998-2001.** Provided independent system and software consulting services for several Silicon Valley companies. Detailed services provided for each company follows.

**SonicWall Inc., Sunnyvale, CA.**

2000-2001

Brought up hardware and developed boot code and drivers for XPRS2 firewall product. Participated in design and architecture of XPRS2 firewall product. Ported VxWorks BSP and proprietary firewall code base to XPRS2 platform. Ported ‘Make’ environment and image handling tools and integrated into company build process. Developed drivers for cryptographic hardware for XPRS2 and ProVx platforms. Consulted on board level problems on other platforms.

**Liberate Technologies, San Carlos, CA.**

1999

Modified software system services layer of proprietary code base to support different application and driver subsystem layers (C). Consulted on VxWorks BSP for Philips platform (C).

**Mayan Networks, Sunnyvale, CA.**

1998

Developed firmware for MPX1 product line (C++, C). Brought up MPX1 hardware. Ported VxWorks to MPX1 platform. Supported hardware group in board verification. Designed and implemented Operating System Services layer. Analyzed and optimized performance of CPCI inter-card communication path. Analyzed system for the purpose of design verification. Designed power on diagnostics.

**Cosine Communications, Belmont, CA.**

1998

Designed multi-processor boot sequence and POST for IPSX product line (C). Developed drivers for proprietary ring topology serial bus inter-card communication and management path (C). Prepared test drivers for custom FPGA loads used by manufacturing department for assembly verification (C).

**Cisco Systems, San Jose, CA.**

1999

Brought up hardware for POPEYE2, a 45 Gbit Point Of Presence internet switch. Modified VxWorks driver and proprietary IPC layers for cell bus inter-card communication path. Prepared test routines for verification of inter-card communication (C).

**Softcom Microsystems, Fremont, CA.**

1998

Designed and implemented power-on, manufacturing, and runtime diagnostic suite for the GigaBlade product (C). The GigaBlade is a PCI based card running VxWorks, with dual OC-3/OC-12 and 1000BaseT Ethernet interfaces driven by an ATM packet processor – the SoftcomEngine.

**Senior Software Engineer**

**GigaLabs Inc., Sunnyvale, CA., 1997-1998.** Authored VxWorks RTOS BSP for all baseboards in a 15 Gbit SAN switch product. Wrote low-level drivers for 10/100 Ethernet and SCSI (C). Worked on topics in management, redundancy, and fault tolerance. Installed and managed both Sourcesafe and VxWorks Tornado for 10 developers.

**Consulting Systems Engineer**

**Systemix Inc., Palo Alto, CA., 1997.** Completed a design study and proposal to use a personally invented technique for controlling the inter-drop spacing during drop delay flow cytometry. The full Mathcad model of optical diffraction theory, detector geometry, and signal processing algorithms provided a linear estimator of inter-drop spacing suitable for use in an analog or digital feedback loop.

**Engineering Physicist**

**Stanford Linear Accelerator Center, Stanford, CA., 1995-1997.** Co-designed and prototyped a 200+ processor data acquisition system for the BABAR high energy physics experiment. Played a strong role in hardware commissioning. Designed microprocessor subassemblies. Authored data flow and sub-detector data acquisition software in C++, C, and Assembly (under VxWorks). Prototyped distributed computing architectures. Modeled ionizing gas detector physics. Supervised technical staff, graduate, and undergraduate students. Undertook independent research into neural methods for pattern recognition as applied to detection and classification of microcalcifications in imaged mammograms, and processing of high energy charged particle trajectories.

**Physicist**

**University of Victoria, Stanford, CA., 1993-1995.** Modeled ionizing gas detectors, or drift chambers, for the verification of the BABAR detector design. Developed code in C++ and C to model the digitization and signal processing algorithms operating on detector outputs. Optimized detector elements for maximal resolution of measurement. Authored portions of the BABAR technical design report and Letter of Intent for the US DOE. Prototyped ionizing gas particle detector subsystems. Developed software in C++, C for prototype data acquisition through custom electronics (VxWorks). Supervised graduate, and undergraduate students. Undertook independent research into pattern recognition as applied to particle detection and tracking.

#### Memberships and Awards

***SLAC Award*** Stanford Linear Accelerator Center Experimental Group C Top Achiever Award, 1996.

***APS*** Member, The American Physical Society.

***NSERC (twice)*** Natural Sciences and Engineering Research Council monetary awards.

***Don Ingham Memorial Scholarship*** University of Victoria, for scholastic achievement in Astronomy.

#### Publications and Documents

***GLAST ISIM (FERMI FES) System Specification,*** By Mark McDougald, Blue Lake Consulting Inc. GLAST Internal document prepared partially under DOE contract 515-C-584, Nov 2002. 55pp.

***The BABAR Detector,*** By BABAR Collaboration (B. Aubert et al.). SLAC-PUB-8569, BABAR-PUB-01-08, Apr 2001. 119pp., Published in **Nucl.Instrum.Meth.A479:1-116,2002.**

***System Faults,*** ByMark McDougald. A design analysis of the bus architecture of the MPX Metro Edge Aggregator., Mayan Networks internal confidential document. 1999. 21pp.

***The BABAR Drift Chamber,*** By BABAR Drift Chamber Collaboration (G. Sciolla et al.). SLAC-PUB-7779, May 1998. 8pp., Published in **Nucl.Instrum.Meth.A419:310-314,1998.**

***Dataflow Reference Manual,*** By(R. Hamilton et al.). BABAR-Note-387, May 98.

***The BABAR Drift Chamber Project,*** By (A. Boucham et al.). Prepared for 7th Pisa Meeting on Advanced Detectors: Frontier Detectors for Frontier Physics, La Biodola, Isola d'Elba, Italy, 25-31 May 1997. Published in **Nucl.Instrum.Meth.A409:46-52,1998.**

***An optical feedback system for drop delay flow cytometry ,*** By Mark McDougald. An initial study prepared for Systemix Inc., Mar 1997. 4pp.

***BABAR Drift Gas Gain,*** ByMark Alden McDougald. TNDC-Note-51, Nov 96.

***BABAR Technical Design Report,*** By BABAR Collaboration (D. Boutigny et al.). SLAC-R-0457, SLAC-R-457, SLAC-0457, SLAC-457, SLAC-R-95-457, Mar 1995. 618pp. For the US DOE.

***Letter of Intent for the Study of CP Violation and Heavy Flavor Physics at PEP-II,*** By BABAR Collaboration (D. Boutigny et al.). SLAC-0443, SLAC-443, SLAC-R-0443, SLAC-R-443, Jun 1994. 335pp.

***BFAST Computing Recommendations,*** By(D. Aston et al.). SLAC-BABAR-NOTE-118, Nov 1993. 13pp.

***Pattern Recognition in a Tracking Chamber using Adaptive Tree Networks (ALNs),*** ByMark Alden McDougald, University of Victoria. A self learning tracking algorithm, 1994. 14pp.

#### References

Pxxxx Dxxxx, PhD

Physicist

Biomedical entrepreneur

Owner Biodtx

ph:  650-868-3610

Jxxx Txxxxx, PhD:

Physicist

Department Head, Linac Coherent Light Source (LCLS) Data Systems

Manager of Fermi Space Telescope Instrument package

ph: 650-556-xxxx

Jxxxx Cxxx, EE:

CEO Salira Systems, a Hitachi Company (FTTH, EPON technology)

ph: 408-750-7099

Jxxxxxxx Dxxxxx, PhD:

Physicist

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President of the Okinawa Institute of Science and Technology, Graduate University

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Vxxx Lxxx, PhD:

Physicist

Group Leader, Experimental Group C at SLAC

ph: 650-926-xxxx

Mxxx Hxxxxx, EE:

Architect of Data Acquistion for BaBar

Data Acquisition for Fermi Space Telescope

Data Acquisition for Atlas detector at CERN

ph: 650-926 xxxx