Day3-Full Subtractor using Half Subtractor #75daysRTL

Full Subtractor is a combinational circuit that consists of 3 inputs to generate Difference and Borrow unit as output.

Generation of Full Subtractor-

1. **Using Gates based on the Equation-**

   Sum = A xor B xor Cin
   Carry = (A'.B)+(B'.Cin)+(A'.Cin)

   To implement Full Adder using Gates we require **2XOR, 3AND, 2OR, 1NOT gates**.

2. **Using Half Subtractor circuit- (Mostly Used)**

   Half adder is a combinational circuit in which a computer binary subtracts two binary inputs a & b to produce output difference & borrow bit.

   Using Structural Modelling we can produce a full subtractor using half subtractors.

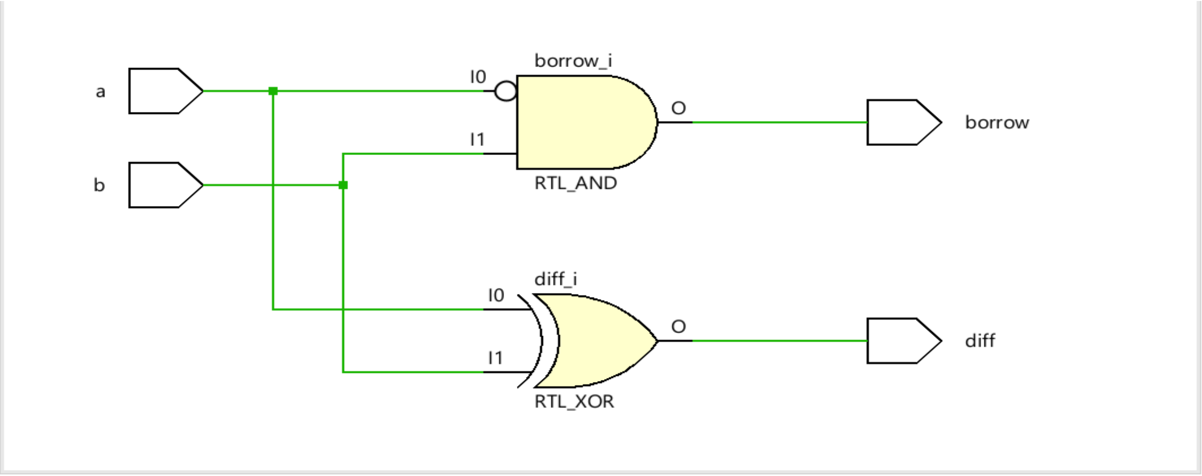
Half Subtractor (Truth Table)-

Input - A	Input - B	Output - Diff	Output - Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Diff = A xor B

Borrow = A' and B

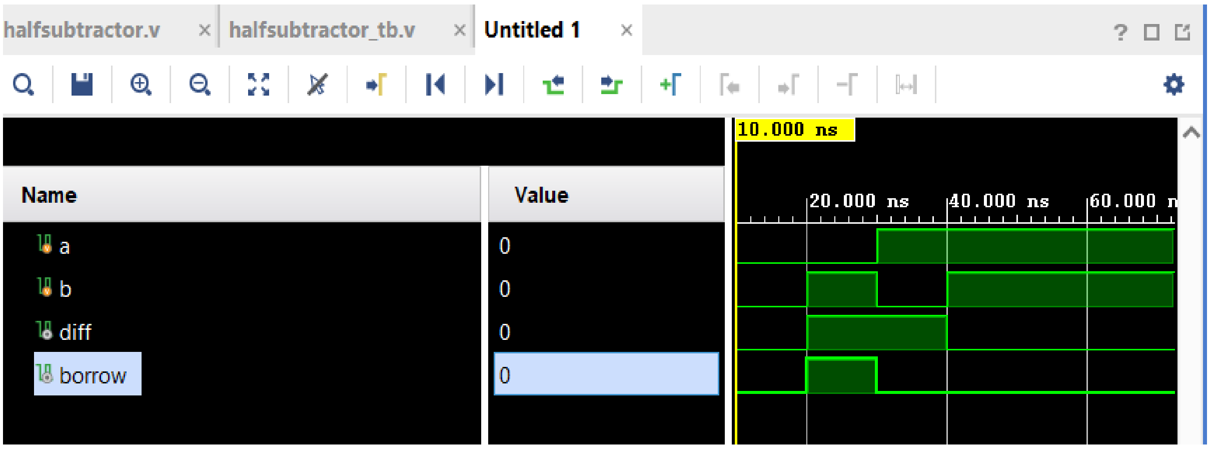
Half Subtractor Schematic View –



Half Subtractor Verilog Code -

```
module halfsubtractor(
    input a, input b, output diff, output borrow
    );
    assign diff=a^b;
    assign borrow=~a&b;
endmodule
module halfsubtractor_tb();
reg a,b;
wire diff,borrow;
halfsubtractor dut(a,b,diff,borrow);
initial begin
#10;
a=0;b=0;
#10;
a=0;b=1;
#10;
a=1;b=0;
#10;
a=1;b=1;
end
endmodule
```

Simulation of Half Subtractor -



Name	Value
a	0
b	0
diff	0
borrow	0

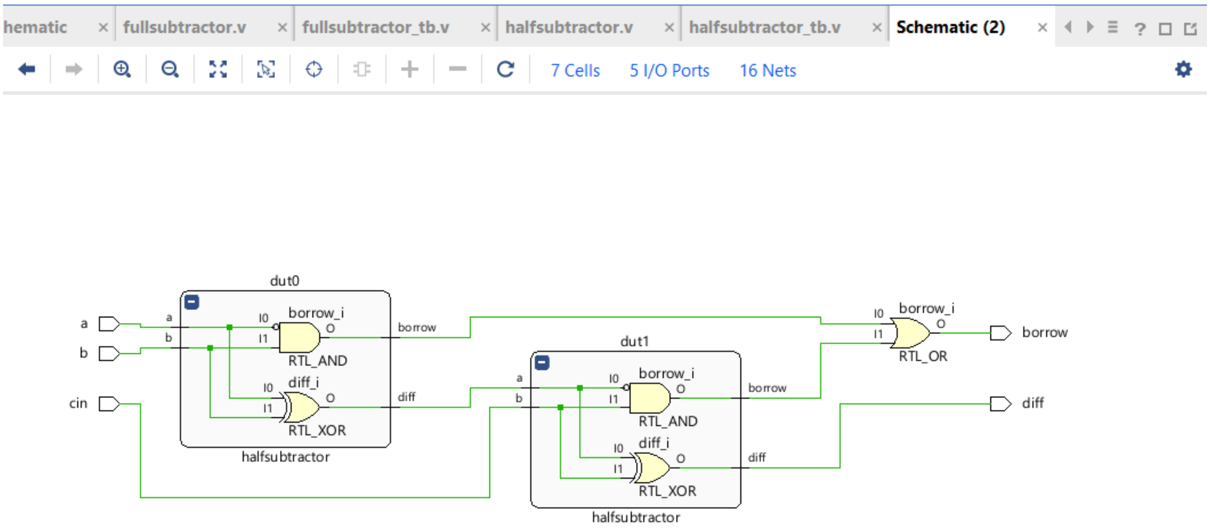
Full Subtractor (Truth Table)-

Input - A	Input - B	Input - Cin	Output - Diff	Output - Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Diff – A xor B xor C

Borrow – (A’.B)+(B’.Cin)+(Cin’.A)

Full Subtractor Schematic View –

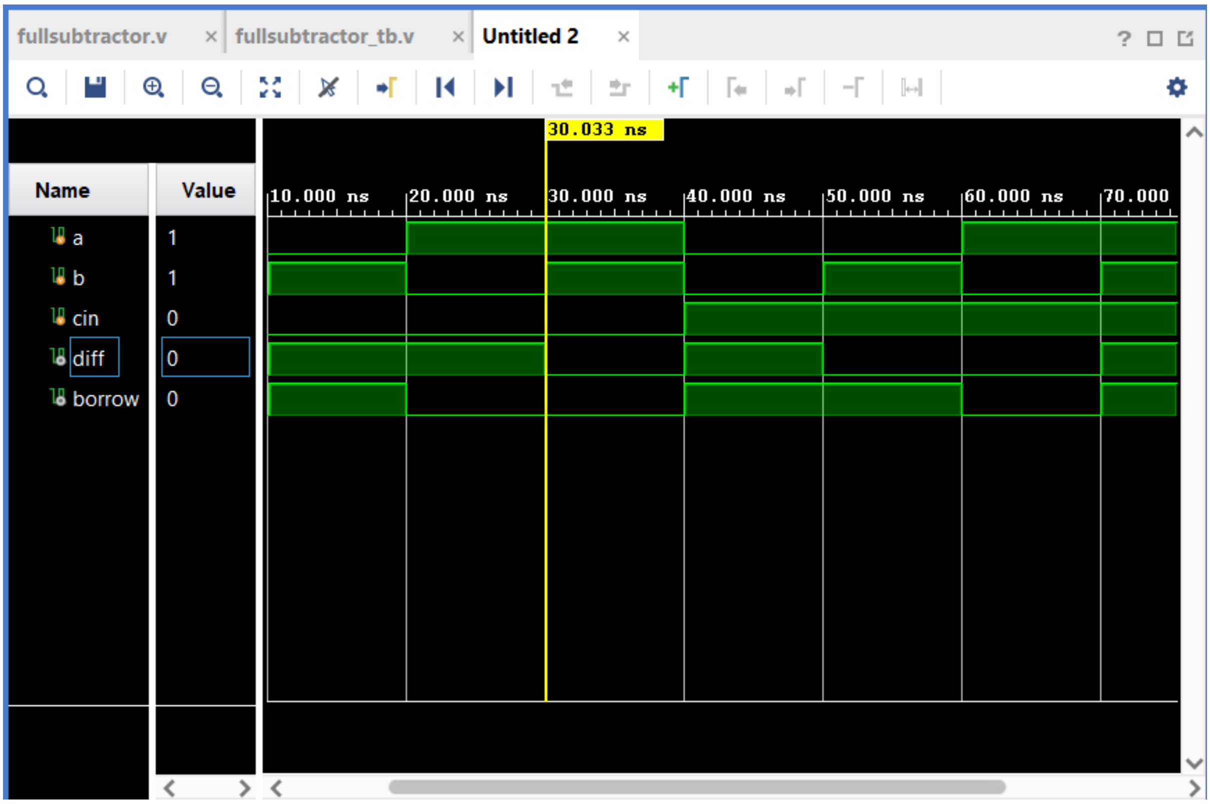


Verilog Code –

```
module fullsubtractor(
    input a, input b, input cin,
    output diff, output borrow
    );
    wire diff_1,borrow_1,borrow_2;

    halfsubtractor dut0(a,b,diff_1,borrow_1);
    halfsubtractor dut1(diff_1,cin,diff,borrow_2);
    assign borrow=borrow_1|borrow_2;
endmodule

module halfsubtractor(
    input a, input b, output diff, output borrow
    );
    assign diff=a^b;
    assign borrow=~a&b;
endmodule

module fullsubtractor_tb();
reg a,b,cin;
wire diff,borrow;

fullsubtractor dut(a,b,cin,diff,borrow);

initial begin
a=0;b=0;cin=0;
#10;
a=0;b=1;cin=0;
#10;
a=1;b=0;cin=0;
#10;
a=1;b=1;cin=0;
#10
a=0;b=0;cin=1;
#10;
a=0;b=1;cin=1;
```

```
#10;
a=1;b=0;cin=1;
#10;
a=1;b=1;cin=1;
#10;
$finish;
end
endmodule
```

Simulation Results –


fullsubtractor.v
fullsubtractor_tb.v
Untitled 2
30.033 ns
Name
Value
a
1
b
1
cin
0
diff
0
borrow
0
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000