Day14- Clock Divider #75daysRTL

A clock divider circuit creates lower-frequency clock signals from an input clock source. The divider circuit counts input clock cycles and drives the output clock low and then high for some number of input clock cycles. where fout = fin / n and "n" is an integer. Frequency dividers are used for both analog and digital applications.

Verilog Code –

```
module clockdivider(input clk,rst,
output reg divby2,divby4,divby8,divby16);
reg [3:0]count=4'b0000;
always@(posedge clk)
begin
if(rst==0)
count=4'b0000;
else
count<=count+1;
divby2<=count[0];
divby4<=count[1];
divby8<=count[2];
divby16<=count[3];
end
endmodule
```

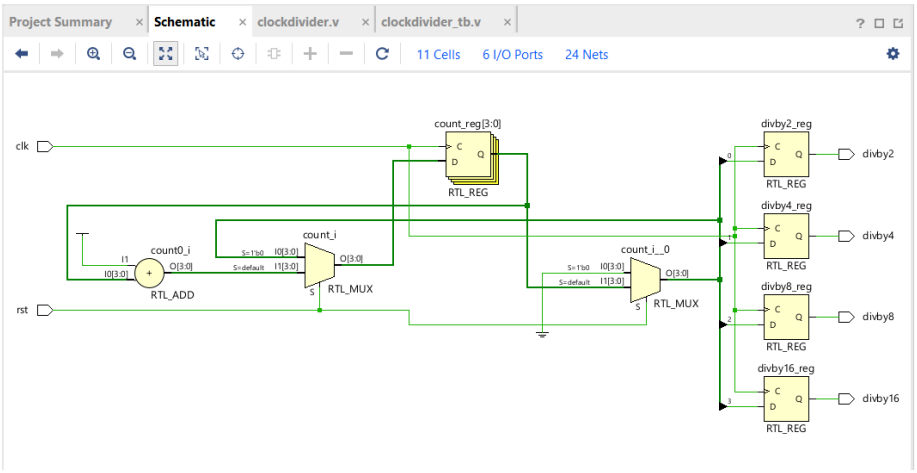
TestBench Code-

```
module clockdivider_tb();
reg clk,rst;
wire divby2,divby4,divby8,divby16;

clockdivider uut(clk,rst,divbu2,divby4,divby8,divby16);
initial begin
clk=0;
rst=0;
#10;
```

```
rst=1;
forever #10 clk =~clk;
#100 $finish;
end
endmodule
```

Schematic View of Clock Divider-



Simulation Result of 3 to 8 Decoder -