Day7-16X1_Mux_using_4X1_Mux #75daysRTL

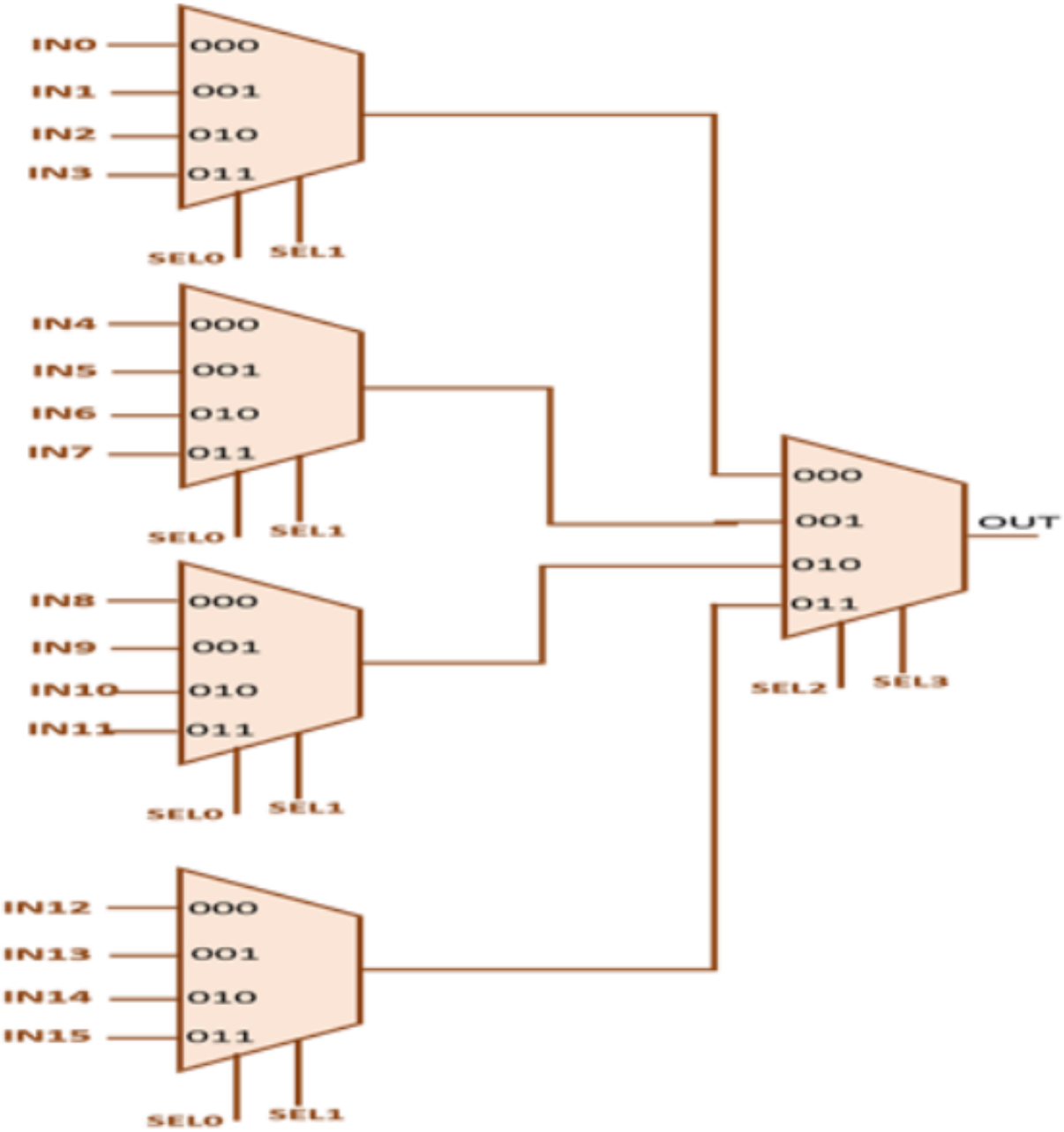
A multiplexer is a data selector device that selects one input from several input lines, depending upon the enabled, select lines, and yields one single output.

A multiplexer of **2^n inputs has n select lines**, which are used to select which input line to send to the output. There is only one output in the multiplexer. We designed a 16x1 Multiplexer where for 16 input lines, 4 select lines and 1 output is selected using 4x1 Multiplexers as instances.

Truth Table (Selection Lines)-

Select-S0	Select – S1	Select – S1	Select – S1	Output Line
0	0	0	0	IN0
0	0	0	1	IN1
0	0	1	0	IN2
0	0	1	1	IN3
0	1	0	0	IN4
0	1	0	1	IN5
0	1	1	0	IN6
0	1	1	1	IN7
1	0	0	0	IN8
1	0	0	1	IN9
1	0	1	0	IN10
1	0	1	1	IN11
1	1	0	0	IN12
1	1	0	1	IN13
1	1	1	0	IN14
1	1	1	1	IN15

Block Diagram –



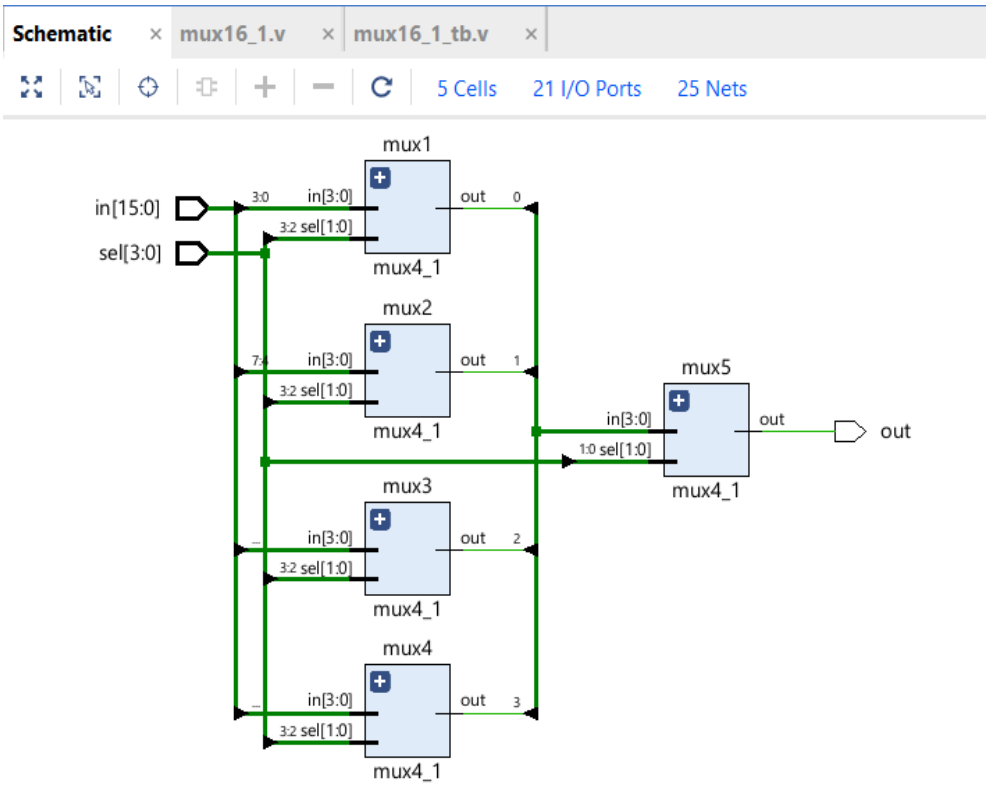
Verilog Code –

```
module mux4_1(in,sel,out);
input [3:0]in;
input [1:0]sel;
output reg out;

always@(in,sel,out)
begin
case(sel)
2'b00:out=in[0];
2'b01:out=in[1];
2'b10:out=in[2];
2'b11:out=in[3];
endcase
endmodule

module mux16_1(in,sel,out);
input [15:0]in;
input [3:0]sel;
output out;
wire [3:0] sel_1;

mux4_1 mux1(in[3:0],sel[3:2],sel_1[0]);
mux4_1 mux2(in[7:4],sel[3:2],sel_1[1]);
mux4_1 mux3(in[11:8],sel[3:2],sel_1[2]);
mux4_1 mux4(in[15:12],sel[3:2],sel_1[3]);

mux4_1 mux5(sel_1[3:0],sel[1:0],out);
endmodule
```

TestBench Code-

```
module mux16_1_tb();
reg [0:15] in;
reg [0:3] sel;
wire out;

mux16_1 dut(in,sel,out);

initial
begin
#20 in=16'b1000000000000000; sel=4'b1111;
#20 in=16'b0100000000000000; sel=4'b0001;
#20 in=16'b0010000000000000; sel=4'b0010;
#20 in=16'b0001000000000000; sel=4'b0011;

#20 in=16'b0000100000000000; sel=4'b0100;
#20 in=16'b0000010000000000; sel=4'b0101;
#20 in=16'b0000001000000000; sel=4'b0110;
#20 in=16'b0000000100000000; sel=4'b0111;

#20 in=16'b0000000010000000; sel=4'b1000;
#20 in=16'b0000000001000000; sel=4'b1001;
#20 in=16'b0000000000100000; sel=4'b1010;
#20 in=16'b0000000000010000; sel=4'b1011;

#20 in=16'b0000000000001000; sel=4'b1100;
#20 in=16'b0000000000000100; sel=4'b1101;
#20 in=16'b0000000000000010; sel=4'b1110;
#20 in=16'b0000000000000001; sel=4'b1111;
end
endmodule
```

Schematic View of 4X1 Multiplexerr-



Simulation Result of 4X1 Multiplexer-