

Day8-4x4_Array_Multiplier

#75daysRTL

Array Multiplication is the basic type of multiplication that we usually do with pen and paper. It is the most basic implementation of multiplication for higher-order bits.

Disadvantages:

1. Delay in computation and high power consumption
2. Physical implementation takes a large area.

Advantages:

1. Simple implementation that uses an add-shift algorithm.
2. Easy to route and scalable.

Array Multiplication 4X4 –

$$\begin{array}{rcccccccc} & & & & a_3 & a_2 & a_1 & a_0 \\ x & & & & b_3 & b_2 & b_1 & b_0 \\ \hline & & & & p_{30} & p_{20} & p_{10} & p_{00} \\ & & & p_{31} & p_{21} & p_{11} & p_{01} & x \\ & & p_{32} & p_{22} & p_{12} & p_{02} & x & x \\ & p_{33} & p_{23} & p_{13} & p_{03} & x & x & x \\ \hline z_7 & z_6 & z_5 & z_4 & z_3 & z_2 & z_1 & z_0 \end{array}$$

Verilog Code –

```
module arraymul4x4(  
    input [3:0]a,  
    input [3:0]b,  
    output [7:0]res );  
  
assign res[0]=(a[0]&b[0]);  
wire x1,x2,x3,x4,x5,x6,x7,x8,x9,x10,x11,x12,x13,x14,x15,x16,x17;
```

```

halfadder halfadder1(res[1],x1,(a[1]&b[0]),(a[0]&b[1]));
fulladder fulladder1(x2,x3,a[1]&b[1],(a[0]&b[2]),x1);
fulladder fulladder2(x4,x5,(a[1]&b[2]),(a[0]&b[3]),x3);
halfadder halfadder2(x6,x7,(a[1]&b[3]),x5);

```

```

halfadder halfadder3(res[2],x15,x2,(a[2]&b[0]));
fulladder fulladder5(x14,x16,x4,(a[2]&b[1]),x15);
fulladder fulladder4(x13,x17,x6,(a[2]&b[2]),x16);
fulladder fulladder3(x9,x8,x7,(a[2]&b[3]),x17);

```

```

halfadder halfadder4(res[3],x12,x14,(a[3]&b[0]));
fulladder fulladder8(res[4],x11,x13,(a[3]&b[1]),x12);
fulladder fulladder7(res[5],x10,x9,(a[3]&b[2]),x11);
fulladder fulladder6(res[6],res[7],x8,(a[3]&b[3]),x10);
endmodule

```

```

module fulladder(sum,carry,a,b,cin);
input a,b,cin;
output sum,carry;
wire sum1,sum2,carry1,carry2;
halfadder d0(.a(a),.b(b),.sum(sum1),.carry(carry1));
halfadder d1(.a(sum1),.b(cin),.sum(sum),.carry(carry2));
assign carry=carry1|carry2;
endmodule

```

```

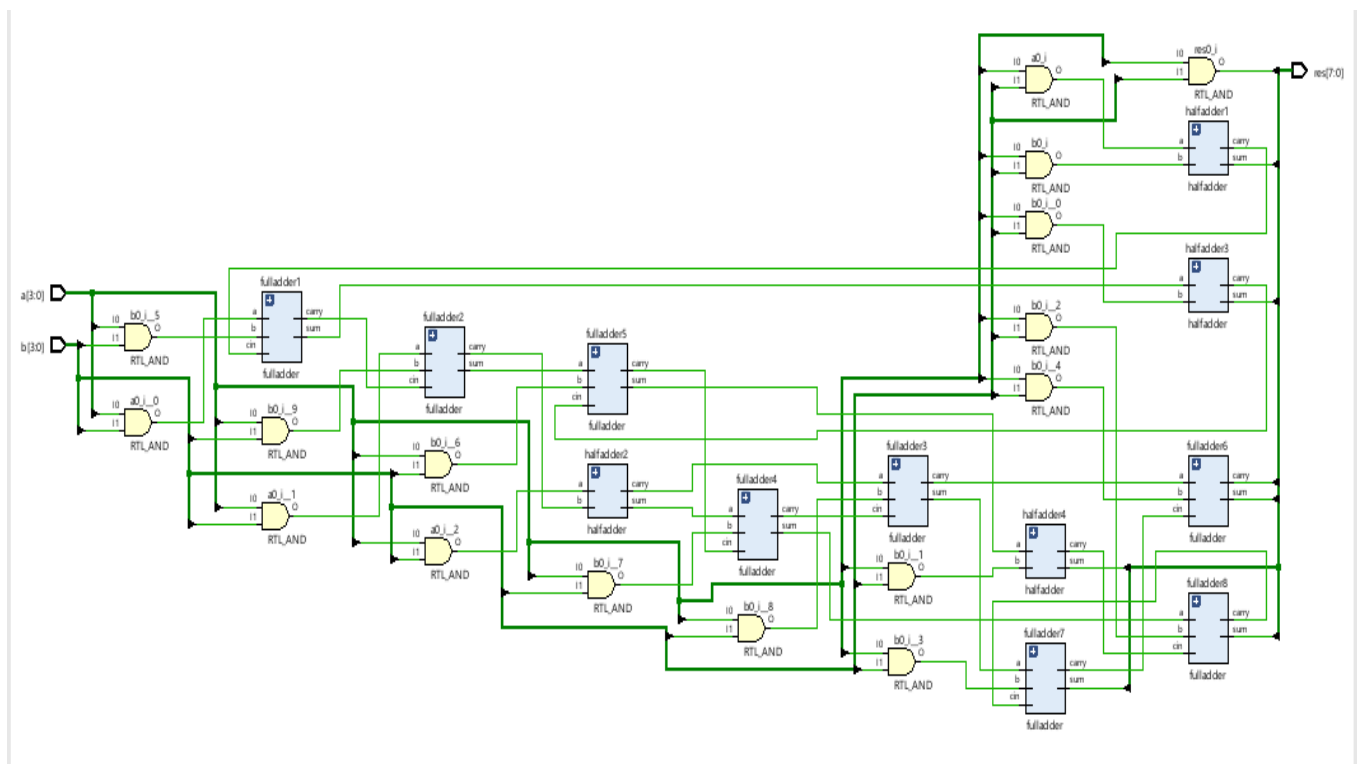
module halfadder(sum,carry,a,b);
input a,b;
output sum,carry;
assign sum=a^b;
assign carry=a&b;
endmodule

```

TestBench Code-

```
module arraymul4x4_tb();  
    reg [3:0] a, b;  
    wire [7:0] res;  
  
    arraymul4x4 mul(a,b,res);  
  
    initial begin  
        a = 1; b = 0; #30;  
        a = 7; b = 5; #30;  
        a = 8; b = 9; #30;  
        a = 4'hf; b = 4'hf;#30;  
        $finish;  
    end  
end  
endmodule
```

Schematic View of 4X1 Multiplexerr-



Simulation Result of 4X1 Multiplexer-

