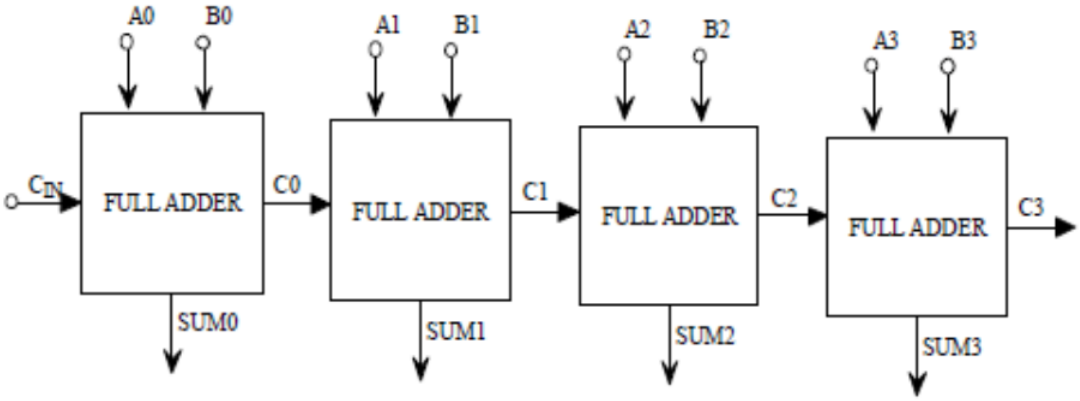
Day4-4bit Ripple Carry Adder #75daysRTL

A 4-bit Ripple Carry Adder is an adder that adds 4 bits of input a and b to produce sum and carry as output. To add multiple bits, multiple full adders are cascaded to produce the summation of the input numbers of higher bits.

Generation of 4bit RCA- To implement 4bit RCA we require 4 full adders.

Block Diagram –



Verilog Code –

```
module ripplecarryadder(a,b,cin,sum,carry);
input [3:0]a;
input [3:0]b;
input cin;
output [3:0]sum;
output carry;
wire c0,c1,c2;
fulladder dut1(sum[0],c0,a[0],b[0],cin);
fulladder dut2(sum[1],c1,a[1],b[1],c0);
fulladder dut3(sum[2],c2,a[2],b[2],c1);
fulladder dut4(sum[3],carry,a[3],b[3],c2);
endmodule


module fulladder(sum,carry,a,b,cin);
input a,b,cin;
output sum,carry;
wire sum1,sum2,carry1,carry2;
halfadder d0(a,b,sum1,carry1);
```

```
halfadder d1(sum1,cin,sum,carry2);
assign carry=carry1|carry2;
endmodule

module halfadder(a,b,sum,carry);
input a,b;
output sum,carry;
assign sum=a^b;
assign carry=a&b;
endmodule
```

TestBench Code-

```
module ripplecarryadder_tb();
reg [3:0]a,b;
reg cin;
wire [3:0]sum;
wire carry;
ripplecarryadder dt(a,b,cin,sum,carry);
initial begin
a=4'b0000;b=4'b0010;
cin=0;
#10;
a=4'b0110;b=4'b1010;
cin=0;
#10;
a=4'b1000;b=4'b1010;
cin=1;
#10;
a=4'b0000;b=4'b0010;
cin=1;
#10;
a=4'b0100;b=4'b1110;
```

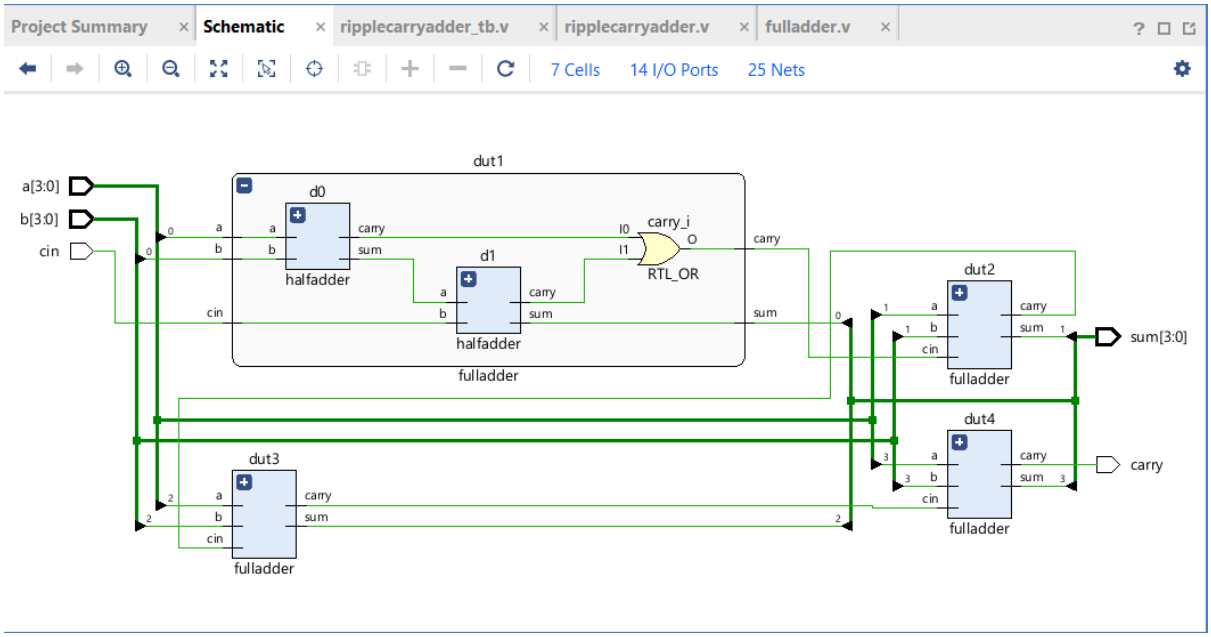
cin=1;

$finish;

end

endmodule

Schematic View of 4bit RCA-



Simulation Result of 4bit RCA-