Day11-1X4_Demultiplexer #75daysRTL

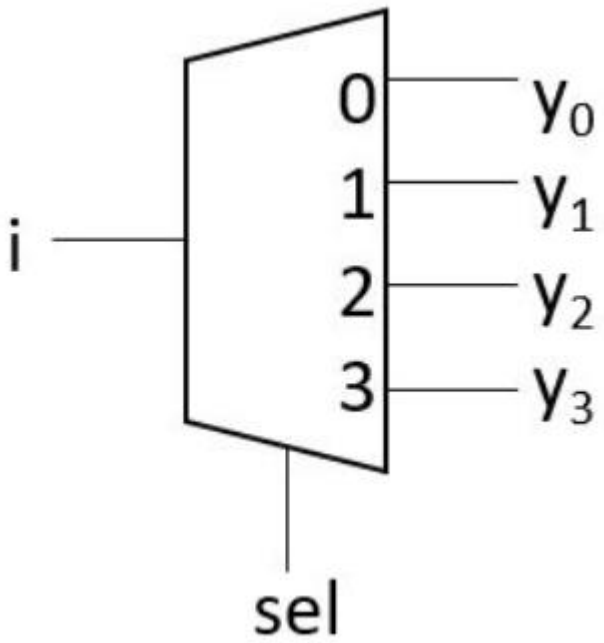
A demultiplexer (DeMux) is a combinational circuit that works exactly opposite to a multiplexer. A DeMux has a single input line that connects to any one of the output lines based on its control input signal (or selection lines)

Usually, for ‘n’ selection lines, there are N = 2^n output lines. We have designed a 1X4 Demultiplexer using 2 selection lines

Truth Table-

Input – Sel[1]	Input – Sel[0]	Output- Y[0]	Output – Y[0]	Output – Y[2]	Output – Y[3]
0	0	i	0	0	0
0	1	0	i	0	0
1	0	0	0	i	0
1	1	0	0	0	I

Block Diagram of 1X4 Demultiplexer-



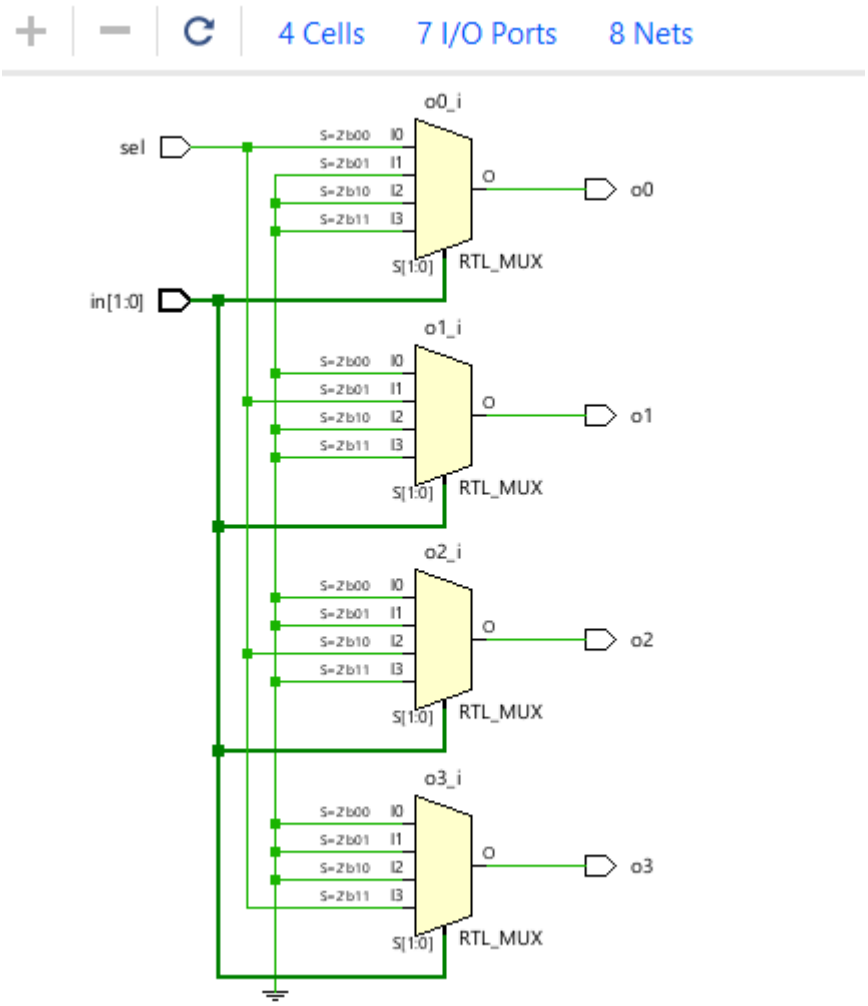
Verilog Code –

```
module demux1x4(input [1:0] in,
  input  sel,
  output reg o0,o1,o2,o3);
  always @(*) begin
    case(in)
      2'h0: {o0,o1,o2,o3} = {sel,3'b0};
      2'h1: {o0,o1,o2,o3} = {1'b0,sel,2'b0};
      2'h2: {o0,o1,o2,o3} = {2'b0,sel,1'b0};
      2'h3: {o0,o1,o2,o3} = {3'b0,sel};
    endcase
  end
endmodule
```

TestBench Code-

```
module demux1x4_tb();
reg[1:0]in;
reg sel;
wire o0,o1,o2,o3;
demux1x4 dut (in,sel,o0,o1,o2,o3);
initial begin
in=2'b00; sel=0; #20;
in=2'b00; sel=1; #20;
in=2'b01; sel=0; #20;
in=2'b01; sel=1; #20;
in=2'b10; sel=0; #20;
in=2'b10; sel=1; #20;
in=2'b11; sel=0; #20;
in=2'b11; sel=1; #20;
$finish;
end
endmodule
```

Schematic View of 1x4 Demultiplexer-



Simulation Result of 1x4 Demultiplexer-