Day1-Half Adder #75daysRTL

Half adder is a combinational circuit in which a computer binary adds two binary inputs a & b to produce output sum & carry.

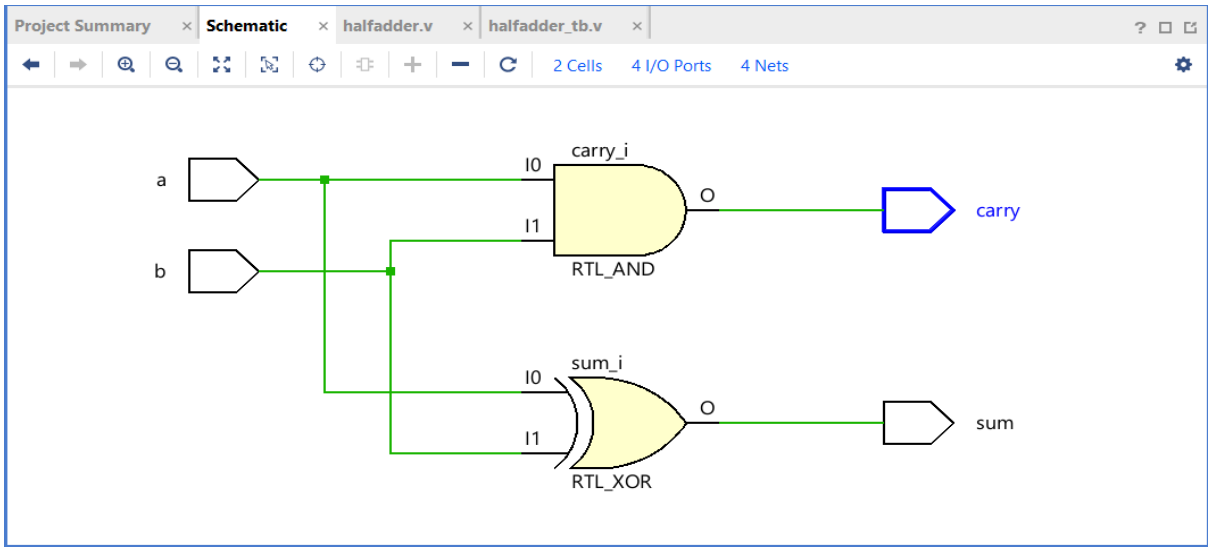
Truth Table-

Input - A	Input - B	Output - Sum	Output - Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Sum = A XOR B

Carry = A AND B

Schematic Diagram-



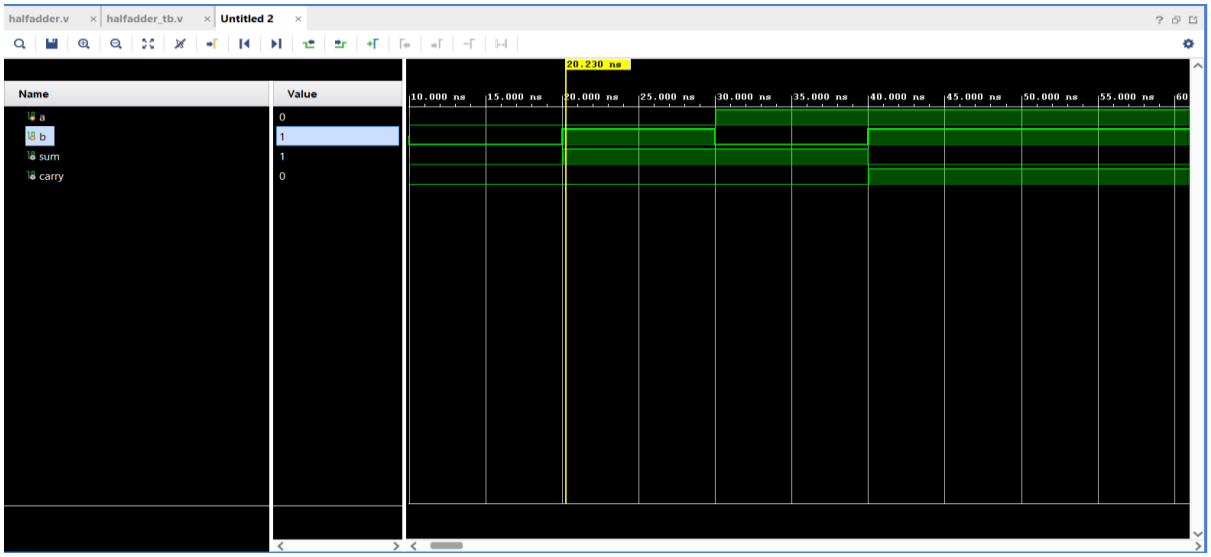
Verilog Code-

```
module halfadder(a,b,sum,carry);
input a,b;
output sum,carry;
assign sum=a^b;
assign carry=a&b;
endmodule
```

Verilog TestBench-

```
module halfadder_tb();
reg a,b;
wire sum,carry;
halfadder dut (a,b,sum,carry);
initial begin
#10
a=0;b=0;
#10
a=0;b=1;
#10
a=1;b=0;
#10
a=1;b=1;
end
endmodule
```

Simulation Results-



Half Adder is one of the basic building blocks of any logic design which includes addition operations.