Day2-Full Adder using Half Adder #75daysRTL

Full adder is a combinational circuit that consists of 3 inputs to generate a sum and carry it as output.

Generation of Full Adder-

1. **Using Gates based on the Equation-**

   Sum = A xor B xor Cin
   Carry = (A.B)+(B.Cin)+(A.Cin)

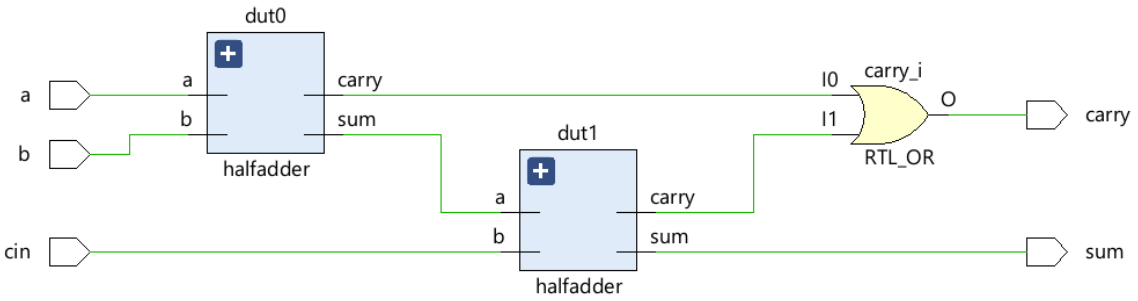
   To implement Full Adder using Gates we require **2XOR, 3AND, 2OR gates**.

2. **Using Half Adder circuit- (Mostly Used)**

   Half adder is a combinational circuit in which a computer binary adds two binary inputs a & b to produce output sum & carry.

   To implement Full Adder using Half Adder we require **2 Half Adders, 1OR gate.**

Schematic View-



Verilog Code-

```
module fulladder(sum,carry,a,b,cin);

input a,b,cin;

output sum,carry;

wire sum1,sum2,carry1,carry2;

halfadder dut0(a,b,sum1,carry1);

halfadder dut1(sum1,cin,sum,carry2);

assign carry=carry1|carry2;

endmodule

module halfadder(a,b,sum,carry);
```

```
input a,b;
output sum,carry;
assign sum=a^b;
assign carry=a&b;
endmodule
```

TestBench Code-

```
module fulladder_tb( );
reg a,b,cin;
wire sum,carry;
fulladder uut(sum,carry,a,b,cin);
initial
begin
a=0;b=0;cin=0;
#10 a=0;b=0;cin=1;
#10 a=0;b=1;cin=0;
#10 a=0;b=1;cin=1;
#10 a=1;b=1;cin=0;
#10 a=1;b=0;cin=0;
#10 a=0;b=1;cin=0;
#10 a=0;b=1;cin=1;
#10 $finish;
end
endmodule
```

Simulation Results-