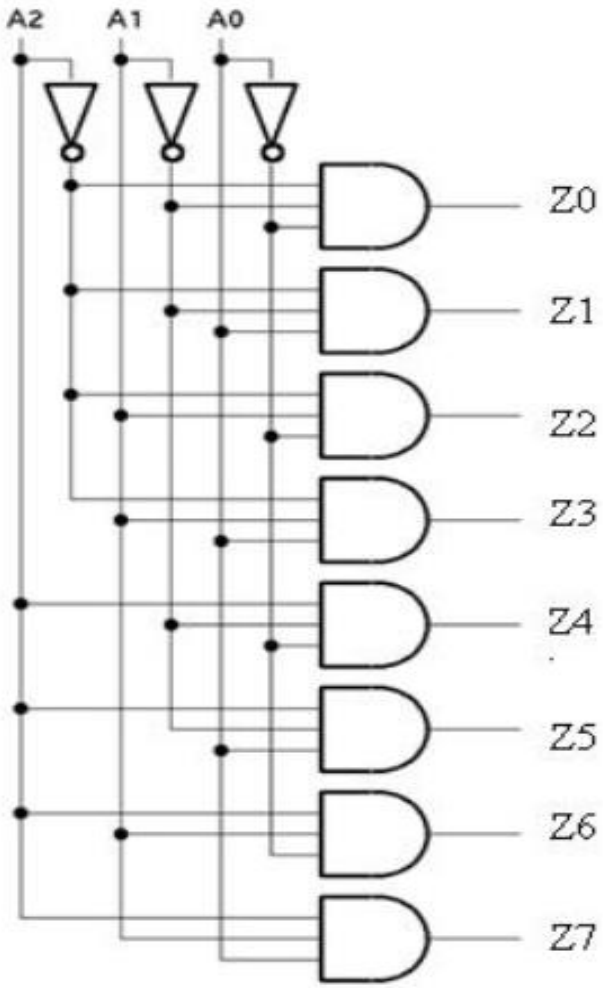
Day13- 3 to 8 Decoder #75daysRTL

3 to 8 decoder circuit gives 8 logic outputs for 3 inputs and has an enable pin. The circuit is designed with AND and NAND logic gates. It takes 3 binary inputs and activates one of the eight outputs. A 3 to 8-line decoder circuit is also called a binary to an octal decoder.

Truth Table-

X	Y	Z	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0
0	0	0	0	0	0	0	0	0	0	**1**
0	0	1	0	0	0	0	0	0	**1**	0
0	1	0	0	0	0	0	0	**1**	0	0
0	1	1	0	0	0	0	**1**	0	0	0
1	0	0	0	0	0	**1**	0	0	0	0
1	0	1	0	0	**1**	0	0	0	0	0
1	1	0	0	**1**	0	0	0	0	0	0
1	1	1	**1**	0	0	0	0	0	0	0

Circuit Diagram of 3 to 8 Decoder-



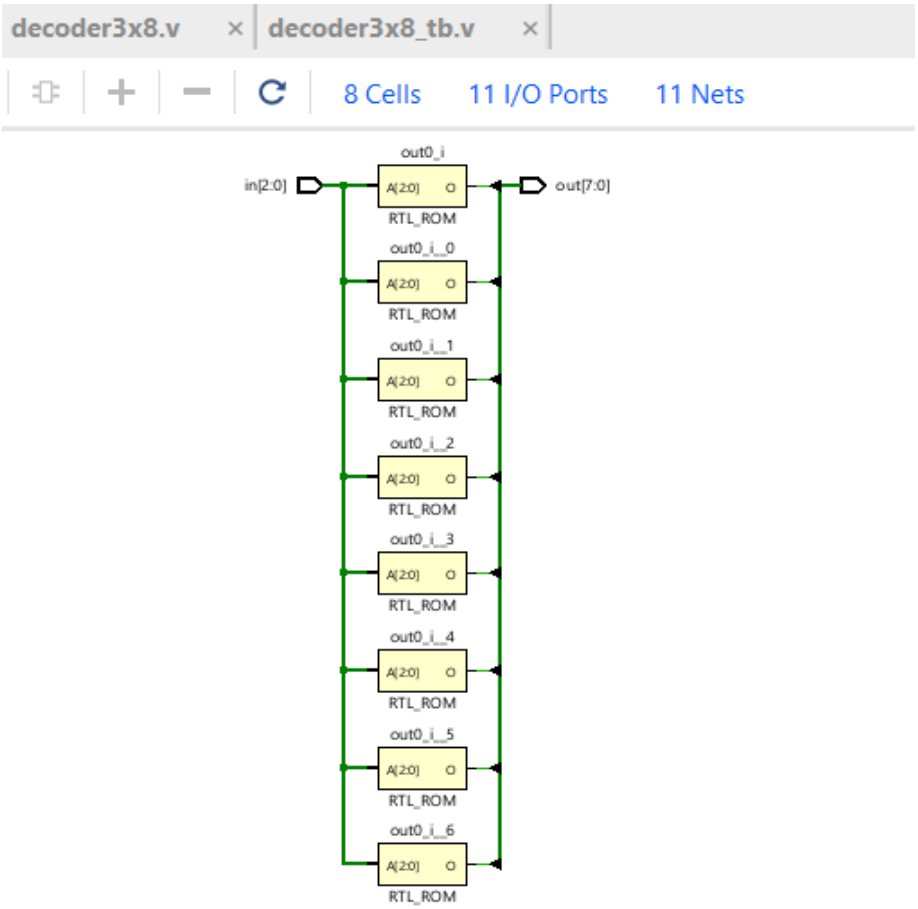
Verilog Code –

```
module decoder3x8(
 input [2:0] in,
 output [7:0] out
);
 assign out[0] = (in == 3'b000) ? 1'b1 : 1'b0;
 assign out[1] = (in == 3'b001) ? 1'b1 : 1'b0;
 assign out[2] = (in == 3'b010) ? 1'b1 : 1'b0;
 assign out[3] = (in == 3'b011) ? 1'b1 : 1'b0;
 assign out[4] = (in == 3'b100) ? 1'b1 : 1'b0;
 assign out[5] = (in == 3'b101) ? 1'b1 : 1'b0;
 assign out[6] = (in == 3'b110) ? 1'b1 : 1'b0;
 assign out[7] = (in == 3'b111) ? 1'b1 : 1'b0;
endmodule
```

TestBench Code-

```
module decoder3x8_tb();
reg [2:0] in;
wire [7:0] out;
decoder3x8 dut (  .in(in),  .out(out) );
initial begin
  in = 3'b000; #10;
  in = 3'b001; #10;
  in = 3'b010; #10;
  in = 3'b011; #10;
  in = 3'b100; #10;
  in = 3'b101; #10;
  in = 3'b110; #10;
  in = 3'b111; #10;
  #10 $finish;
end
endmodule
```

Schematic View of 3 to 8 Decoder-



Simulation Result of 3 to 8 Decoder -