# Day6-4X1_Multiplexer #75daysRTL

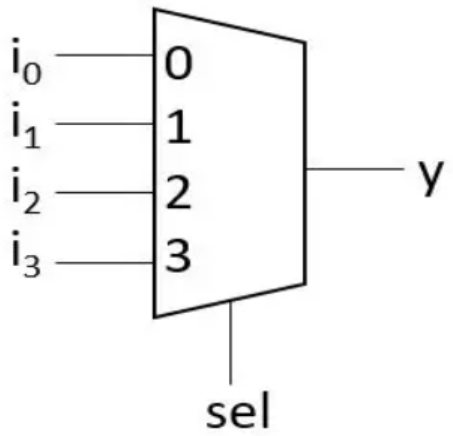
A multiplexer is a data selector device that selects one input from several input lines, depending upon the enabled, select lines, and yields one single output.

A multiplexer of **$2^n$ inputs has n select lines**, which are used to select which input line to send to the output. There is only one output in the multiplexer. We designed a 4x1 Multiplexer where for 4 input lines 1 output is selected.

**Truth Table (Selection Lines)-**

| Select-S0 | Select – S1 | Output Line |
|---|---|---|
| 0 | 0 | A0 |
| 0 | 1 | A1 |
| 1 | 0 | A2 |
| 1 | 1 | A3 |

**Block Diagram –**




**Verilog Code –**

```
module mux4_1(in,sel,out);

input [3:0]in;

input [1:0]sel;

output reg out;


always@(in,sel,out)

begin

case(sel)
```

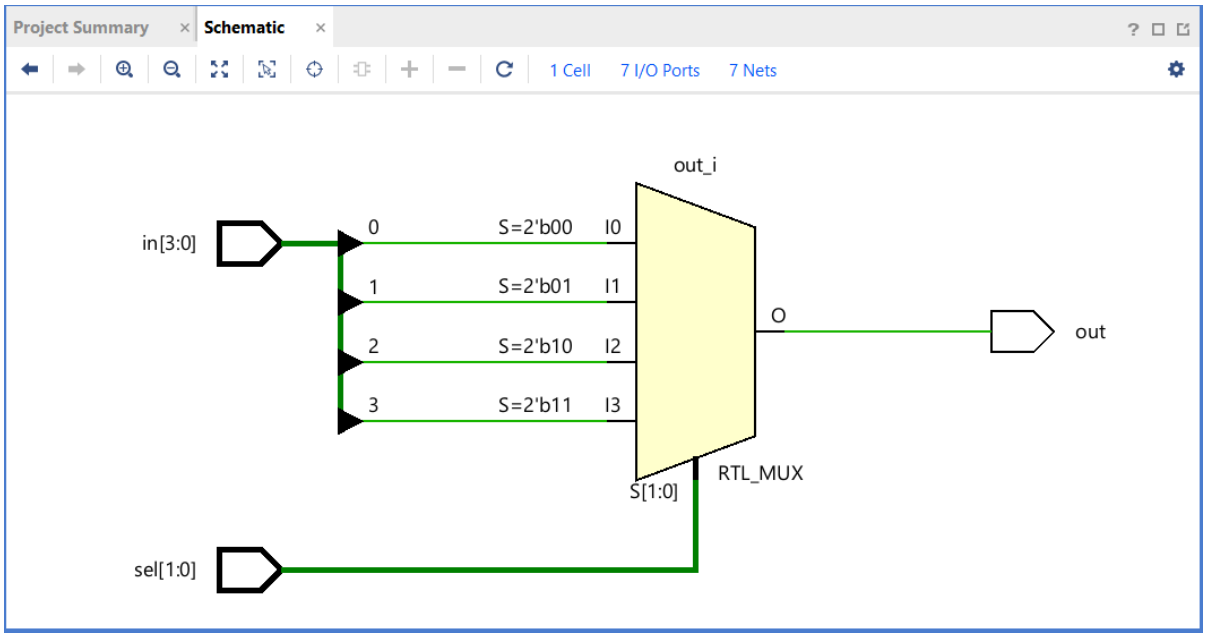
```
2'b00:out=in[0];
2'b01:out=in[1];
2'b10:out=in[2];
2'b11:out=in[3];
endcase
```

**TestBench Code-**

```
module mux4_1_tb();
reg [3:0]in;
reg [1:0]sel;
wire out;

mux4_1 dut(in,sel,out);
initial begin
in=0;sel=0;
#10;
in=4'b1010;
sel=2'b01;
#10;
sel=2'b11;
#10;
sel=2'b00;
#10;
sel=2'b10;
#10;
$finish;
end
endmodule
```

## Schematic View of 4X1 Multiplexerr-




## Simulation Result of 4X1 Multiplexer-