DDR-L:DDR-R=
DDR-L:CXL-ASIC=
CXL-DMSim$_L$:CXL-DMSim$_A$=
Cfg1. 100%:0%
Cfg2. 50%:50%
Cfg3. 0%:100%
Cfg4. 100%:0%
Cfg5. 50%:50%
Cfg6. 0%:100%
Cfg7. 100%:0%
Cfg8. 50%:50%
Cfg9. 0%:100%
Memory Configurations
Cfg9
Cfg8
Cfg7
Cfg6
Cfg5
Cfg4
Cfg3
Cfg2
Cfg1
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
l3cache.overall.AvgMissLatency
dram.avgMemAccLat
dram.avgQLat
100% CXL-DMSim$_A$ is zero
100% CXL-DMSim$_A$ is zero
0.0
0.4
0.8
1.2
1.6
Normalized Latency
(b) Latency metrics