

Advanced Gate Driving Techniques and Inverter Design Considerations of  
Wide-Band-Gap Devices

by

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## ABSTRACT

The continuous demand for higher power density and better efficiency to reduce the global energy consumption, is the driving force to introduce new semiconductor technologies. Wide-band-gap (WBG) material based devices such as gallium nitride high electron mobility transistors (GaN HEMTs) and silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) are considered promising candidates for replacing conventional silicon MOSFETs, mainly because of their capabilities of higher switching frequencies with less switching and conduction losses. Although WBG devices can largely improve the conversion efficiency, the implementation of WBG devices brings in some challenges in power converter design.

Firstly, the high voltage changing slew rate of WBG devices introduces a distortion current to the gate through the coupling capacitance of the device. The distortion current may cause mis-trigger or overvoltage breakdown of the device gate. This issue is so-called crosstalk effect. This dissertation proposes a multilevel gate driving profile to address this issue.

Secondly, due to the gate-to-substrate voltage bias, the integration of multiple GaN devices suffers from the high on-state resistance. This issue is so-called current collapse or electron trap. This dissertation proposes a gate current injection method to address this issue. By injecting relatively large gate current at specific time period, the on-state resistance is largely improved at both hard-switching and soft-switching scenarios.

Thirdly, series connection of switches is an effective way to achieve higher blocking voltage of the device. The serial connection of WBG devices suffers from the dynamic voltage unbalance and short-circuit protection issues. The additional short-circuit scenarios are found in the series-connected devices, which are not covered by

the traditional short-circuit protection scheme. Dynamic voltage sharing problem is addressed using proposed current source gate driver. Besides, the short-circuit protection circuit is integrated in the proposed gate driver to cover all the short-circuit scenarios of series-connected devices.

Finally, this dissertation uses a practical converter design example to comprehensively elaborate the design considerations of WBG based converters. A 1.5 MHz/ 2 kV/ 80 A commercial burst-mode inverter using SiC MOSFETs is designed for electromagnetic acoustic transducer. This inverter design includes comprehensive fault protection, hardware and controller design.

# ***To My Family:***

*My Wife: Zhaotong Duan*

*My Son: Zeyu Liu*

*My Parents: Jinbao Liu and Yuhua Li*

*My Parents In Law: Yiwu Duan and Huazhi Deng*

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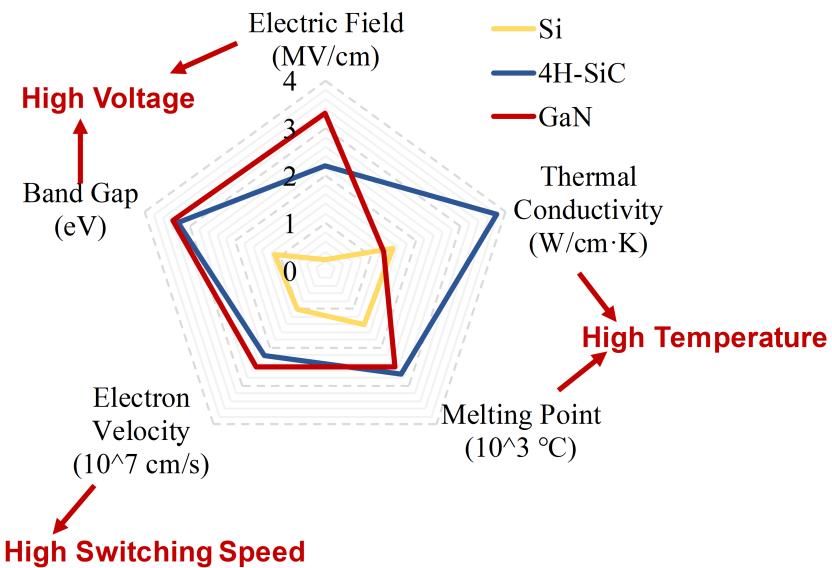
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# Chapter 1

## INTRODUCTION

### 1.1 Overview of Wide-band-gap (WBG) Power Devices

In modern industries, requirements for the performance of various power electronic based converters are becoming stricter in terms of capacity, voltage level, efficiency, and size (switching frequency related issues). In order to enhance the performance of existing power converters, replacing conventional Si switching devices with wide-band-gap (WBG) switching devices such as gallium nitride (GaN) high electron mobility transistors (HEMTs) and silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) is currently a popularly adopted method.

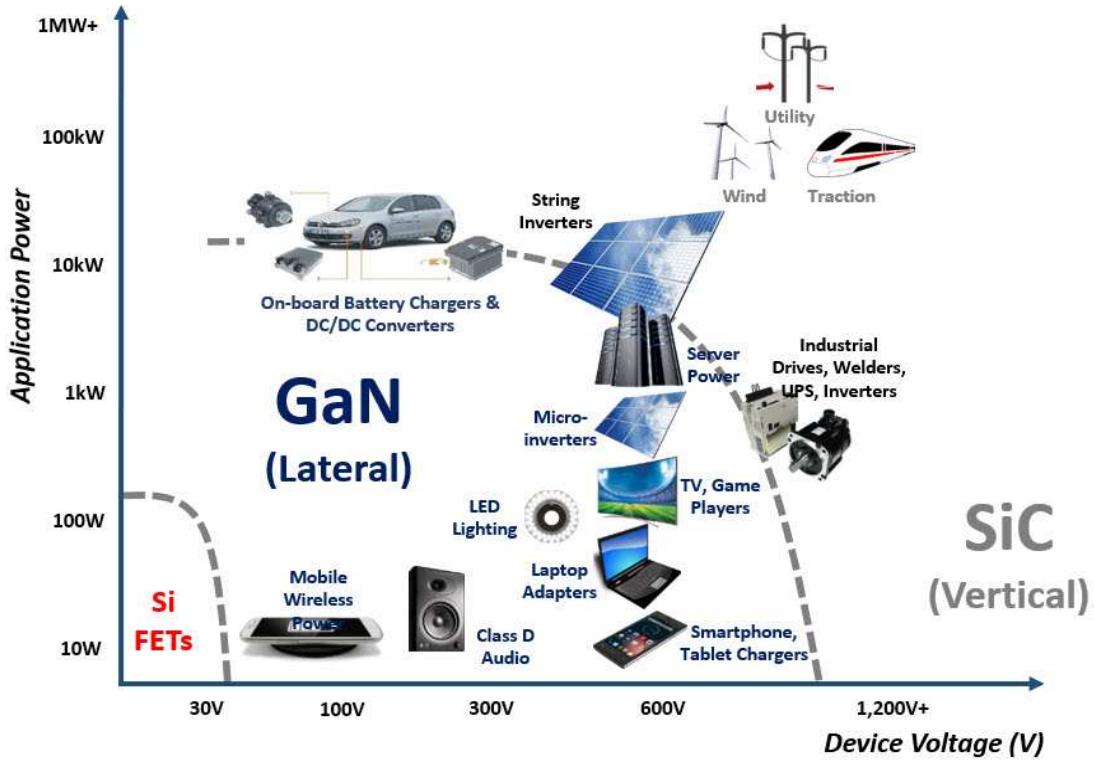


**Figure 1.1:** Si vs. SiC vs. GaN, the Material Characteristics Comparison.

WBG semiconductor materials offer superior characteristics to those of Si, as shown in Fig. 1.1. The respective merits of GaN and SiC lead to the advantageous

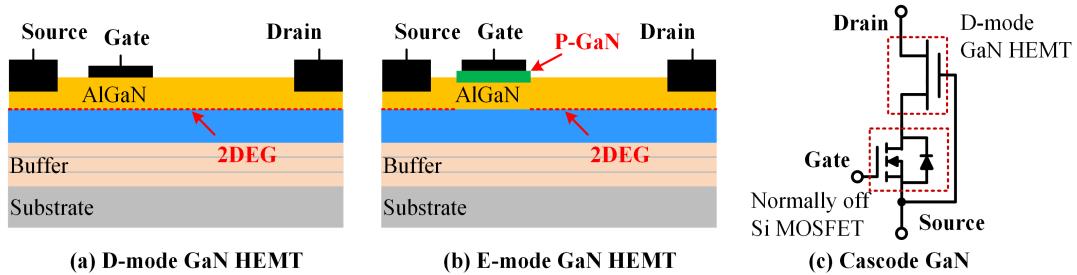
adoption of GaN HEMTs for low ( $< 1$  kW) to mid ( $< 10$  kW) power applications and SiC MOSFETs for mid to high ( $> 10$  kW) power applications in practical design scenarios, as shown in Fig. 1.2. The superiority of GaN HEMTs is yet to be fully utilized because they feature some form of heterogeneous integration with dissimilar substrate. This leads to large thermal boundary resistance between GaN and substrate, causing the self-heat issue, which may cause the switching device to overheat. However, GaN HEMTs offer the highest efficiency and switching speed, and SiC MOSFETs provide the highest voltage, current, and temperature capabilities. GaN's wide band gap allows power applications with voltages between 100 V and 600 V to use smaller, more efficient chips, reducing costs and energy consumptions. SiC, with higher thermal conductivity, is suited for the highest power applications that require large heat dissipation. Current flow is another critical difference. SiC is a ‘vertical’ device which is optimized for high power only, while commercial GaN has a ‘lateral’ structure that makes monolithic (‘same chip’) integration possible. The lateral structure enables GaN power ICs to integrate power FETs with drive, logic, protection, sensing and control.

The GaN HEMT is designed with a unique aluminum gallium nitride (AlGaN)/GaN heterojunction structure where two-dimensional electron gas (2DEG) is formed. The 2DEG allows large bidirectional current and yields extremely low on resistance. GaN HEMTs are currently divided into three types: depletion mode (D-mode), enhancement mode (E-mode), and cascode devices. The D-mode GaN HEMT, as shown in Fig. 1.3(a), is naturally on because of the 2DEG and can be turned off with negative gate-source voltage. The E-mode GaN HEMT, as shown in Fig. 1.3(b), is normally off because the 2DEG has been depleted by an additional P-doped layer of GaN or AlGaN on the gate, and it can be turned on with appropriate gate-source voltage. The cascode GaN HEMT, as shown in Fig. 1.3(c), is also normally off because it consists



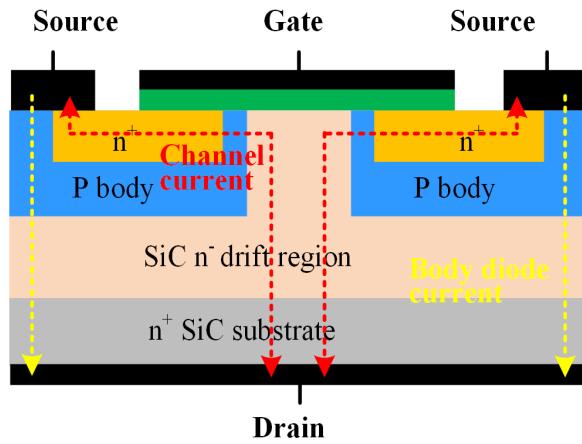
**Figure 1.2:** Landscape of WBG Devices[1]

of a D-mode GaN HEMT and an additional high-speed low-voltage Si MOSFET, and it can be turned on with appropriate gate-source voltage applied on the Si MOSFET. E-mode and cascode GaN HEMTs possess different characteristics mainly because of the additional Si MOSFET in the cascode device: the E-mode device offers lower on resistance, higher operating temperature, and no body diode, while the cascode device offers less strict driving requirements [2–6].



**Figure 1.3:** Structure of GaN HEMTs.

The SiC MOSFET has a similar structure to that of Si MOSFET, as shown in Fig. 1.4, but the thickness can be made an order smaller because of SiC's higher voltage capability. This leads to much smaller on resistance (although not as small as that of the GaN HEMT). Additionally, the SiC MOSFET offers the highest power capability. The operation of the SiC MOSFET is the same as that of the Si MOSFET: with appropriate gate-source voltage, the device can be turned on, and the body diode is used for reverse conduction during off state [7].



**Figure 1.4:** Structure of SiC MOSFETs.

The main challenge of using the WBG semiconductor switching devices is overcoming potential difficulties introduced from their high slew rates, which could worsen electromagnetic interference (EMI) level and may cause voltage oscillation and instability [2–6]. Besides, the high slew rates result in additional issues in some advanced applications, such as monolithic integration of GaN HEMTs and series-connected W-BG devices. The following paragraphs will introduce the challenges when designing WBG devices based converters.

## 1.2 Challenges in Crosstalk Suppression of WBG Devices

Now the Silicon Carbide device is expected to replace the Si device due to its high switching speed capability, allowing shorter dead-time in a phase-leg and higher switching frequency. These benefits of SiC MOSFETs lead to higher power density and higher efficiency of power electronics converters [8–11]. However, in practical application, the switching speed of SiC MOSFETs is limited and usually much lower than expected potential speed, especially in phase-leg configuration because of crosstalk phenomenon [10–16].

The biggest problem is the parasitic inductance in both gate loop and main power loop, which may introduce significant oscillation in device drain-source voltage ( $V_{ds}$ ) and gate-source voltage ( $V_{gs}$ ) at high switching speed. Besides, the equivalent coupling capacitor (gate-drain capacitor,  $C_{gd}$ , miller capacitor) between power loop and gate loop will induce current to the gate during  $V_{ds} \frac{dv}{dt}$  transient. This miller current charges  $C_{gs}$  while  $dv/dt$  is positive, which happens during device turn-off transient, and discharges  $C_{gs}$  while  $dv/dt$  is negative, which occurs during device turn-on transient. If positive  $dv/dt$  happens during or after  $V_{gs}$  falling edge, the additional miller charging current may delay the turn-off, or mis-trigger the device after turn-off, which can result in the phase leg shoot-through fault. If negative  $dv/dt$  happens before  $V_{gs}$  rising edge, the additional miller discharging current will introduce a negative overshooting on the negative gate voltage, which may cause over-voltage breakdown of device gate [8]. These problems are so-called crosstalk effect [10–16]. The mis-trigger problem is severe in hard-switching case and the negative overshooting problem is severe in soft-switching case. To avoid miller effect caused failure, the device switching speed needs to be forced low [8–13], thus the fast switching characteristics of the SiC MOSFET is not fully utilized and the device efficiency will hit a certain boundary.

Previous work has been reported to deal with crosstalk problems in two aspects: power loop and gate driver loop. In terms of power loop, many papers [14, 17–20] make improvements on enhancing  $dv/dt$  immunity of isolation barrier [14], minimizing common source inductance [20] or controlling  $V_{ds} dv/dt$  and  $I_{ds} di/dt$  [17–19]. In terms of gate loop, commonly used crosstalk mitigation methods fall into four categories:

1. Add external  $C_{gs}$  to shunt the miller current [21–24]. This additional  $C_{gs}$  provides low impedance for miller current, leading to gate voltage spikes reduction and crosstalk suppression. But this external  $C_{gs}$  will slow down the device switching speed and raise the device switching losses.
2. Employ active miller clamping [24–26]. This method is widely used in commercial gate driver ICs [24, 25]. The principle is that  $V_{gs}$  will be detected by the gate driver. Once the  $V_{gs}$  rises to threshold voltage during off-state, an additional transistor between gate and off-state voltage supply will be triggered and provides a short-circuit path to clamp the  $V_{gs}$  back to off-state voltage. However, for SiC devices, due to the high switching speed, the measured  $V_{gs}$ , largely interfered by coupling common-source inductance and internal gate resistor, is not real device  $V_{gs}$ . Besides, the miller clamping bandwidth is not high enough for the mis-trigger suppression because of  $V_{gs}$  detection loop parasitic inductance and circuit propagation delay [20]. And the miller clamping function inserted in the gate driver IC has limited current capability, usually within hundred milli-ampere level. This current capability is far lower than the miller current level, usually within ampere level for SiC MOSFETs. So, the miller clamping function helps little for SiC devices [20].
3. Use a negative gate off voltage [15–23, 27, 28]. This method can suppress the mis-trigger issue but worsen the gate negative overvoltage issue.
4. Apply multi-level gate voltage [21–23, 29, 30]. The basic idea is to modify the gate voltage during the  $V_{ds} dv/dt$  transient to avoid negative overvoltage breakdown

or mis-trigger. During the turn-off transient of positive  $V_{ds}$   $dv/dt$ , if the  $V_{gs}$  jumps to the threshold voltage, usually a relatively low voltage for the SiC MOSFET [22], the switch will mis-turn on. This issue can be overcome by lowering the off-state gate voltage to a safe negative level (e.g. -5 V [22]), to make  $V_{gs}$  harder to reach the threshold voltage. However, the issue followed is the higher risk of negative gate overvoltage breakdown before the turn-on transient, since the starting point of the negative overshoot is already a negative voltage. To address this problem, the state-of-the-art work proposed the methods of clamping the gate voltage to 0 V or less negative level, e.g. -2 V, by adopting different circuit topologies. The intelligent gate driver proposed in [10–12, 28, 31] can be actively controlled to generate multi-level  $V_{gs}$  to mitigate the issue, with additional transistors and diodes. However, the auxiliary switches themselves introduce additional control signals and gate driving circuit. Thus, in addition to the isolation barrier required between the power switch and the controller, the auxiliary switches also need their own driving signals and galvanic isolations, which adds large number of auxiliary components and makes the circuit relatively complex. Moreover, these additional isolation barriers introduce additional common mode noise conduction path for the leakage current caused by the high  $dv/dt$  of the device, which may distort the control signal of the other channel at the controller side and may cause severe EMI issue (e.g. mis-trigger)[14, 32].

A smart self-driving multi-level gate driver (SMGD) for SiC MOSFETs, with mis-triggering and negative overvoltage suppression function, is proposed. Using original  $V_{gs}$  with simple RC delay as control signal of the auxiliary circuit, the proposed SMGD has following advantages over the other crosstalk suppression techniques: 1. No additional control signals; 2. No additional DC/DC power supply and signal isolation stages for the auxiliary switch; 3. Easy to be implemented on the commercial gate driver IC.

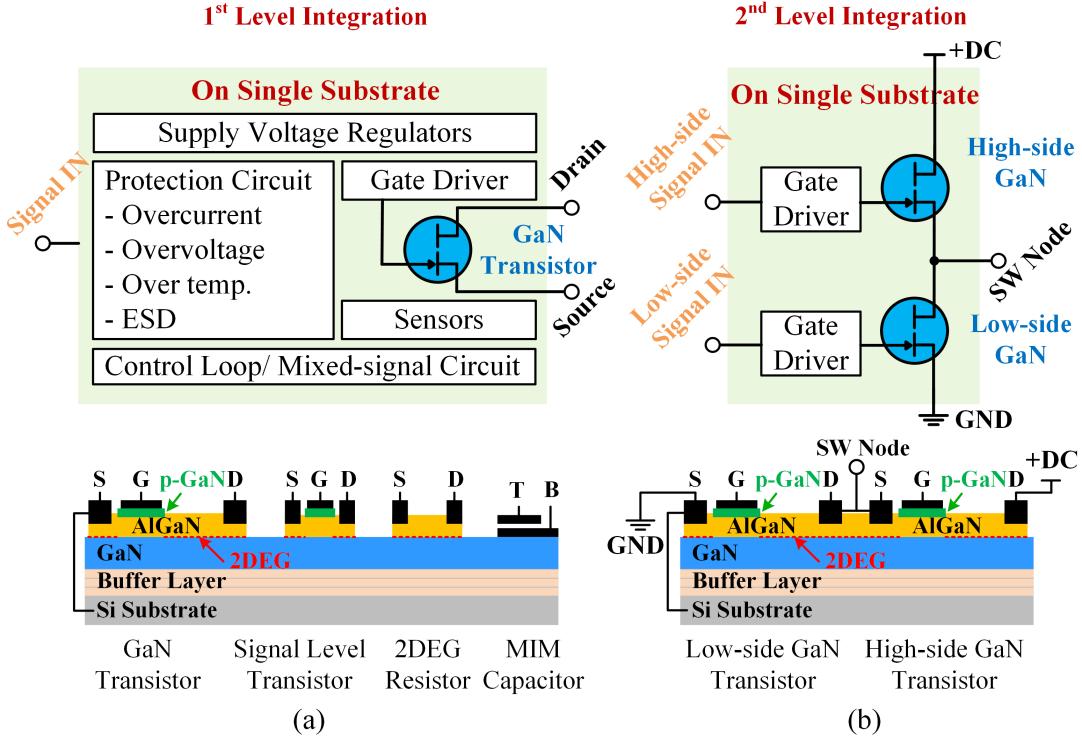
### 1.3 Challenges in Monolithic Integration of Gallium Nitride (GaN)

#### Transistors

Gallium nitride (GaN) transistors show superior figures of merit (FOM) for high voltage (HV) and high frequency (HF) switching applications [33]. To increase power density, smaller passive components and smaller cooling system are preferred, but this requires higher switching frequency and higher efficiency. Due to their small specific output capacitance, GaN transistors enable higher switching speed and higher efficiency for power converters [29, 34, 35]. However, these publications report that due to the high switching speed, the use of discrete GaN FETs introduces severe gate loop and power loop challenges [30].

To achieve more compact and simple-to-use solutions, there is a trend in converter design to integrate semiconductor power devices in a single package in silicon technology [36–38]. In the state-of-the-art e-mode GaN processes with p-GaN gate, a 650 V GaN high-electron mobility transistor (HEMT) is formed by a lateral two dimensional electron gas (2DEG) structure [39, 40]. In contrary to vertical transistor structures (e.g., silicon superjunction and silicon carbide), the lateral nature of the AlGaN/GaN-on-Si technology in combination with the highly-insulating GaN buffer in vertical direction enables the integration of logic and gate driver circuits on a single die, without additional complex assembly steps compared to single devices [41, 42]. Thereby, the gate loop parasitics are minimized, relaxing the challenges for the gate driver. Furthermore, the cost reduction and the increase of reliability are additional driving forces for higher integration levels. Recent advances in semiconductor technology enable even higher level of integration, combining mixed-signal circuits [43], sensors [44], supply voltage generation, control loop, and protection circuit [45] together with gate driver [46]. In [47, 48], GaN converters with integrated drivers from

Navitas Semiconductors are presented, showing reduced gate loop parasitics and also a higher efficiency. To achieve an even more compact system, a buck converter including control loop is integrated into e-mode GaN chip [46], revealing the trend of higher integration level leading to higher efficiency. This single power device level integration is called first-level integration [49], as shown in Fig. 1.5.



**Figure 1.5:** The Scope of the Monolithic GaN Integration and its Cross-section View: (a) 1<sup>st</sup> Level Integration, Including Low Voltage Transistors for Signal Circuits, 2DEG Resistors and Metal-Insulator-Metal (MIM) Capacitors; (b) 2<sup>nd</sup> Level Integration, Two GaN Power Transistors on Single Substrate.

However, the device of the first-level integration can only be used in low side device application. In most HV GaN applications, such as totem-pole PFC [50], LLC [51], and motor drive [52], a phase-leg (two power devices) or even three-phase (six power devices) monolithic integration on one chip is desired. This multiple power devices level integration is defined as second-level high voltage integration [49]. Integrating

high-low side switches on a single conductive substrate is able to minimize not only the gate loop parasitics but also the power loop parasitics. Furthermore, the heatsink can be directly attached to the common substrate without isolation, improving the system thermal design. Therefore, converters with higher efficiency and higher power density can be designed. To achieve second level integration, the phase-leg configuration can be regarded as a basic research object.

The biggest challenge of second-level integration is to solve the issue induced by the substrate voltage bias, either positive or negative [42, 53–55]. High-voltage biases modulate 2DEG channel conductivity and lead to significant on-state resistance ( $R_{dson}$ ) increase. Two mechanisms can comprehensively explain this phenomenon: first, the static degradation with applying a bias voltage at the substrate contact, known as static back-gating effect; second, a dynamic degradation may arise after the substrate bias has been reset to zero. This is due to electrons trapped into the buffer layer during applied bias. After resetting the bias, the captured electrons distort the band diagram and a complete or partial depletion of 2DEG occurs, known as dynamic electron trapping [56]. For discrete devices, the substrate of the device is tied to its source terminal to avoid substrate bias, as proposed by the GaN manufacturer [57]. The voltage potential of the substrate is the same as the source. In other words, the voltage bias of the substrate to the device channel is nearly zero when device is on. However, for the integrated phase-leg, high-low side switches share the same substrate potential. Taking grounded substrate condition as an example, this grounded substrate will typically introduce a dc-link voltage bias for the high side device. When high side switch is on, the voltage potential between the substrate and the channel is dc-link voltage. This substrate voltage bias causes back-gating effect, lifting up the conduction band from the substrate and reducing the 2DEG density [42]. As a result, the  $R_{dson}$  of high side switch degrades, and the conduction loss

increases dramatically. As for the low side switch, the connection type is the same as discrete device. Therefore, the performance of low side switch will not degrade.

Because of the substrate bias effect, a monolithic half-bridge GaN chip composed of two 600 V/20 A GaN HEMTs can only operate up to 200 V under the grounded substrate configuration. It is because the  $R_{dson}$  will have severe degradation if the substrate bias is higher than 200 V, causing severe thermal failure. To mitigate this effect, researchers in [42] investigated different connection of the substrate. This method is to lift up the substrate potential, decreasing the substrate bias amplitude for high side device. In this way, the operating voltage can be boosted to 400V with little  $R_{dson}$  degradation. However, if the operating voltage goes higher, the substrate bias voltage will be bigger than 200 V for both high side and low side switches, leading to severe degradation for both devices. In [58, 59], different capacitor and resistor networks have been inserted between the substrate and the ground to dynamically manipulate the substrate bias. Hence, the voltage can reach 450 V without failure. However, the idea of changing the substrate voltage potential still suffers from the substrate bias effect, sacrificing the device voltage utilization. Moreover, these kind of methods can only be used to validate the failure mechanism, and is not practical. It is because the substrate is normally grounded to avoid additional processing steps. The grounded substrate is also convenient for multi-phase monolithic integration. The state-of-the-art mature solution for second-level monolithic GaN integration is the trench-isolation technology [60, 61]. By etching through the GaN to the  $SiO_2$  buried layer of GaN-on-SOI (silicon-on-insulator), the conductive substrate can be fully isolated. Therefore, the source of high-low side devices can be connected to two substrates independently. This method avoids the substrate bias effect, but the voltage level is limited to 200 V, as demonstrated in GaN manufacture EPC [62, 63]. Moreover, this approach increases switching node capacitance [64] from the buried

oxide, which slightly increases hard-switching losses compared to a discrete device. In addition, the processing steps are complex. In the aspect of material, research in [65] reports that the thicker buffer structure with low defect rates suppresses the substrate bias effect. This is an attractive method for monolithic half-bridge, because no additional processing steps are required. Furthermore, the thicker buffer realizes higher blocking voltage and reduces parasitic capacitance.

For single GaN device, holes injection through p-GaN from drain region has been proved to effectively release the trapped electrons, so that the  $R_{dson}$  degradation is fully eliminated [56]. For the monolithic integrated half-bridge, the trapped electrons are located mainly in source region of the high side device. The work in Chapter 3 addresses the substrate bias effect from the perspective of the gate driver. By injecting additional holes (current) into the device source region through the gate driver, the electrons trapped in the buffer layer can be partially released, and the  $R_{dson}$  degradation is mitigated. Moreover, based on the mechanisms, this work found that there are different  $R_{dson}$  degradation phenomena for hard-switching and soft-switching scenarios. The timing and amount of additional holes (current) injection strategies should be different under hard-switching and soft-switching conditions.

#### 1.4 Challenges in Series-connected WBG Devices

Now SiC MOSFETs are expected to replace Si IGBT in power electronic applications because of its supreme characteristics [8]. However, the highest voltage rating of commercial SiC MOSFETs is 3.3 kV. For medium and high voltage applications, SiC MOSFETs with higher voltage rating, from 5 kV to 20 kV, are preferred because high voltage rating device helps reducing system complexity and increasing system power density [66].

There are two choices to get a high voltage rating device pack: 1. A single

device with high breakdown voltage by semiconductor design; 2. A series-connected string of low voltage devices. For a single SiC MOSFET, 10 kV and 15 kV voltage rating device can be fabricated [66, 67]. However, the lower voltage SiC MOSFET, such as 900 V, 1.2 kV and 1.7 kV device, has more mature technology and lower cost. Therefore, series-connected string of low voltage devices is a technology-ready and economic way to form a high voltage rating device. Besides, a series-connected string of SiC MOSFETs has following benefits over a single SiC MOSFET at the same breakdown voltage [68]: (1) Lower voltage derating rate; (2) Lower  $R_{dson}$  per unit voltage; (3) Higher current rating per unit die area. These benefits significantly improve the device pack performance on power loss, voltage rating and current rating.

The biggest challenge of series-connected devices is the drain-source voltage ( $V_{ds}$ ) sharing [69]. Each device has the same  $V_{ds}$  at steady state as well as during switching transient. Otherwise, at least one device of the series-connected string will encounter overvoltage. The causes of unequal voltage sharing can be summarized: 1. Gate driving loop difference, including gate signal delay variance caused by gate driver isolation [70] and gate loop component difference [71] (gate resistor, gate parasitic inductor, etc.); 2. Power loop parasitic parameters difference, including gate/drain/source terminals to ground parasitic capacitance difference [70, 72–75]; 3. Device part-to-part parameter spread caused by fabrication process [74, 76], such as parasitic capacitance ( $C_{iss}$ ,  $C_{oss}$  and  $C_{rss}$ ), anti-parallel diode parameters and gate threshold voltage.

The state-of-the-art to address this challenge is discussed as follows:

- A. Snubber vs. Snubberless: A common solution is to add snubber circuit, which has been used by ABB [69], Siemens [77] and GE [78]. The snubber circuit is simple and reliable, but it introduces additional loss [79]. Therefore, small snubber or even snubberless circuit is desired. However, the concept of snubberless [80, 81] is proposed if the active control is implemented because the device

voltage balancing be actively controlled by the gate signals.

B. Active Control vs. Non-active Control: The active control involves  $V_{ds}$  feedback control loop. There are mainly two problems: Firstly, if the feedback loop involves central controller [72, 75, 82, 83], the feedback signals are transmitted through the high voltage isolation barriers. Since the devices in a serial string are not on the same potential, the different isolation levels will lead to different signal delays. These delays may not be sensitive in IGBT case, but it will make big difference for fast switched SiC MOSFETs. Secondly, even though local closed-loop control [70, 71, 74, 84] is achieved, the control bandwidth is still not high enough to control the  $dv/dt$  at the  $V_{ds}$  rising/falling edge. It takes several switching cycles to achieve equal voltage sharing [70]. Thus, the initial condition is the same as uncontrolled case. The snubber circuit or active clamping circuit should be designed under uncontrolled case. The best idea is to make gate voltages ( $V_{gs}$ ) highly-synchronized under uncontrolled condition and to use closed-loop control to micro-tune the devices' difference. In other word, if the gate loop difference can be eliminated under uncontrolled condition, the snubber circuit can be designed only for the power loop difference. Thus, before feedback control takes effect, the  $V_{ds}$  difference is already small, and the snubber circuit can be tiny and have low loss. If the active control has high dynamic response and high resolution for the WBG devices, the snubber can be eliminated, further improving the efficiency.

C. Voltage Source Gate Driver (VS-GD) vs. Current Source Gate Driver (CS-GD):

To achieve synchronized  $V_{gs}$ , CS-GD basically has three benefits over VS-GD:

C1. Linear  $V_{gs}$ .

The  $V_{gs}$  of VS-GD is hard to be synchronized because of its nonlinear rising/-

falling slope. The constant gate current of CS-GD leads to a constant  $V_{gs}$  change rate [85], which is easy to control.

### C2. Miller Current Compensation.

A miller plateau of  $V_{gs}$  is caused by  $V_{ds} dv/dt$  induced miller current [10]. In the application of SiC MOSFETs with excessive  $V_{ds} dv/dt$ , this miller plateau can turn into a voltage trap [86]. The gate current of VS-GD changes nonlinearly from high to low. At the miller plateau region, there is not enough gate current to compensate the miller current. The  $V_{gs}$  will drop significantly, and the device may be turned off by mistake. This miller current distortion makes  $V_{gs}$  even harder to be synchronized. The CS-GD has the constant and sufficient gate current to compensate or even completely cancel out the miller current.

### C3. Sensitivity to Gate Loop Components' Variance.

The gate current of VS-GD depends on the supply voltage and the components on the gate path. The gate currents of VS-GD can be very different if there is difference of gate loop parameters including gate resistance and parasitic inductance [87]. The gate current of CS-GD is constant and immune to the gate resistance variance. Although the gate loop parasitic inductor delays the rising/falling edges of current pulse, it does not influence the amplitude of pulse current. The time of the current pulse edge is within 10 ns, and the impact is negligible compared with the current pulse length (hundreds of ns). In summary, CS-GD is better than VS-GD in terms of sensitivity to gate loop differences, and  $V_{gs}$  of CS-GD is easier to be synchronized.

This dissertation proposes two versions of current source gate drivers for series-connected WBG devices. First version is an open-loop current source gate driver with novel gate driver structure. Different from VS-GD, where the control signals

and the power supply have separate isolation barriers, the proposed CS-GD adopts a unique current pulse to carry both control information and power. The current pulse is generated by a current source inverter (CSI) at primary side and is equally split by a multi-winding transformer to each channel of SiC MOSFETs. This novel driver structure uses multi-winding transformer to guarantee the homogeneous gate current of each channel. Because the transformer cannot clamp the gate voltage, and it will provide discharging path for  $C_{gs}$  of the SiC MOSFET, a secondary auxiliary circuit is necessary. By implementing a self-driving secondary circuit, high voltage isolated gate signals for auxiliary switches are avoided. Hence, all the control signals are at the primary side with common ground. The channel-to-channel propagation delay difference, caused by different isolation levels, is eliminated. Due to the highly synchronized  $V_{gs}$  of the proposed CS-GD, only a tiny snubber circuit is needed to compensate for the power loop difference and device part-to-part tolerance. The first version of CS-GD successfully verifies that the CS-GD is better in terms of achieving synchronized gate voltages. However, although the gate voltage is highly synchronized, it is found that the device terminal to ground parasitic capacitance is a major factor of unequal voltage sharing. It is because the junction capacitance of WBG devices is comparable to the parasitic capacitance. The parasitic capacitance of each serial device is different due to different device positions. Thus, the equivalent capacitance of each device will be different. To improve the reliability of the series-connected switches, the gate driver with active voltage balancing function is preferred. Thus, second version current mirror based CS-GD is proposed. Because the voltage balancing is achieved by actively adjusting the gate current of each serial channel, the multi-winding transformer for equally shared gate current is no longer necessary. Due to the high dynamic response of current mirror, the second version of CS-GD can flexibly adjust the current amplitude, pulse width and delay time with very high

bandwidth. Without the multi-winding transformer, the size of current source gate driver is comparable to the commercial VS-GD. Compared with VS-GD, the second version of CS-GD has more control freedoms, thus, easier to achieve voltage balancing at both soft-switching scenario and hard-switching scenario.

Another major challenge of series-connected devices is the reliability issue [72], the complete protection functions should be implemented to guarantee the reliable operation of the converter system. For the single SiC MOSFET, the protection functions have been widely investigated by researchers in terms of overcurrent/short-circuit protection [88, 89], gate overvoltage/undervoltage protection [90–92], and crosstalk suppression [86]. For series-connected SiC MOSFETs, the protection functions can be directly borrowed except for the short-circuit (SC) protection. Besides the traditional SC scenarios, there are unique SC scenarios: short-circuit and open-circuit of a single device among the series-connected string. Take the phase-leg configuration as an example, for the single device application, the short-circuit of one device usually results in shoot-through of the phase-leg when the complimentary switch turns on. This will cause severe overcurrent. Unlike the single device short-circuit, the short-circuit of one device among the series-connected string may not cause shoot-through of the phase leg. It is because the other devices in the series-connected string are still off to block the dc-link voltage. In this case, the ( $V_{ds}$ ) of the short-circuit device is zero, and the voltage across other devices will increase, which may cause overvoltage failure of these devices. The transient voltage suppressor (TVS) is commonly implemented in parallel with each series-connected SiC MOSFETs to avoid overvoltage failure. However, monitoring each device in the serial string is still necessary. It is because by monitoring the single device voltage, the single device failure can be detected. Compared with single device applications, where a single device open-circuit will not cause severe problems, the open-circuit of a single device in the serial string

may lead to severe destructions. It is because the voltage rating of a single device is usually smaller than the dc-link voltage in the application of the series-connected devices. Therefore, the open-circuit of a single device among a serial string should also be protected timely. Since open-circuit of a single device is short-circuited by the TVS diode, the open-circuit of single device also belongs to short-circuit fault in this article. To sum, both short-circuit and open-circuit of a single device in the serial string should be taken into consideration. For series-connected devices, the SC scenarios are complicated and numerous. In order not to neglect any SC scenario, a systematic analysis method is proposed.

The SC withstand time (SCWT) for the SiC MOSFETs is within microsecond ( $\mu\text{s}$ ) level [93], which is much shorter than that of Si-based devices. Therefore, the short-circuit protection for SiC MOSFETs should be fast enough to finish within SCWT. On the one hand, researchers are trying to reduce the response time of the protection circuit. However, short dynamic response time may reduce the noise immunity capability. Moreover, the response time is limited by the hardware components and cannot be reduced indefinitely. On the other hand, some works try to increase the SCWT. Previous work has found that the SCWT is related to  $V_{\text{ds}}$ ,  $V_{\text{gs}}$  and operating temperature [94, 95]. In order to increase SCWT, works in [88, 89] have proposed that when the short-circuit fault is detected,  $V_{\text{gs}}$  can be quickly reduced first to increase the SCWT, providing sufficient time for the subsequent action. This method is also called two-level turn off (2LTO) [88].

There are basically two steps for the fault protection. First step is to detect the fault based on the fault indicator. Second step is to take actions to safely terminate the fault. For the action of short-circuit fault, the 2LTO mentioned above is a useful strategy if the response time of the protection circuit is low. Besides, the soft turn-off is widely implemented to avoid huge current and voltage oscillations

[95]. For the detection of short-circuit fault of a single device, five short-circuit indicators, temperature, dc-link voltage dip, drain-source current, gate charge and  $V_{ds}$  saturation voltage, have been reported. Infineon has proposed a temperature triggered zener diode for short-circuit protection of Si devices [96]. The short-circuit induced temperature rise can make the embedded zener diode clamps the gate voltage ( $V_{gs}$ ) to a lower level, thus, the SCWT increases, leaving a sufficient time for the turn-off response. However, the response time of this temperature indicated method is in millisecond level, which is not suitable for the short-circuit of SiC MOSFETs. Researchers in OSU [88] utilize the abrupt dc-link voltage dip to detect the SC, achieving  $< 100$  ns detection time. However, this method is very sensitive to the dc loop parasitic parameters. Some research groups directly measure the drain-source current ( $I_{ds}$ ) for the short-circuit fault, such as Rogowski coil [89], current transformer [97], embedded current mirror [98], etc.. However, the current mirror suffers from the mirror tolerance and needs to modify the semiconductor internally. The embedded Rogowski coil and current transformer can achieve high bandwidth and high  $dv/dt$  immunity, but it is limited by the package of the SiC module. Moreover, the failure of single device among series-connected string may not cause overcurrent. Therefore, these current sensing based protection methods cannot cover all the SC scenarios of series-connected devices. Gate charge detection method [99] has been proposed to detect the SC, which avoids high voltage ( $V_{ds}$ ) and high current ( $I_{ds}$ ) measurement. Moreover, its integration circuit leads to high noise immunity. However, this method can only detect the SC during the turn-on transient. The most common and reliable short-circuit detection method is desaturation protection (DeSat). This method monitors the  $V_{ds}$  at the on state. If the  $I_{ds}$  is high, the  $V_{ds}$  voltage drop will become high and trigger the DeSat. Paper [89, 94] has been reported that the short-circuit fault can be protected within hundred ns using DeSat method. The simplicity, experience,

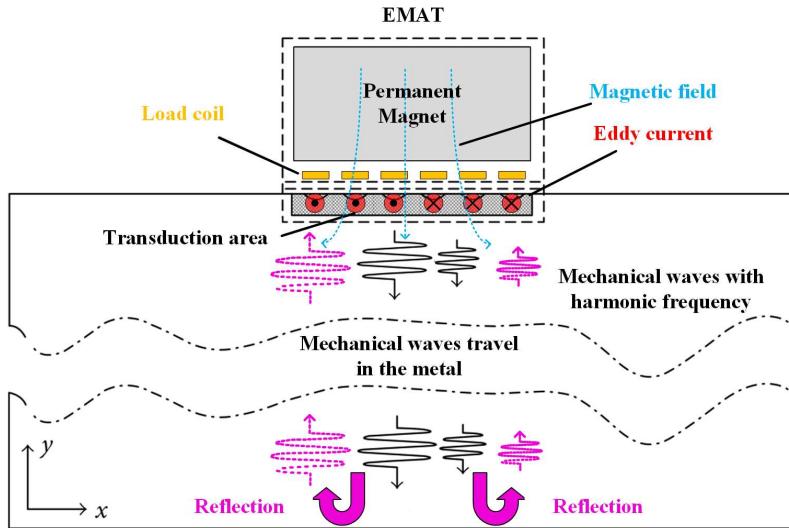
and familiarity with the DeSat solution make it popular even in the SiC MOSFET applications. Yet, ambiguity about its proper utilization still exists, and none of the references cover its performance in all types of the SC in a half-bridge module of series-connected SiC MOSFETs.

The above mentioned detection methods are for a single device short-circuit, in which overcurrent will occur during the on-state of the device. However, the overcurrent phenomenon will not occur under some SC scenarios of series-connected devices. Therefore, these methods cannot be directly implemented for the series-connected devices. For the SC detection of a single device in the series-connected string, one straightforward method is to monitor the  $V_{ds}$  voltage during off state. If the  $V_{ds}$  of one device is too low, this device is regarded as short-circuit. However, this detection method is likely to be mis-triggered, because the low voltage may also result from the unbalanced voltage sharing of the series-connected devices at transient period. In Chapter 4, the DeSat method is improved to detect the short-circuit of a single device in the serial string during the off state. Meanwhile, the original overcurrent short-circuit protection of DeSat is retained. By implementing the DeSat circuit at both on and off state, two above mentioned short-circuit cases can be detected. After the detection, the turn-off action should be synchronized for each series-connected device to avoid unbalanced voltage sharing issue. Therefore, the command of the turn-off action should be generated by the primary side.

In this dissertation, a short-circuit protection method is proposed to cover all the SC scenarios of series-connected SiC MOSFETs. This SC protection circuit is integrated in the proposed current mirror based gate driver. Thus, the proposed smart current source gate driver can achieve both voltage balancing and SC protection for the series-connected devices.

## 1.5 A Practical Design Example of WBG Based Converter: Burst Mode Inverter

Pulse power supply (pulser) is widely used in industrial applications, such as sensor power supply, laser generator, x-ray and MARX, etc. The design consideration of the pulser is different from the power supply under continuous operation. Specific to the sensor power supply, the priority is to achieve good performance, including sensing accuracy and measurement range. There are some restrictions on power density and thermal stress, but they are not priority.



**Figure 1.6:** Principle of EMAT Sensor.

To measure thickness of the metal in a non-contact manner is required in many industrial areas, such as pipeline in-service defect inspection [100], flaw detection in steel products and railroad inspection, etc [101]. Electro-Magnetic Acoustic Transducer (EMAT) sensing technology [102, 103] is a competitive candidate for this thickness measurement application. An EMAT induces ultrasonic waves into a test object through two interacting magnetic fields. A high frequency (ultrasonic frequency) field

generated by electrical coil induces eddy current in the metal and interacts with a static field generated by permanent magnet. This interaction generates high frequency Lorentz forces that further cause mechanical vibration in the metal. This mechanical vibration causes ultrasonic waves to propagate in the metal and be reflected back by the metal surface. After the echo is reflected back, the transmitting coil also serves as a receiving coil to capture the echo induced magnetic field, thereby the thickness can be calculated. The principle of this EMAT sensor is shown in Fig. 1.6. To receive strong echo signals, the voltage and current in the high frequency coil should be sufficient to generate strong Lorentz forces. Meanwhile, the frequency should be in the megahertz range because a higher frequency ensures less attenuation of ultrasonic waves [104]. Therefore, an ultrahigh frequency (megahertz) high voltage ( $> 800$  V) AC power supply is required to supply the coil, and it should operate in burst mode with low repetitive frequency (hundred hertz). In this way, the transmitting signals and echo signals can be differentiated. Moreover, the coil current and voltage should be sinusoidal with low THD. This is because high THD causes a series of high frequency harmonics and excites different frequency ultrasonic waves with different traveling speed in the metal. Thus, the echoes will arrive at different time, affecting the measurement accuracy.

One of the challenges faced by the EMAT pulser is to achieve high voltage and high frequency simultaneously. In the pulser application, MARX generator with solid state switches is widely used [105, 106]. It basically charges capacitors in parallel and discharges them in series to elevate the output voltage. Some improved topologies can achieve narrow pulses [107–109]. However, the equivalent pulse frequency cannot reach the megahertz level, and the circuit is very complicated, with five or higher number of stages. Moreover, these MARXs cannot produce the sinusoidal output voltage, which is a critical requirement for EMAT power supply. Additional-

ly, the overvoltage and overcurrent protection of MARX is very complicated, which also brings obstacles to its application on EMAT sensors with harsh environments and difficult maintenance [110–112]. The simplest and most reliable topology of the inverter is the H-bridge. However, conventional Si IGBTs and Si MOSFETs cannot switch at megahertz and kilovolt to complete the required conversion. Si MOSFETs at megahertz switching frequency can only withstand a few hundred volts. Si IGBTs above 1 kV can only sustain a switching frequency of several kilohertz, limited by low switching speed and high switching loss [8]. Therefore, the state-of-the-art solution of EMAT power supply adopts a three-stage design: a low-to-intermediate voltage step-up DC/DC converter (e.g., 24 V to 200 V), a full bridge inverter based on Si MOSFETs, and a high-frequency pulse transformer boosting the voltage to the target (e.g.,  $\pm 800\text{V}$ ) [113]. Due to the resonance between transformer parasitic capacitance and load coil inductance, this topology suffers from high THD on the AC output side. Now, SiC MOSFETs can operate at megahertz and kilovolt because its switching speed is 10 times faster than Si MOSFETs [8, 114], eliminating the high-frequency pulse transformer and simplifying the system into two stages: DC/DC boost stage and inverter stage. Moreover, the resonant filter has been implemented at the inverter output to achieve better THD.

Another challenge of this pulser is the wide range of the load variation. To cope with the wide load range, existing solutions are from two aspects: modulation and filter topology. Previous work proposed variable frequency control [115], dual mode control [116] and asymmetrical PWM control [117, 118] to achieve high efficiency and ZVS in the wide load range. However, these modulation methods require closed-loop control, which will increase system complexity. Other research focused on the filter topology. By adding resonant elements to existing resonant filters, many additional functions can be obtained, such as notch filter for specific order harmonics amplifi-

cation and suppression [119, 120], variable resonant elements for different operating condition [121], and multi-element filters for better filter characteristics [122, 123]. However, these methods require additional resonant elements. In EMAT sensor application, the load is the combination of a fixed coil and a variable metal. The model of the load is a variable inductor in series with a variable resistor. It is because the thickness and material of the testing metal can be different, which changes the equivalent core of the inductor. In addition, mechanical waves have energy loss when propagating, and the eddy currents also induce power loss. Therefore, an equivalent resistor is used to model the power loss. Under such a large load variation, low THD of the output voltage should be guaranteed to ensure the accuracy. Meanwhile, the zero-voltage soft-switching (ZVS) [124] should be implemented for reliability consideration. Therefore, a resonant filter for inductive loads should be designed to meet specific requirements. The voltage gain curve is a common tool in the filter analysis, which is based on First Harmonic Approximation (FHA) method [125, 126]. However, this method is based on resistive load condition, which is not practical in many non-resistive load applications. It is because the impedance of the inductive or capacitive load changes with the frequency. Thus, the Q factor cannot be fixed. In this dissertation, a modified Q factor method is proposed, extending the gain curve analysis to the non-resistive load condition. Moreover, the design considerations of the resonant components in the burst mode are different from the continuous mode. The special design considerations for the pulse filter components are demonstrated in this dissertation.

Next challenge of the pulser is the start-up and ending transient of the pulses. The start-up and ending transient under burst mode happens every repetitive time period. For the start-up transient, the output filter is at zero state. At each burst operation, the first one or two pulses are used to charge the filter to a steady state.

The output voltage amplitude of the initial pulse is smaller than that of the following pulses. This effect makes the first one or two pulses invalid, because it cannot excite enough magnetic force. For the pulse ending transient, the filter residual energy circulates with the load, so that the load voltage cannot be immediately reduced to zero. When the oscillation exists in the coil, the coil cannot receive effective echo signals. This oscillation time is called blank time. The blank time actually represents the minimum thickness measurement capability of EMAT sensor. Therefore, it is important to minimize the oscillation duration after the pulses. In [127, 128], the state-trajectory analysis is used to derive the switching patterns for fast settling the state variables of the resonant filter to the optimal steady state condition. By optimizing the first pulse width, the state variables are settled to the steady state trajectory in the minimal time. However, the duration of the first pulse needs to be fine-tuned, and may vary depending on the filter parameters and load conditions [129, 130]. Considering reliability and cost, sensing and closed-loop control are not feasible for this industrial application. This dissertation uses transient state analysis to propose a new start-up method, which pre-charges the filter tank to a state close to the final steady state. Since there is not additional hardware and pre-charge timing issue, it can be open-loop and much convenient.

The last challenge is the extraction of echo signals. Because the transmitting and receiving signals are in the same coil, the transmitting signal are kilovolt (kV) level while the receiving echo signals are only microvolt ( $\mu$ V)) level. Therefore, the voltage level of transmitting signal is supposed to be curtailed to the level of receiving signals. How to scale down the high voltage transmitting signal while maintaining the weak receiving signal is a big challenge for the receiving circuit. Moreover, when the transmitting signal is scaled down, the time delay should be minimized, because the time delay will affect the accuracy of the measured time interval. A unit using

depletion MOSFET has been presented in [131, 132] to block the high voltage. When the applied voltage is high, the depletion MOSFET works in saturation region. No matter what the applied high voltage signal is, the circuit will output a constant low current. However, this circuit is unipolar and can only block dc voltage. In this dissertation, a bipolar isolated signal conditioning circuit is designed to scale down the high voltage transmitting signals and amplify the subtle receiving signals.

This dissertation uses the design example of pulser inverter to illustrate the issues that need to be considered in the WBG based converter design. These issues include EMI, crosstalk, high frequency magnetics and resonant tank design.

## 1.6 Dissertation Outline

As discussed above, the philosophy of replacing conventional Si devices with WBG devices is an ongoing trend. However, realizing the full potential of WBG semiconductor devices is very challenging due to its high slew rates and high sensitivity to the parasitics. This dissertation investigates some of the tricky challenges while designing a WBG based converter. Afterwards, a SiC MOSFETs based inverter is designed to illustrate the design considerations of WBG based converters. This dissertation is organized as follows.

Chapter 2 investigates the crosstalk effect and introduces a smart self-driving multi-level gate driver (SMGD) to suppress the crosstalk issue. Using original  $V_{gs}$  with simple RC delay as control signal of the auxiliary circuit, the proposed SMGD has following advantages over the other crosstalk suppression techniques: 1. No additional control signals; 2. No additional DC/DC power supply and signal isolation stages for the auxiliary switch; 3. Easy to be implemented on the commercial gate driver IC. A SMGD based on the commercial gate driver ADuM4135 is developed.

Chapter 3 investigates the state-of-the-art monolithic GaN HEMTs integration.

Due to the lateral structure of GaN HEMTs, the integration of power switches, protection circuit, gate driver and logic circuit is convenient. However, the integration of power switches is challenging. It is because the channel of the high-side switch is floating. The voltage bias between substrate and high-side channel significantly impacts the channel conductivity. To address this issue, several methods are investigated, including substrate bias manipulation, passive components insertion between substrate and ground, and current injection from gate. Finally, a three level gate driver is implemented to significantly improve the conductivity of the high side channel.

Chapter 4 investigates the voltage balancing issue and the short-circuit protection issue of series-connected SiC MOSFETs. A current mirror based current source gate driver with active control scheme is proposed to address these two issues. Due to the high dynamic response of mirror based current source gate driver, the voltage balancing issue under both soft-switching scenario and hard-switching scenario is solved properly. The short-circuit scenarios of series-connected devices are investigated. Besides the traditional high-inductance and low-inductance short-circuit scenarios, the failure of single device among the serial devices can also cause overcurrent or over-voltage failure of the serial string. The proposed short-circuit protection method can cover all the short-circuit scenarios of series-connected devices. The proposed short-circuit scheme is implemented in the proposed current source gate driver with soft turn-off function. The response time of the proposed short-circuit protection method is within 300 ns, which is sufficient to protect the high speed WBG device string.

Chapter 5 presents a design example of WBG based converters. The resonant tank design methodology is illustrated. Moreover, the practical design considerations of capacitors and inductors in the WBG converter are discussed. A practical transient state equation analysis method is proposed to cope with the start-up and ending transient issues of WBG based inverter. Compared to the state-of-the-art pulse inverter,

the designed inverter has low output THD with higher power density and smaller box volume. The crosstalk, EMI, fault protection, PCB layout of gate loop and power loop and other engineering design considerations are also included.

Conclusions and future work are given in Chapter 6.

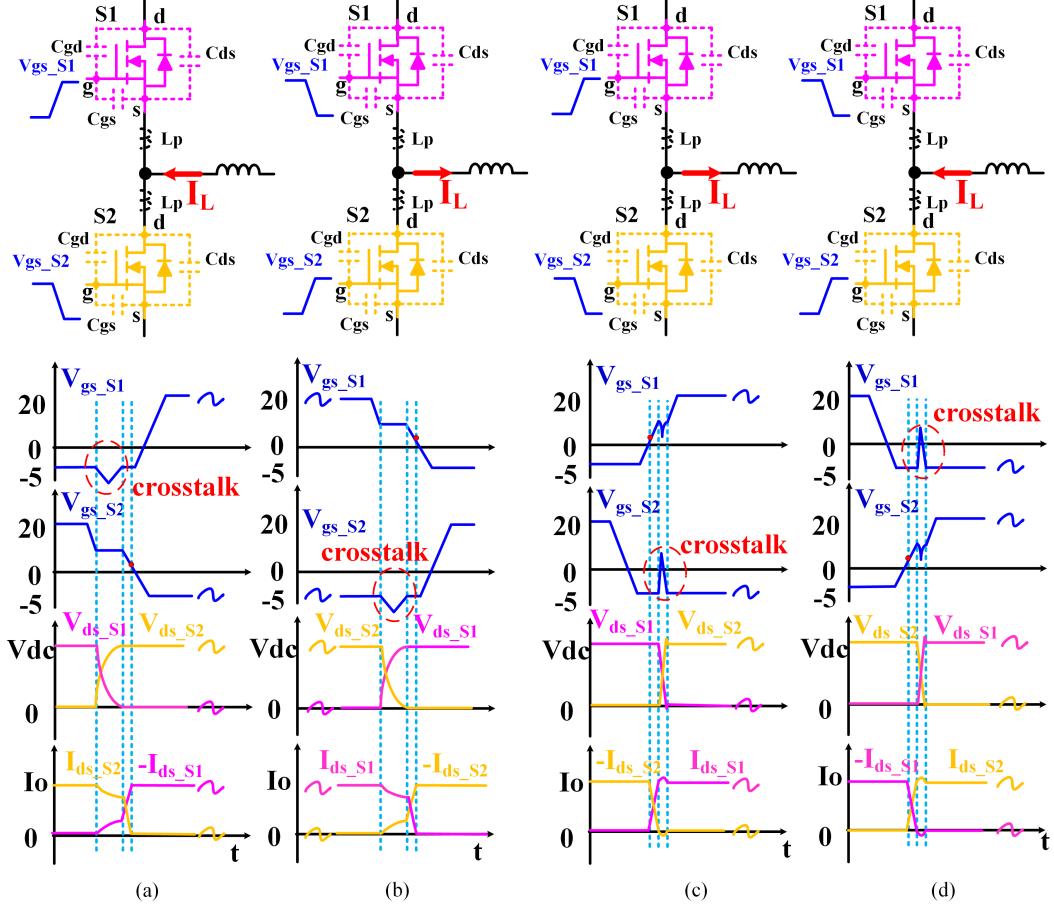
## Chapter 2

# SMART MULTI-LEVEL GATE DRIVER FOR FAST SWITCHING AND CROSSTALK SUPPRESSION

In this chapter, the switching transient typical waveforms in a phase-leg configuration is analyzed and the root cause of the crosstalk effect is discussed. Based on the analysis, the proposed smart self-driving multi-level gate driver is illustrated in detail. By applying variable gate voltage through auxiliary circuit, the crosstalk problem can be mitigated. Using the original gate-source voltage as auxiliary circuit driving signal, the gate driver does not introduce any extra control signals, which avoids additional signal/power isolation barriers and makes the auxiliary circuit very convenient to be implemented on the existing commercial gate driver. After that, the design guideline of the proposed gate driver for SiC MOSFETs application is demonstrated. Finally, the proposed gate driver is validated by experiments and its performance is evaluated in detail.

### 2.1 Switching Transient Analysis in a Phase-leg and Root Cause of Crosstalk

Fig. 2.1 shows the typical switching transient waveforms in a phase-leg configuration. The crosstalk happens at the device  $V_{ds} dv/dt$  transient and causes distortion on the device  $V_{gs}$ . The  $V_{ds} dv/dt$  can generate current flow (miller current) between MOSFET drain and gate through the gate-power loop coupling capacitor  $C_{gd}$ . At turn-off, the miller current caused by the positive  $dv/dt$  tries to charge the  $C_{gs}$ . At turn-on, the miller current caused by the negative  $dv/dt$  tries to discharge the  $C_{gs}$ . Looking at one on/off transient of a phase leg, if the load current helps to charge the



**Figure 2.1:**  $V_{gs}$ ,  $V_{ds}$  and  $I_{ds}$  Waveforms When (a) (b) Load Current Helps to Charge the  $C_{ds}$  of Turn-off Device and Discharge the  $C_{ds}$  of the Complimentary Device in the Deadtime (ZVS Soft-Switching); (c)(d) Load Current Does Not Help Building Up the Device  $V_{ds}$  Voltage in Deadtime (Hard-Switching).

$C_{ds}$  of the turn-off device and discharge the complimentary device during deadtime, the  $V_{ds} \frac{dv}{dt}$  of both devices will start at the turn-off signal and will complete during deadtime. This  $\frac{dv}{dt}$  caused miller current elevates the  $V_{gs}$  of the turn-off device and causes the turn-off miller plateau. Meanwhile, it pulls down the complimentary switch's  $V_{gs}$  which is still at the off state. Thus, overvoltage breakdown may happen to the device gate. This is typically the ZVS soft-switching case, as shown in Fig. 2.1(a)(b). In contrast, if the load current direction is from source to drain of the turning off device, a much larger  $V_{ds} \frac{dv}{dt}$  is forced to happen during the turn-on

device  $V_{gs}$  rising edge in the deadtime zone, which elevates the  $V_{gs}$  of the off device at a large amplitude and may cause mis-trigger to the device. The  $V_{ds} dv/dt$  also pulls down the  $V_{gs}$  of the complimentary device during its rising-up to delay the turn-on process (turn-on miller plateau). This case is shown in Fig. 2.1(c)(d), which is the turn-on and turn-off typical waveforms of hard-switching. For the SPWM and double pulse test, the waveforms of a phase-leg can be (a)(d) or (b)(c) depending the load current direction.

## 2.2 Proposed Suppression Method for Crosstalk Effect

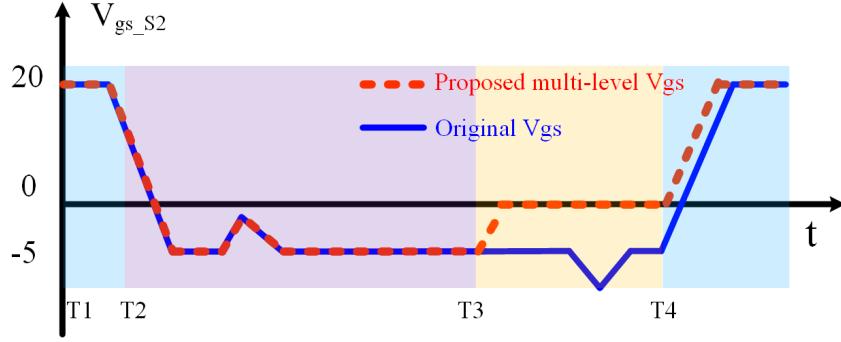
To mitigate the risk of gate mis-triggering caused by  $V_{ds}$  positive  $dv/dt$ , one effective method is to bring the off-state gate voltage to a negative level. However, this will take the  $V_{gs}$  negative overshoot to a more negative level thus exposes the gate to higher risk of negative over-voltage breakdown.

Many gate driver companies [22, 24, 25, 133, 134] and papers [9, 32, 135] suggest using clamping strategies:

1. Use Zener diode to directly clamp  $V_{gs}$  between +20 V and -5 V;
2. Use two Schottky diodes to directly connect the MOSFET gate to power supply voltage +20V/-5V to limit  $V_{gs}$  in the range of -5 V to 20 V.

Because the dynamic response of Schottky diode is faster than that of Zener diode, the Schottky diode clamping is more effective than Zener diode clamping, but still, the Schottky diode clamping performance is limited by its dynamic response and diode current rating [9, 24, 25, 133]. Moreover, the parasitic inductance on the Schottky diode clamping path will affect the clamping result. As a result, usually the voltage overshooting can be alleviated to a certain extent by using Schottky diode clamping strategy, but it cannot guarantee the device is safe from overvoltage breakdown.

Therefore, a more effective strategy is to keep the gate voltage at an adequate negative level when the gate positive spike (possible mis-trigger) happens and pull up the gate voltage to a less negative level before the gate negative overshooting event. This requires a multi-level gate voltage at off state.

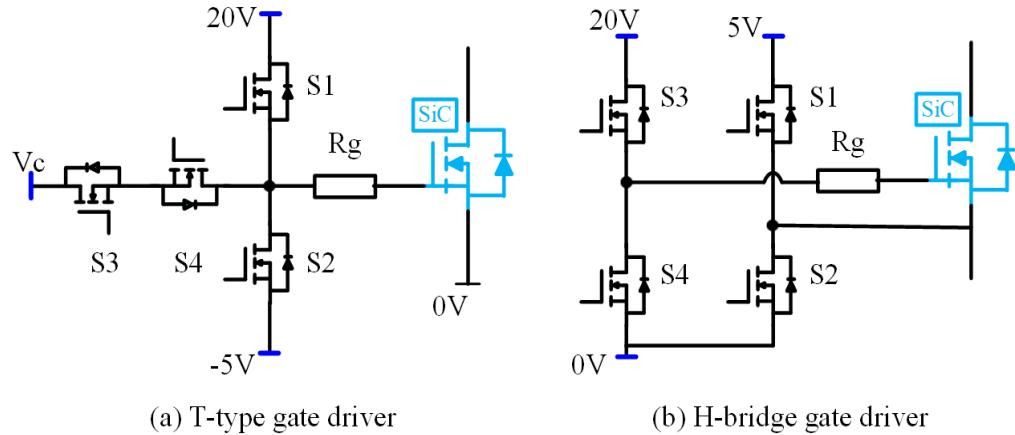


**Figure 2.2:** Proposed Gate Voltage Waveform for Crosstalk Suppression.

As shown in Fig. 2.2, the proposed crosstalk suppression method (red dotted line) brings up the gate voltage to 0V and clamps it at 0V after the mis-triggering period ( $T_2-T_3$ ) and before the turn-on signal comes ( $T_4$ ), making negative overshooting ride on 0V level ( $T_3-T_4$ ). Therefore, the risk of negative breakdown is significantly mitigated. The proposed gate driver circuit achieves this goal with minimum number of auxiliary devices and a very simple passive circuit.

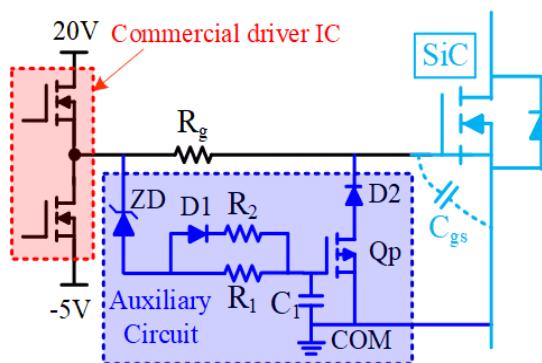
### 2.3 Operation Principle of Proposed Smart Self-driving Voltage Source Gate Driver

The commonly used voltage source gate driving circuit for SiC MOSFET consists of three components (non-bootstrap type): one isolated gate driver IC for signal amplification and signal isolation, one isolated DC/DC power converter for supplying gate driving power and on/off gate resistors to limit the maximum gate driving current and adjust the switching speed.



**Figure 2.3:** State-of-the-art Three-level Gate Driver Topologies.

To implement the three-level gate driver, one easy way is to use the three-level circuit topology, such as H-bridge and single-phase T-type, as shown in Fig. 2.3, to connect three levels of power supply voltage to the gate. However, the devices themselves in these circuit need gate driver circuits. Moreover, all these gate driver circuits require three parts: isolated gate signal, isolated gate power supply and gate resistors. It not only adds many extra components to the circuit, but also introduces additional high voltage isolation barriers which can lead to complex common mode current path and distort the gate signal in an unpredictable way.



**Figure 2.4:** Proposed Three-level Gate Driver Schematic for Crosstalk Suppression.

In order to overcome these drawbacks, the key is to utilize the existing gate signal

and gate power supply to drive the auxiliary switch. The proposed gate driver is a highly cost-effective and compact self-driving three level gate driver, as shown in the blue part of Fig. 2.4. To create a zero-level gate voltage during the off-state, an active switch  $Q_p$  is used to connect the gate and source; whenever the zero voltage level is needed, it can be turned on to clamp the gate voltage to 0V. Originally it needs an additional gate driver circuit, but this can be avoided if the original gate driver output off-state voltage can be utilized to drive this switch. The gate driver IC output voltage at off-state cannot be directly used since the zero clamping does not happen at the same moment of the off signal, however, the off-state gate voltage can be delayed with a RC circuit to drive the active switch  $Q_p$  as long as  $Q_p$  is a P-channel MOSFET. The RC time constant can be designed to guarantee the  $Q_p$  is triggered after the gate positive overshooting period. The operation of  $Q_p$  is supposed to be active only during the off-state, which cannot be simply achieved by this RC circuit. Whenever the  $V_{gs}$  is positive,  $Q_p$  should be turned off, therefore, a series-connected diode is needed to block the positive gate voltage as well as the reverse conduction of the  $Q_p$  body diode. Under this condition, in order to turn off the  $Q_p$ , an adequate positive voltage should be applied on the gate of  $Q_p$ . Since the gate of  $Q_p$  is connected to the gate driver IC output, which at this moment outputs a positive high voltage (e.g. 20V, 18V etc.), a component is necessary on the  $Q_p$  gate path to reduce this high voltage to a proper value to protect the  $Q_p$  from gate overvoltage breakdown. Besides, this component should not affect the off-state negative gate voltage. A Zener diode is suitable to achieve this goal. Therefore, the complete auxiliary circuit is constructed, as shown in the dark blue block of Fig. 2.4. The auxiliary circuit consists of two parts: the first part is the SiC MOSFET gate-source clamping circuit - the Schottky diode  $D_2$  and auxiliary switch  $Q_p$  in series connection. The second part is the RC delay circuit connected to gate driver IC output port to generate the control signal

for the auxiliary switch  $Q_p$ . The labels' corresponding components are listed in Table 2.1.

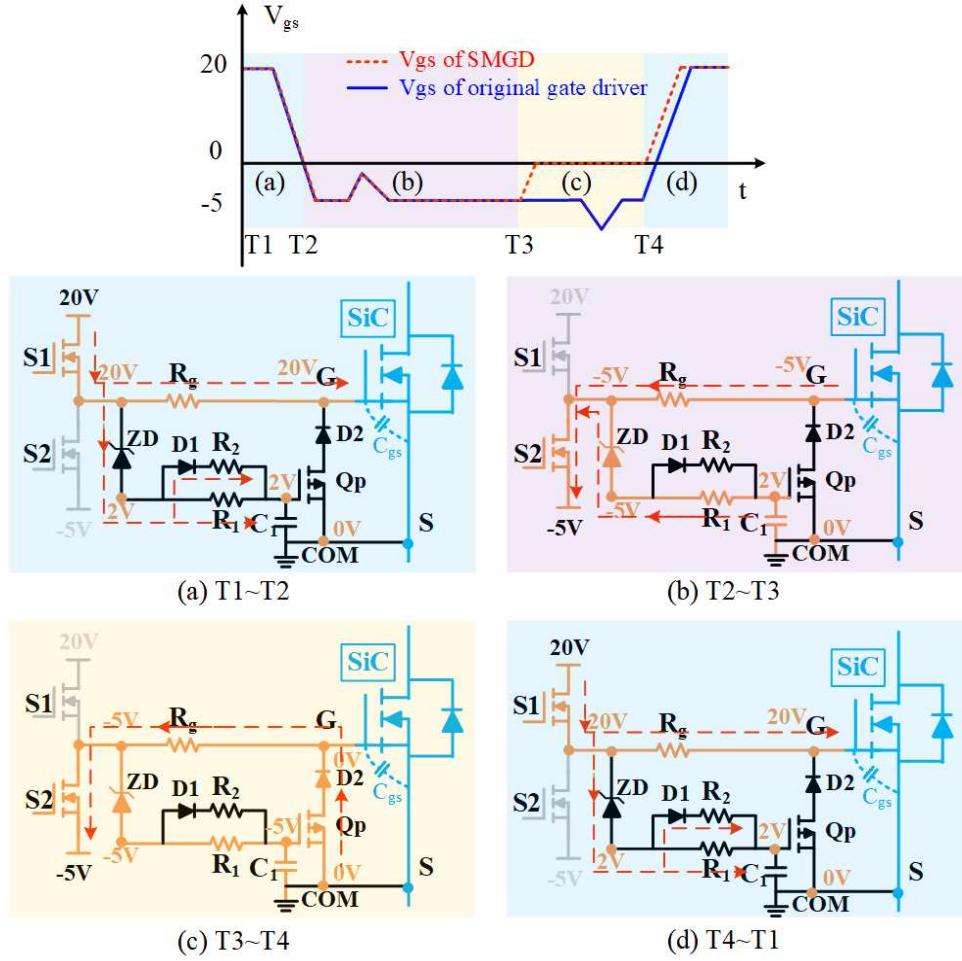
**Table 2.1:** Components List for SMGD.

Label	Components
$ZD$	18 V Zener diode
$D_1, D_2$	Schottky barrier diode
$Q_p$	P-channel MOSFET
$C_1$	Gate-source capacitor of $Q_p$
$R_1, R_2$	Gate on/off resistor of $Q_p$

The gate of the auxiliary switch  $Q_p$  is connected to the output of traditional gate driver IC through RC circuit. When the turn-off signal comes, the gate driver negative output voltage (-5V) will charge the gate of SiC MOSFET through  $R_g$  and meanwhile the IC output voltage will charge the auxiliary RC circuit to make the voltage across  $C_1$  reach the threshold voltage of  $Q_p$  after a designed delay time. This delay makes the  $Q_p$  turn on after the SiC MOSFET gate passes the positive overshooting period (T2-T3 in Fig. 2.2). Once  $Q_p$  turns on, the  $Q_p$  and  $D_2$  provide the short circuit path between the SiC MOSFET gate and source. Therefore, the 0V gate voltage is achieved by  $D_2-Q_p$  clamping.

The operation procedure can be divided into four stages in Fig. 2.5:

- (a) T1-T2: The  $V_{gs}$  is in steady on-state with 20V voltage. The auxiliary circuit is blocked by  $D_2$  and  $Q_p$ , the ZD is working at Zener diode breakdown voltage to limit the voltage across  $C_1$ , protecting the gate of  $Q_p$  from overvoltage.
- (b) T2-T3: When turn-off gate signal comes, the -5V voltage connects through S2, the -5V voltage supply will discharge the SiC MOSFET gate-source capacitor



**Figure 2.5:** Operation Principle for Each Stage.

( $C_{gs}$ ) and the auxiliary  $R_1C_1$  circuit at the same time. Due to the  $R_1C_1$  delay, the SiC MOSFET gate voltage ( $V_{gs}$ ) is already discharged to -5V before the voltage across  $C_1$  reaches  $Q_p$  threshold voltage. This negative  $V_{gs}$  helps SiC MOSFET turn-off faster and moreover, it protects the device from mis-triggering.

(c) T3-T4: After T3 time point, the gate voltage of  $Q_p$  reaches its threshold and  $Q_p$  is turned on, clamping the SiC MOSFET  $V_{gs}$  to 0V by  $D_2-Q_p$  branch. Thus, before the next turn-on, a clamping circuit is connected directly from gate to

source, the gate voltage is already 0V and is harder to exceed gate negative voltage limit. When turn-on gate signal comes, the  $C_{gs}$  voltage will be charged from 0V to 20V, which takes less time to turn-on than traditional gate driver (from -5V to 20V).

- (d) T4-T1: Once the gate voltage becomes positive, the auxiliary  $D_2-Q_p$  branch will be blocked by the Schottky diode  $D_2$  immediately. The 20V power supply, at the same time, will charge the  $R_2C_1$  circuit, the Zener diode ZD is in series with the RC circuit to limit the voltage on  $C_1$  lower than positive driving voltage (20V), protecting the P channel MOSFET from gate overvoltage breakdown. The steady state voltage on  $C_1$  is 2 V. Although  $D_2$  blocks the connection between gate and source, the auxiliary switch  $Q_p$  still needs to be turned off as soon as possible, in order to prepare for the next  $Q_p$  turn-on procedure. The  $Q_p$  has the possibility to not be completely turned off due to the RC delay circuit, especially when the SiC has a short on period. If this happens, when the gate off signal comes, the  $Q_p$  is still at on-state instead of being turned on after an expected RC time delay, which brings the gate voltage to zero level before the  $V_{gs}$  positive overshooting happens. The bad impact of this is that the positive spike will ride on a 0V  $V_{gs}$  rather an adequate negative level, which exposes the device in a much higher risk of mis-triggering. Therefore, a small RC time constant is still necessary for the  $Q_p$  turn-off even though the  $D_2$  can block the positive voltage immediately. That is why a parallel gate path with  $R_2$  and  $D_1$  are used here. It will not affect the  $Q_p$  turn-on time constant and turn-on/off time constants can be designed separately.

## 2.4 Design Guideline of Proposed Smart Self-driving Voltage Source Gate Driver

### 2.4.1 RC Circuit Design

There are two different RC circuits in the auxiliary gate circuit: ON time RC circuit  $R_1C_1$  and OFF time RC circuit  $(R_1//R_2)C_1$ . These two time constants should be considered separately.

#### 1) The ON time $R_1C_1$ time constant

The rise time of  $R_1C_1$  circuit  $T_r$  is set to be 3 times of the time constant  $T_{c1}$  for 95% voltage rise:

$$T_r = 3T_{c1} = 3R_1 \cdot C_1 \quad (2.1)$$

The  $V_{gs}$  of  $Q_p$  relationship with RC time constant is shown in 2.2.

$$V_{gs,Qp} = V_i - (V_i - V_\infty)e^{-t/R_1C_1} \quad (2.2)$$

where  $V_{gs}, Q_p$  is the  $V_{gs}$  of  $Q_p$ ,  $V_i$  is the initial voltage which is 2V in this case, and  $V_\infty$  is the final state voltage which is -5V in this case. This 95% voltage rise is mainly based on the  $T_r$  upper limit design consideration. Because 95% voltage rise makes -4.65 V  $V_{gs}$  of  $Q_p$  per 2.2. This  $V_{gs}$  voltage level can guarantee  $Q_p$  will safely turn on considering the temperature influenced gate threshold voltage shifting (from -1V to -3V) [136]. Besides, the on-state resistance ( $R_{ds(on)}$ ) is smaller when gate voltage of  $Q_p$  is higher than 4 V. This low  $R_{ds(on)}$  guarantees good voltage clamping performance of SiC gate voltage. Additionally, after the  $V_{gs}$  reaches threshold voltage, it takes around tens of nano-second to make  $Q_p$ 's  $V_{ds}$  rise from -5 V to nearly 0 V. A certain time margin should be considered. Thus, 95% voltage rise is determined to guarantee

that  $Q_p$  is safely on with low on-state resistance ( $0.15 \Omega$  [136]) and that  $V_{ds}$  of  $Q_p$  has already changed from -5 V to 0 V to clamp the gate of SiC MOSFET. Therefore,  $T_r$  should fulfill the first constraint 2.3

$$T_r < T_{uplim} \quad (2.3)$$

Where  $T_{uplim}$  represents the upper limit of the rise time  $T_r$ .  $T_{uplim}$  is designed to guarantee that before the negative overvoltage happens,  $Q_p$  is already at on-state to clamp the  $V_{gs}$  at zero voltage. The crosstalk, which is  $V_{gs}$  negative overvoltage in this situation, takes place at the complimentary switch turn-off transition. In this chapter's analysis, as shown in Fig. 2.1(a)(b), S2's  $T_{uplim}$  should start from the time point of active switch S2's  $V_{gs}$  turn-off signal and should end at the time point of complementary switch S1's  $V_{gs}$  turn-off signal. Thus,  $T_{uplim}$ , the upper limit of rising time  $T_r$ , can be calculated by 2.4:

$$T_{uplim} = T_{offmin} - DT \quad (2.4)$$

Where  $T_{offmin}$  is the SiC MOSFET minimum off-state time, which usually depends on the modulation index or maximum duty cycle of the converter, and  $DT$  is deadtime. For the lower limit of  $T_r$ , once the  $V_{gs}$  of  $Q_p$  reaches threshold voltage (-1 V–3 V), the  $Q_p$  starts to turn on, which means  $Q_p$  may turn on prior to  $T_r$  time. Based on this consideration, in order to make sure that  $V_{gs}$  of SiC MOSFET stays -5 V for the turn-off  $V_{ds} dv/dt$  transient. The lower limit should cover the gate threshold voltage shifting range (-1 V–3 V) which means the time of  $Q_p$   $V_{gs}$  from steady off-state (2 V) to minimum threshold voltage (-1 V), named  $T_{Qp,on,min}$ , should be larger than the SiC MOSFET turn-off transient time. According to 2.2,  $T_{Qp,on,min}$  can be calculated when  $V_{gs,Qp}$  is -1 V. Equation 2.5 shows the relationship between  $T_{Qp,on,min}$ ,  $T_r$ , and  $T_{c1}$ .

$$T_{Q_p,\text{on,min}} = 0.85 \times T_{C1} = 0.28 \times T_r \quad (2.5)$$

Equation 6 shows  $T_{Q_p,\text{on,min}}$  design constraint:

$$T_{Q_p,\text{on,min}} > T_{\text{set}} \quad (2.6)$$

where  $T_{\text{set}}$ , is time period from the gate off signal falling under threshold to the end of the  $V_{ds} dv/dt$  in the hard-switching case (Fig. 2.1(c)(d)), and the time period of the deadtime in the soft-switching case (Fig. 2.1 (a)(b)).

Combined 2.5 and 2.6, the criterion for the  $T_r$  lower limit  $T_{\text{lowlim}}$  is as 2.7:

$$T_r > 3.57 \times T_{\text{set}} = T_{\text{lowlim}} \quad (2.7)$$

Thus, the rise time  $T_r$  range is determined by

$$3.57 \times T_{\text{set}} = T_{\text{lowlim}} < T_r < T_{\text{uplim}} = T_{\text{offmin}} - DT \quad (2.8)$$

For example, in the SPWM application, there is minimum pulse and maximum pulse limitation. If the switching frequency is 1 MHz, and the real duty cycle is limited in 0.1-0.9. Per 2.1 and 2.8, the  $T_r$  and  $R_1C_1$  time constant  $T_{c1}$  can be determined:  $71.4ns < T_r < 80ns$ ;  $23.8ns < T_{C1} < 26.7ns$ . Thus, the  $(R_1, C_1)$  can be selected as  $(25 \Omega, 1 nF)$ .

Besides, the gate circuit time constant  $T_{c1}$  affects the switching speed of the  $Q_p$ , which is also the transition speed of the SiC MOSFET  $V_{gs}$  rising from -5 V to 0 V. The switching speed of the  $Q_p$  heavily depends on its  $V_{gs}$  slew rate around the threshold point. A smaller time constant  $R_1C_1$  leads to a higher  $V_{gs}$  slew rate thus creates a higher  $V_{ds} dv/dt$  for the  $Q_p$ . The total time cost for the gate of SiC MOSFET

changing from -5 V to 0 V is composed of the  $R_1C_1$  time delay ( $T_r$ ) and the transition time of  $Q_p$ . As discussed, the transition time of  $Q_p$  is positively related to the  $T_r$ . Therefore, if the application needs an ultra-high switching frequency, the  $T_r$  should be designed as small as possible, for example, reaching the lower limit  $T_{\text{lowlim}}$ .

## 2) The OFF time $(R_1//R_2)C_1$ time constant

The off time constant should fulfill the constraint 2.9:

$$3T_{c2} < T_{\text{onmin}} \quad (2.9)$$

where  $T_{c2}$  is  $(R_1//R_2)C_1$  time constant and  $T_{\text{onmin}}$  is SiC MOSFET minimum on-state time. Choosing three times of RC time constant is for the same reason as the  $T_r$  design).

When the turn-on transient comes, it is not necessary to turn off the auxiliary PMOS  $Q_p$  immediately since the Schottky diode  $D_2$  will block the SiC gate on state voltage (20V) even though the  $Q_p$  is still on. The  $(R_1//R_2)C_1$  time constant should guarantee that during the minimum SiC MOSFET  $V_{gs}$  on-state time (determined by the application minimum duty cycle), the  $Q_p$  can be completely turned off before the next SiC turn-off transient, which means  $C_1$  finishes charging process to positive steady state voltage before the next turn-off transient. Moreover,  $C_1$  value should be the sum of the  $Q_p$  gate-source capacitor  $C_{gs}$  and the external capacitor.

## 3) $R_1, R_2$ design

After the ON/OFF time constant are determined, the resistor  $R_1$  and  $R_2$  values are mainly limited by the gate driver IC pulse current limit. Different from conventional gate driver, the output current of the gate driver IC in the proposed circuit flows into two parallel paths one is the gate of the main SiC MOSFET, and another is

the gate of the auxiliary switch  $Q_p$ . The commercial gate driver current limit should be bigger than the sum of the SiC gate pulse current and auxiliary switching pulse current. The equations are:

$$\begin{cases} \frac{V_{cc}(20V) - V_{ZD} - V_{ss}(-5V)}{R_1//R_2} + \frac{V_{cc}(20V)}{R_g} \leq I_{GD,SOURCELimit} \\ \frac{V_{cc}(20V) - V_{ZD} - V_{ss}(-5V)}{R_1} + \frac{V_{cc}(20V) - V_{ss}(-5V)}{R_g} \leq I_{GD,SINKLimit} \end{cases} \quad (2.10)$$

where the  $V_{cc}(20V)$  and  $V_{ss}(-5V)$  are 20 V/-5 V gate driving voltage;  $V_{ZD}$  is Zener diode ZD breakdown voltage;  $I_{GD,SOURCELimit}$  is the gate driver IC output positive current pulse limit;  $I_{GD,SINKLimit}$  is the gate driver IC output negative current pulse limit. If the gate resistor of the main SiC MOSFET  $R_g$  is determined per application desired  $dv/dt$ ,  $R_1$  and  $R_2$  lower limit can be calculated by 2.10. Once  $R_1$  and  $R_2$  are calculated, the capacitor  $C_1$  is determined per time constant  $T_{c1}$  and  $T_{c2}$  limitation.

#### 2.4.2 Diode $D_2$ and ZD Selection

$D_2$  is to block the SiC positive gate voltage, so  $D_2$  voltage rating should be larger than the gate absolute voltage ( $V_{g+} + |V_{g-}|$ ). And the Schottky diode is preferred since the reverse recovery loss is neglectable. When selecting the Schottky diode, the reverse static loss [137] is an important parameter since it is directly related to the auxiliary circuit additional power loss. ZD is to protect  $Q_p$  gate from overvoltage breakdown. So, the Zener diode breakdown voltage  $V_{ZD}$  should fulfill the equation:

$$V_{cc} > V_{ZD} > V_{cc} - V_{Qp,gsmax} \quad (2.11)$$

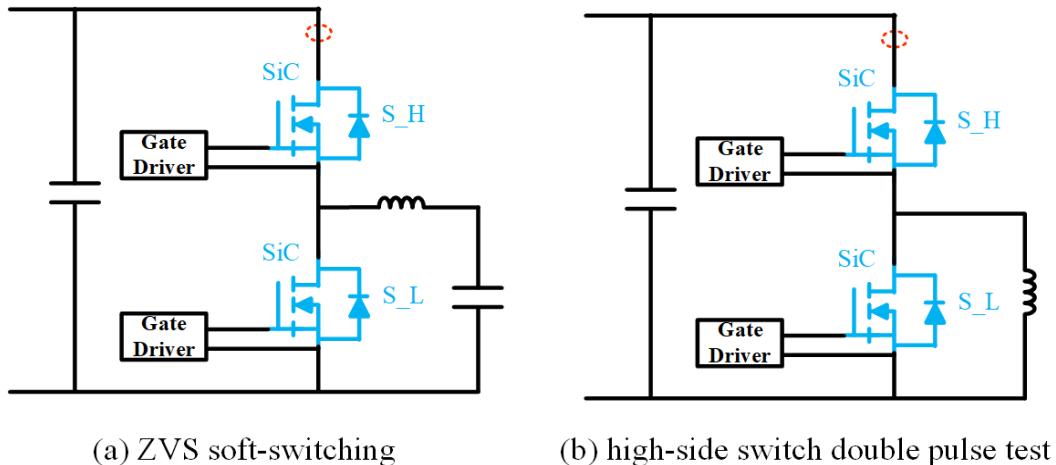
where  $V_{Qp,gsmax}$  is  $Q_p$  maximum gate voltage;  $V_{cc}$  is gate absolute voltage difference ( $V_{g+} + |V_{g-}|$ ). By this constraint 2.11, the  $Q_p$  gate voltage is guaranteed to be smaller than maximum gate voltage.

### 2.4.3 Gate Resistor $R_g$ Selection

During the clamping time of  $V_{gs} = 0V$  (T3-T4 in Fig. 2.5(c)), the  $R_g$  will conduct continuous current. Thus, the power consumed on  $R_g$  becomes higher. A high-power rating thin film resistor with small package can be chosen. First, this kind of resistor is available, like the high-power film resistor PHP series from VISHAY [138]. Second, the 2512 package resistor will not introduce large parasitic inductance because the parasitic inductance of the thin film resistor is smaller than 2nH [139, 140]. Therefore, the chosen resistor induced gate loop parasitic inductance and footprint change are negligible. The detailed  $R_g$  loss calculation will be illustrated in the experimental section.

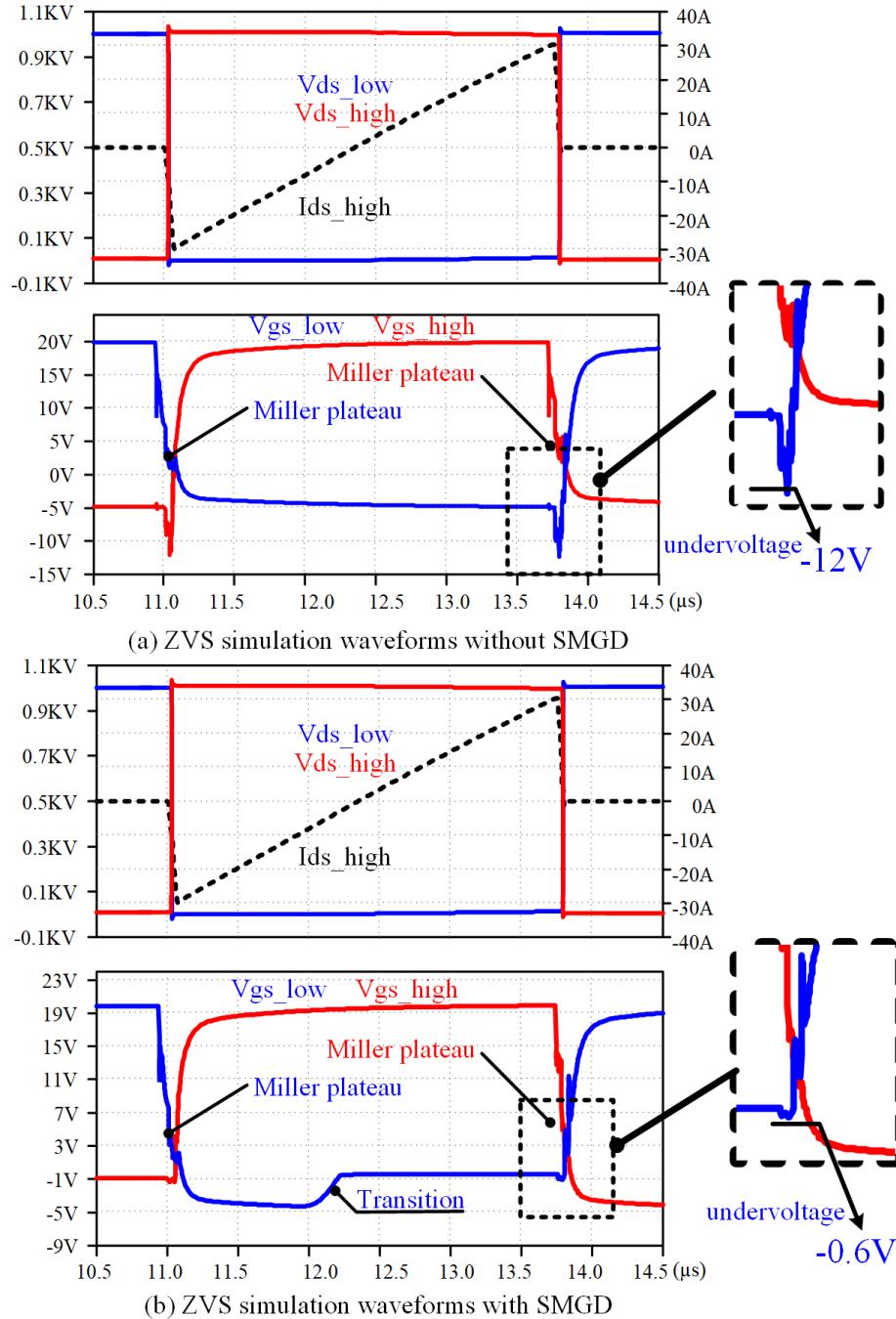
## 2.5 SPICE Simulation Results

In this section, two representative cases simulations for phase-leg configuration, ZVS soft-switching and double pulse test, are conducted. The schematics are shown in Fig. 2.6.



**Figure 2.6:** Schematics of SPICE Simulations: (a) ZVS Soft-switching; (b) High-side Switch Double Pulse Test.

### 2.5.1 Simulation Results of ZVS



**Figure 2.7:** ZVS Simulation Results: (a) Without Proposed Auxiliary Circuit, the High-side and Low-side MOSFET  $V_{gs}$  Waveforms; (b) With Proposed Auxiliary Circuit, the High-side and Low-side MOSFETs  $V_{gs}$  Waveforms.

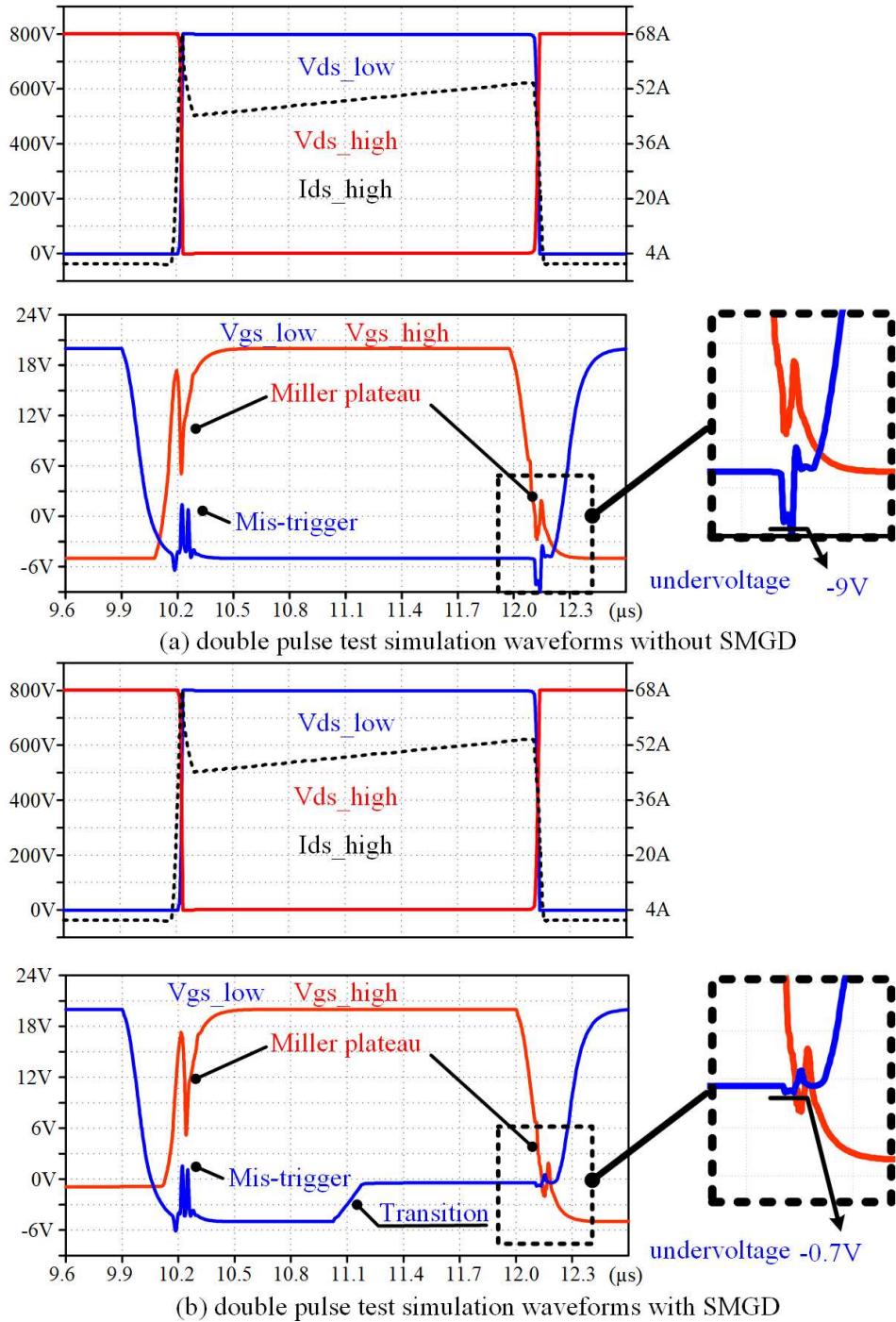
The SPICE simulation using half bridge ZVS soft-switching is developed, corresponding to the case of Fig. 2.1 (a)(b). Fig. 2.7 shows the  $V_{gs}$  waveforms with and without the proposed auxiliary circuit. Without auxiliary circuit, the  $V_{gs}$  waveforms of both high-side and low-side devices in the phase-leg have negative overshooting voltage before  $V_{gs}$  rise-up. There is a large negative overshooting during phase-leg deadtime period which could result in gate overvoltage breakdown. While using the auxiliary circuit, the negative overshooting voltage is almost clamped to 0 V.

### 2.5.2 Simulation Results of Double Pulse Test

Fig. 2.8 shows the double pulse test simulation results, corresponding to the case of Fig. 2.1 (a)(d) or (b)(c). The  $V_{gs}$  of device under test (red) has the miller plateau for both  $V_{gs}$  rising and falling edge because it is hard-switching, and the change of  $V_{ds}$  depends on this device  $V_{gs}$  signal. And the complementary switch  $V_{gs}$  (blue) has possible mis-trigger and negative overvoltage issues. Without auxiliary circuit, as shown in Fig. 2.8(a), the  $V_{gs}$  negative overshooting reaches -9 V. With auxiliary circuit, as shown in Fig. 2.8(b), the negative overshooting nearly disappears. From the simulation, the transition time from -5 V to 0 V is around 100 ns. The crosstalk suppression capability of this auxiliary circuit is verified for both ZVS soft-switching and double pulse test. The simulation and hardware components part number are listed in Table 2.2.

## 2.6 Experimental Verification and Performance Evaluation

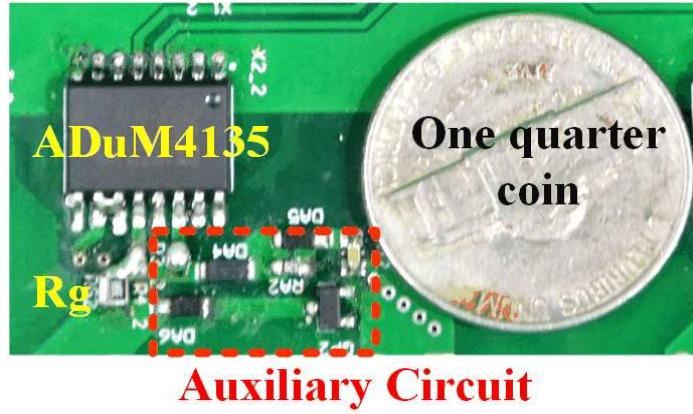
A gate driver board with proposed auxiliary circuit is developed, and the picture of gate driver auxiliary circuit is shown in Fig. 2.9. The gate signal of SiC MOSFET and  $V_{gs}$  waveforms of the auxiliary P-MOS before the main power is on are shown in Fig. 2.10. A zero level gate voltage is created for the SiC MOSFET in the middle of



**Figure 2.8:** Double Pulse Test Simulation Results: (a) Without Proposed Auxiliary Circuit, High-side and Low-side MOSFET  $V_{gs}$  Waveforms; (b) With Proposed Auxiliary Circuit, the High-side and Low-side MOSFETs  $V_{gs}$  Waveforms.

**Table 2.2:** Components List for Auxiliary Circuit.

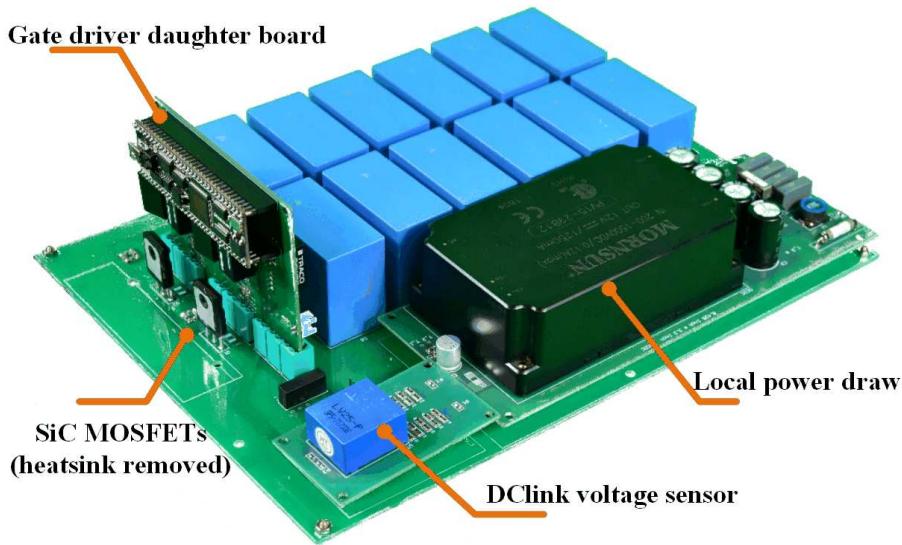
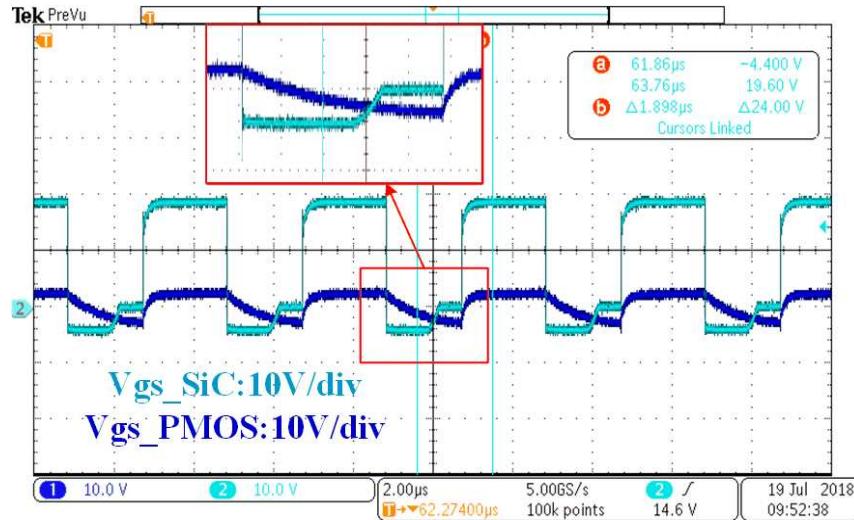
Label	Description	Components
$ZD$	18 V Zener diode	TDZV18B
$D_1, D_2$	Schottky barrier diode	RB550VYM-30FHTR
$Q_p$	P-channel MOSFET	FDN358P
$C_1$	Gate-source capacitor of $Q_p$	4.7 nF
$R_1, R_2$	Gate on/off resistor of $Q_p$	20 $\Omega$
$R_g$	Gate resistor	10 $\Omega$



**Figure 2.9:** Gate Driver Hardware Picture.

the off period, right after the gate voltage of the auxiliary PMOS  $Q_p$  (negative gate voltage driving) reaches its threshold. The RC time constant controls the start time of the zero gate voltage. The rise time from -5 V to 0 V for SiC gate voltage is around 100 ns.

Rather than focusing on the assessment of the SiC MOSFET switching characteristics as traditional double pulse test [20–22, 32, 141–146], this chapter focuses on the crosstalk suppression performance of proposed SMGD in the phase-leg configuration. A double pulse test is conducted using half bridge circuit, as shown in Fig.



2.6(b). The test setup is shown in Fig. 2.11. The DLink voltage sensor is not used in this study and the local power draw module is to convert dlink voltage to gate driver signal power supply voltage. In this double pulse test, the commercial gate driver is ADuM4135 from Analog Device, and the power device is C2M0040120D

from Wolfspeed. The  $V_{gs}$  measurement accuracy is most critical to show the crosstalk suppression, so the most accurate probe TPP1000 with 1 GHz bandwidth is used to measure the  $V_{gs}$  of the low side device. The high-side device is served as DUT to reveal the crosstalk issue of the low-side  $V_{gs}$ , since the passive probe can only measure grounded signals. Several papers have discussed about the measurement accuracy issue [20, 32, 145]. Table 2.3 shows the rise/fall minimum time of the measured signals and corresponding oscilloscope probes, the bandwidth or estimated minimum rise/fall time measurement capability of the probes is sufficient [20, 32]. Although 120MHz bandwidth current probe, compared with coaxial shunt, may not be precise for the switching energy calculation due to the time delay or switching V-I timing alignment [32, 146–148], this probe can reveal the details of the current waveforms [20, 32].

**Table 2.3:** Probes Used in the DPT Experiment.

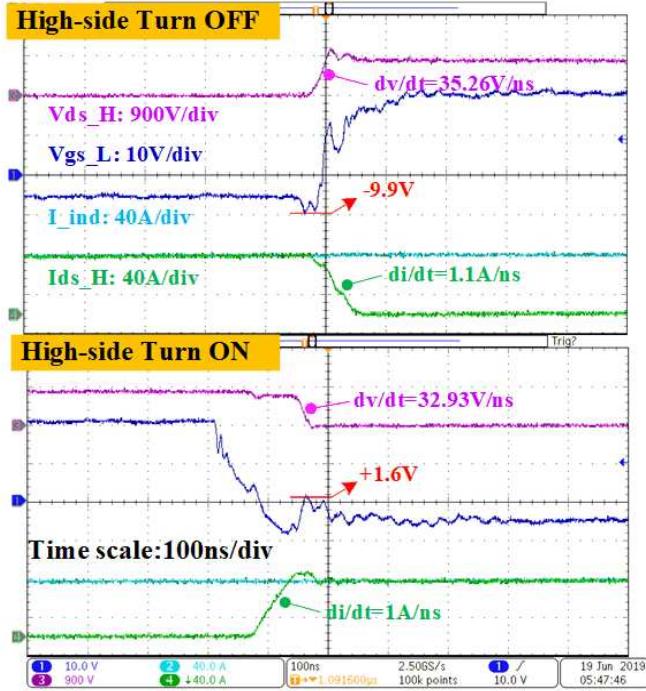
Measured signals	Low side $V_{gs}$	High side $V_{ds}$	High side $I_{ds}$	Inductor current
Probe model	TPP1000	P5205A	P6022	P6022
Probe bandwidth	1 GHz	100 MHz	120 MHz	120 MHz
Probe minimum rise/fall time capability*	1.75 ns	1.75 ns	14.58 ns	14.58 ns
Estimated experiment signal minimum rise/fall time**	15 ns	21 ns	30 ns	-
Measured signal minimum rise/fall time	20 ns	25 ns	60 ns	-

\*Rise time is calculated based on [25] with 5 times margin.

\*\*Suppose  $I_{ds} \frac{di}{dt}$  slope 2 A/ns and  $V_{ds} \frac{dv}{dt}$  slope 40 V/ns based on the SiC MOSFET double pulse test waveform [146] with 1.3 times margin.

Three gate driver configurations - traditional gate driver without Schottky diode

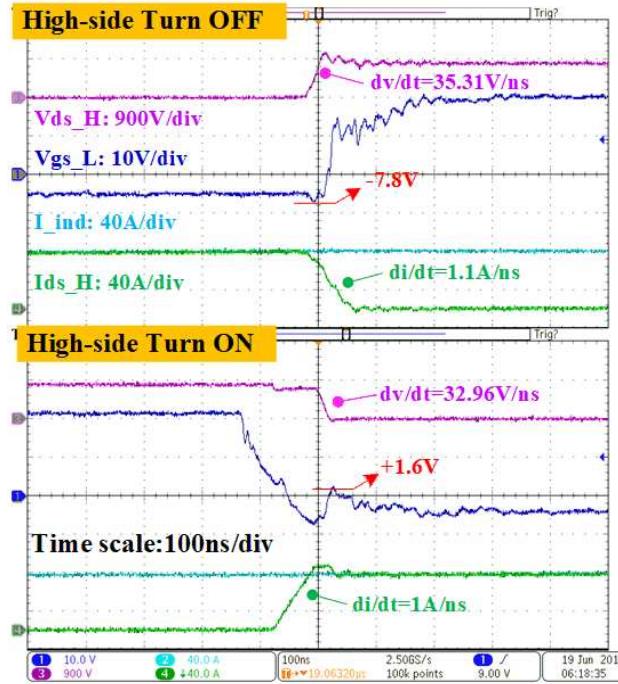
clamping, gate driver with Schottky diode clamping and SMGD, are implemented to verify the effectiveness of the proposed SMGD.



**Figure 2.12:** 850V/60A Double Pulse Test Waveforms: Original Gate Driver Configuration Without Diode Clamping. The  $V_{ds\_H}$  Represents High Side Device Drain-source Voltage; the  $V_{gs\_L}$  Is the Low Side Device Gate-source Voltage; the  $I_{ind}$  Is the Inductor Current; the  $I_{ds\_H}$  Is the High Side Drain-source Current.

In the double pulse test, the gate resistor value and the other power loop parameters are the same for three configurations. The test condition is 850V dclink voltage and 60A device current for 1200V/60A device. Under this full rating (or even excessive rating) voltage and current, the device will exhibit the maximum  $dv/dt$  which will expose the gate to the highest risk of mis-triggering or negative over-voltage breakdown. If under this extreme case, the proposed strategy can help mitigate the risk significantly, it is persuasive to claim the proposed method is effective under the full operation region. Fig. 2.12 shows the double pulse test results of the original gate driver configuration. For the high-side device turn-off transient, the  $V_{ds}$   $dv/dt$

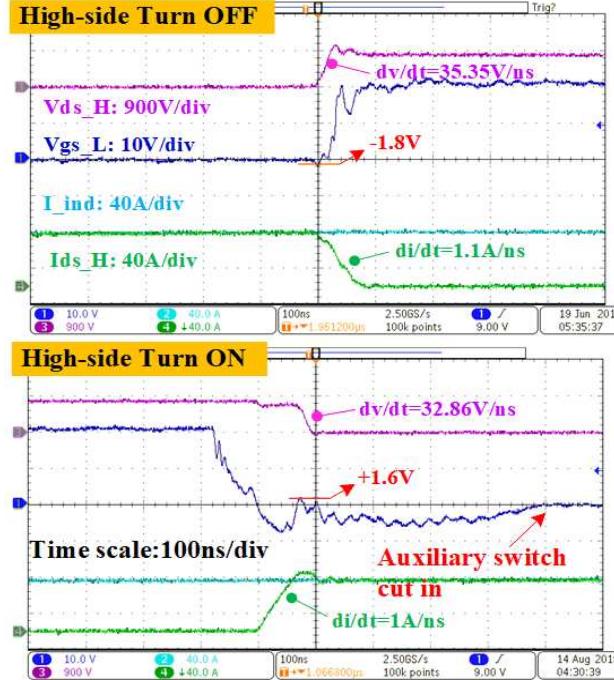
is 35.26V/ns and the  $I_{ds}di/dt$  is 1.1 A/ns. The high  $dv/dt$  results in huge crosstalk effect, which makes the low-side  $V_{gs}$  negative overshooting reach -9.9 V, close to the datasheet stated minimum allowable gate voltage “-10 V”. This negative overshooting voltage makes the device vulnerable to the gate breakdown.



**Figure 2.13:** 850V/60A Double Pulse Test Waveforms: Original Gate Driver Configuration With Diode Clamping.

When the Schottky diode clamping technique is used, as shown in Fig. 2.13, the negative overshooting voltage is reduced to -7.8V. The amplitude of the negative overvoltage is reduced but to limited extent, so the risk of gate breakdown still exists, especially under long time operation.

Fig. 2.14 shows the results of the proposed SMGD. The  $V_{gs}$  negative overshooting is significantly alleviated, with only -1.8 V at  $V_{ds} dv/dt$  35.57 V/ns. The transition time of the gate voltage from -5 V to 0 V is around 100 ns. Table 2.4 summarizes the experiment data of these three gate driver configurations. Different from the afore-



**Figure 2.14:** 850V/60A Double Pulse Test Waveforms: Proposed Smart Self-driving Gate Driver Configuration.

mentioned two methods, the proposed SMGD completely saves the device from gate negative overvoltage breakdown, showing a transformative solution rather than an additive improvement. With this solution, the device  $dv/dt$  can be raised significantly since the risk of gate mis-triggering or negative breakdown is significantly mitigated. In other words, an important obstacle limiting the SiC MOSFET actual switching speed has been removed by the proposed method. With improved switching speed, the device switching loss can be reduced.

By utilizing the auxiliary circuit, the driving loss will increase. The major driving loss of the auxiliary circuit is due to the loss of  $R_g$  during the 0V  $V_{gs}$  period, since the  $R_g$  is connected to the gate IC output directly through  $Q_p$ . During the time of  $V_{gs}$  clamping to 0V, the continuous current will incur around 2W power loss in the worst case. However, the impact of this additional loss on the converter is negligible.

**Table 2.4:** 850 V/60 A Double Pulse Test Results of Three Gate Driver Configurations.

GD configurations	Original GD w/ Zener diode clamping	Original GD w/ Schottky diode clamping	Proposed SMGD
<b>Turn on</b> $dv/dt$ (V/ns)	32.93	32.96	32.86
<b>Turn off</b> $dv/dt$ (V/ns)	35.26	35.31	35.57
<b>Mis-trigger</b> $V_{gs}$ (V)	+1.6	+1.6	+1.6
<b>Undervoltage</b> $V_{gs}$ (V)	-9.9	-7.8	-1.8
<b>Turn on</b> $di/dt$ (A/ns)	1.1	1.1	1.1
<b>Turn off</b> $di/dt$ (A/ns)	1	1	1

Through calculation, it can be seen that at worst case, this additional power loss takes up around 0.1% of total device power loss at 1MHz switching frequency, and around 0.7% of total power loss at 50kHz switching frequency (Since SiC is usually adopted for operation at frequency; 65kHz, only the frequency above 50 kHz is considered). The percentage of this additional loss in the total power loss is small, so it won't affect the efficiency that significantly. The details of the gate driving loss calculations are shown in the following paragraphs. The traditional voltage source gate driver loss is calculated by 2.12 [149]

$$P = Q_g \times (V_{g+} - V_{g-}) \times f_{sw} \quad (2.12)$$

where  $Q_g$  is gate total charge,  $V_{g+}$ ,  $V_{g-}$  are on/off state gate voltage, and  $f_{sw}$  is switching frequency.

For the 1.2kV/60A SiC MOSFET C2M0040120D [150] from Wolfspeed switching at 1MHz frequency, the driver loss is 2.875W per 2.12. If higher current rating MOSFET is used, the gate total charge  $Q_g$  will be bigger and the driver loss will be

bigger (e.g. 4.025W driver loss for 1.2kV/90A MOSFET C2M0025120D [151]).

The additional loss induced by the auxiliary circuit is composed of three parts:

1. P-MOS  $Q_p$  gate driving loss; 2.  $D_2$  reverse static power loss; 3.  $Q_p$ ,  $D_2$ ,  $R_g$  conduction loss during clamping period.

1 For ZD,  $D_1$ ,  $R_1$ ,  $R_2$  driving circuit, if  $Q_p$  is FDN358P [136] from ON Semiconductor, the loss per 2.12 is  $P1 = 0.028W$ .

2 If  $D_2$  is Schottky barrier diode RB550VYM-30FHTR [137] from ROHM semiconductor, the  $D_2$  reverse recovery loss can be neglected, and the static reverse power loss  $P2$  is 0.04 W [137].

3 The conduction loss during clamping is big, because the negative voltage is largely applied to gate resistor  $R_g$ . In the proposed SMGD,  $R_g$  is  $10 \Omega$  and the negative voltage is -5V; the forward voltage-drop of  $Q_p$  and  $D_2$  are 0.1 V and 0.4 V, respectively. So, the current  $I_{g,clp}$  can be calculated.

The power loss during clamping time can be calculated by 2.13.

$$P_3 = k \times I_{g,clp} \times V_{g-} \quad (2.13)$$

where  $k$  is the portion of clamping time on the total switching period. For different cases,  $k$  is different. Three cases are considered: 1. worst case, permanently off state, where  $k$  equals to 1; 2. 50% duty cycle PWM case, where  $k$  equals to 0.25 supposing the clamping happens in the middle of the off state; 3. SPWM case, where  $k$  equals to 0.5 supposing the average duty cycle of SPWM is 0.5; So, the additional power loss induced by auxiliary circuit is

$$P_{\text{add,loss}} = P_1 + P_2 + P_3 \quad (2.14)$$

**Table 2.5:** Components List for Auxiliary Circuit.

Item	Loss (W)	Percent of total loss
Traditional gate driving loss	2.875	83.81%
Additional gate resistor loss	0.631	14.20%
Auxiliary driving circuit loss	0.028	0.82%
Diode $D_2$ static loss	0.04	1.17%
<b>Total</b>	<b>3.506</b>	<b>100%</b>

Table 2.5 shows the gate driving loss breakdown for the case of 50% duty cycle PWM at 1 MHz frequency. The additional loss takes up only 16% of total gate driving loss. This extra power loss induced influences on the gate driver can be classified into three points:

- 1 No change on the Gate driver IC selection. This clamping circuit won't increase the gate peak current, and the power dissipation inside the gate driver IC will not exceed its limit since the internal gate resistor is small.
- 2 A DC/DC isolated power supply with a higher power rating is needed. Higher power rating DC/DC converter (2W higher) with the same package is available in the market, such as products from RECOM, MURATA, CUI, etc.
- 3 A higher power rating gate resistor  $R_g$  should be selected as discussed in Section IV. C.

Table 2.6 shows the power loss evaluation with and without SMGD at most common operation conditions for phase-leg configuration. The driving loss percentage of total SiC device loss is around 0.1% at 1MHz high switching frequency and is only around 0.7% at 50 kHz low switching frequency.

**Table 2.6:** Power Loss Evaluation With and Without SMGD at Different Operation Conditions.

Switching frequency	Cases	Traditional driving loss	Additio-nal dri-v ing loss	Total driving loss	SiC switch-ing loss	SiC conduc-tion loss	Driving loss per-cent-age of total SiC loss
1MHz	Permen-ently off	2.875W	2.318W	5.193W	3836W	144W	0.13%
	SPWM	2.875W	1.193W	4.068W	3836W	144W	0.10%
	50% duty cycle PWM	2.875W	0.631W	3.506W	3836W	144W	0.08%
50kHz	Permen-ently off	0.145W	2.291W	2.436W	191.8W	144W	0.72%
	SPWM	0.145W	1.165W	1.310W	191.8W	144W	0.39%
	50% duty cycle PWM	0.145W	0.603W	0.748W	191.8W	144W	0.22%

\*The calculation is based on the parameters of 1.2 kV/60 A SiC MOSFET C2M0040120D.

## 2.7 Conclusions

Wide band gap devices can switch at much higher speed ( $dv/dt$  and  $di/dt$ ) than Si devices. This brings many benefits at system level in terms of efficiency and power density. But high switching speed can cause problems such as EMI,  $V_{ds}$  overvoltage, gate overvoltage breakdown or mis-triggering, and so on. A smart self-driving multi-level gate driver is proposed to solve the issues of high  $dv/dt$  caused gate mis-triggering and gate negative overvoltage breakdown. By inserting a zero level in  $V_{gs}$  during the off period, the first portion of  $V_{gs}$  can be designed more negative to avoid the mis-triggering, and more importantly, the negative overshooting in the second portion of

the off period can occur based on the zero voltage level instead of a negative voltage level to avoid the negative over-voltage breakdown. When designing the circuit, the circuit complexity is significantly reduced by utilizing the original gate voltage as the trigger of the auxiliary circuit, instead of utilizing independent gate driving circuits and isolation stages. The proposed circuit is easy to be integrated with the commercial gate driver ICs to form the complete three-level gate driver. The proposed gate driver is highly efficient and highly compact, as well as cost-effective.

## Chapter 3

### INTEGRATION OF MONOLITHIC GAN HALF-BRIDGE USING MULTI-LEVEL GATE DRIVER

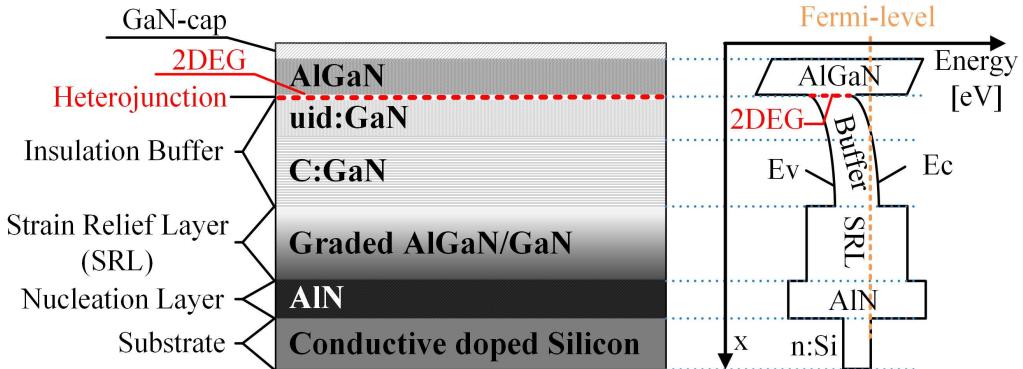
For single GaN device, holes injection through p-GaN from drain region has been proved to effectively release the trapped electrons, so that the  $R_{dson}$  degradation is fully eliminated [56]. For the monolithic integrated half-bridge, the trapped electrons are located mainly in source region of the high side device. The work in this chapter addresses the substrate bias effect from the perspective of the gate driver. By injecting additional holes (current) into the device source region through the gate driver, the electrons trapped in the buffer layer can be partially released, and the  $R_{dson}$  degradation is mitigated. Moreover, based on the mechanisms, this work found that there are different  $R_{dson}$  degradation phenomena for hard-switching and soft-switching scenarios. The timing and amount of additional holes (current) injection strategies should be different under hard-switching and soft-switching conditions.

Firstly, this Chapter will elaborate on the two mechanisms of the substrate bias effect. The different mechanisms of high-side and low-side devices at grounded, floating and semi-floating substrate configurations are investigated. Secondly, the  $R_{dson}$  degradation phenomena for hard-switching and soft-switching scenarios will be analyzed in detail. After that, a multi-level gate driver is proposed for the grounded substrate monolithic GaN half-bridge to suppress the substrate bias effect. Then, the experimental results are thoroughly analyzed, and the feasibility of the proposed gate driver are verified at both hard-switching and soft-switching scenarios. Finally, the last part draws the conclusions and future work for the second-level monolithic

integration of GaN HEMTs.

### 3.1 Substrate Bias Effect and its Corresponding $R_{dson}$ Degradation

The epitaxial layer structure, as shown in Fig. 3.1[152, 153], is important for understanding the substrate bias effect [42]. The GaN device uses conductive silicon as the substrate. After the thin AlN-nucleation layer is applied on the substrate, a graded buffer structure is grown on top [154, 155]. This graded buffer structure is composed of a strain relief layer (SRL), a carbon doped GaN layer (C:GaN), and an unintentionally-doped GaN layer (uid:GaN) [156]. The 2DEG is created by means of the hetero-epitaxial growth of a thin AlGaN layer. A high density of conductive electrons channel is formed in this 2DEG layer because of piezoelectric and spontaneous polarization [157].



**Figure 3.1:** The Epitaxial Layer Structure of GaN Transistor and Its Energy Band Diagram at Equilibrium.

#### 3.1.1 Substrate Bias Effect: Root Cause of $R_{dson}$ Degradation

Although substrate bias effects and its experimental validations have been widely investigated in [42, 158], the theory will still be presented because it is fundamental in this investigation. According to the way of applying bias stress, it can be divided

into static substrate bias and dynamic substrate bias. The static substrate bias effect occurs when the substrate bias is applied. While the dynamic bias effect happens after the substrate bias is reset to zero from certain static substrate bias. The measurement routine of these two substrate bias effects are depicted in [42]. Moreover, the polarity of substrate bias can be positive and negative. The  $R_{\text{dson}}$  degradation is caused by the electrons being trapped in the buffer layer. When the external electric field is applied, negative or positive, there will be electrons trapped in the buffer layer. The trapped electrons distort the energy band, leading to temporary 2DEG channel partial depletion.

The energy band diagrams of the GaN transistor at different substrate bias conditions are plotted in Fig. 3.2. The quasi Fermi-level is the average energy level of the electron population probability for the compound material [153]. If the energy band of the material is below Fermi-level, the electrons will have relatively low energy. Therefore, the probability of electrons staying at this energy level is high, and consequently the electrons are stable. If the energy band is above Fermi-level, the energy of electrons will be positive. This will increase the probability of the electrons transitioning energy levels. For GaN device, the electron density of 2DEG is directly related to the conductivity. The 2DEG under Fermi-level means that there are large amount of stable electrons populating in 2DEG. Thus, the conductivity of 2DEG is high. In contrast, if the 2DEG is above Fermi-level, the electrons will have sufficient energy and become unstable. Unstable electrons are easily affected by the stimuli such as temperature and electric field. Therefore, unstable electrons may transit to other places (trapping), leading to a decrease of the electron density in 2DEG. As a result, the conductivity of the channel decreases, and the  $R_{\text{dson}}$  of the device increases.

When the device is at unstressed state, as shown in Fig. 3.2(a), the 2DEG is below Fermi-level. This represents that the electrons in 2DEG are stable, and do not have

enough energy to be trapped into the buffer layer. Therefore, the electron density of 2DEG and channel conductivity are not degraded.

### a. Static Substrate Bias Effect

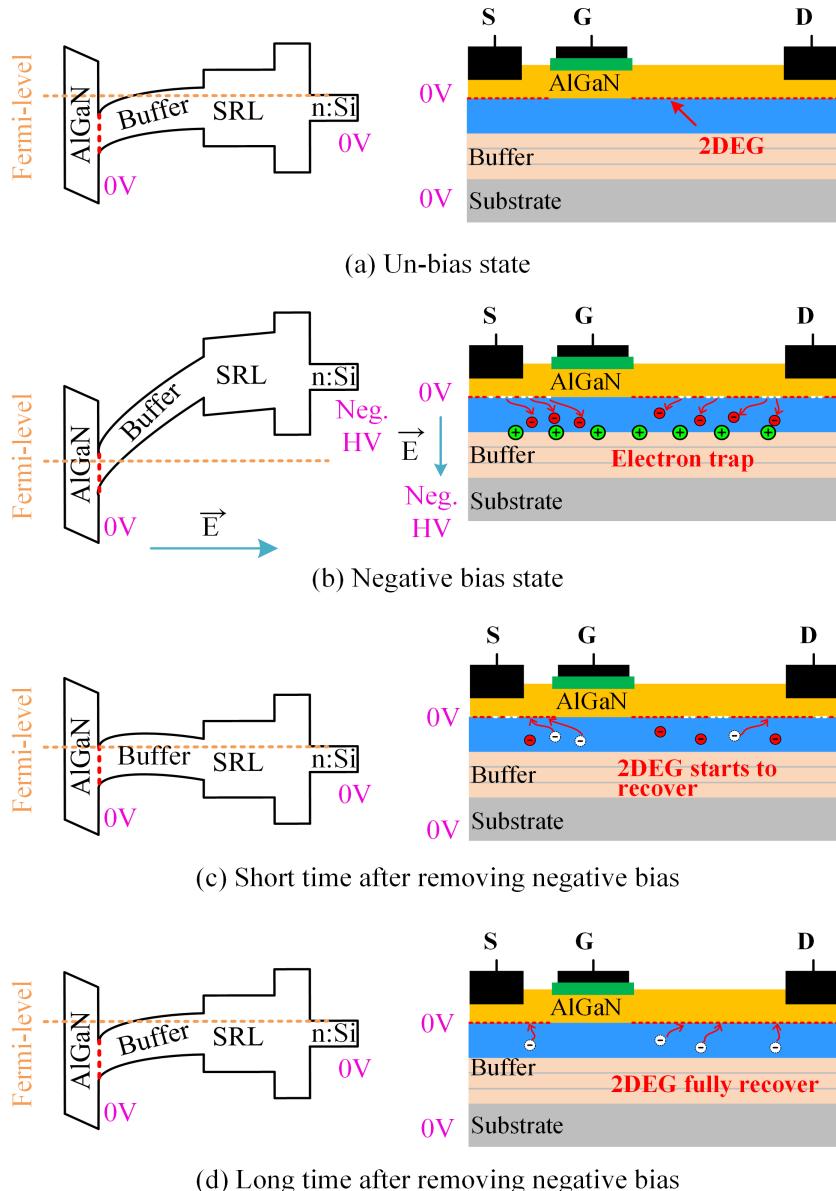
If the static negative substrate bias is applied, as shown in Fig. 3.2(b), the positive charges will accumulate at the top of the buffer layer and stimulate the electrons in 2DEG to occupy the electron orbitals higher than the Fermi-level of the buffer layer materials. It will lift up the energy band, and cause depletion of 2DEG. The depletion level depends on the amplitude of the substrate negative bias.

If the static positive substrate bias is applied, as shown in Fig. 3.2(a), negative charges will accumulate at the top of the buffer layer, pulling down the energy band of the buffer layer. Thus, the electron density in 2DEG will not be influenced because the energy band of 2DEG is still lower than the Fermi-level. Thus, the  $R_{dson}$  of the device will not be degraded under static positive substrate bias condition.

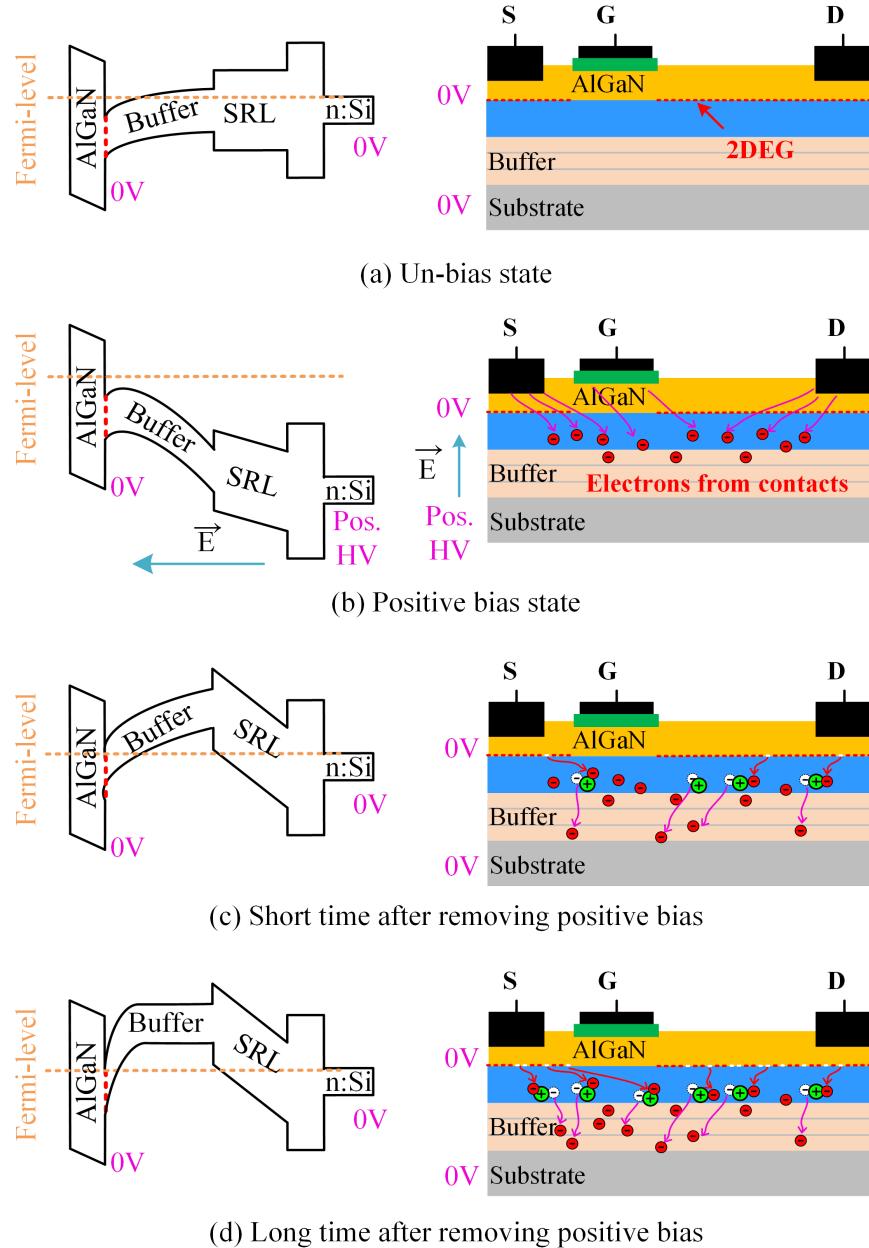
### b. Dynamic Substrate Bias Effect

A short time after resetting the negative or positive substrate bias to zero, the dynamic bias effect can be observed. The electrons in the buffer layer will not release immediately after resetting the biases. Therefore, these trapped electrons distort the energy band and consequently influences the electron density of 2DEG.

For the dynamic negative substrate bias, the resetting substrate pulls down the energy band, as shown in Fig. 3.2(c). Thus, part of the trapped electrons in the buffer will be released to 2DEG. If the time is sufficient, the device will fully recovered to the unstressed state, and the  $R_{dson}$  will become normal, as shown in Fig. 3.2(d). However, the electrons release takes time. A short time after resetting the bias, the electrons cannot be fully recovered immediately, and the  $R_{dson}$  degradation still



**Figure 3.2:** Static and Dynamic Negative Substrate Bias: Band Diagram Distortions and Corresponding Electrons Trapping Process.



**Figure 3.3:** Static and Dynamic Positive Substrate Bias: Band Diagram Distortions and Corresponding Electrons Trapping Process.

exists. According to the experimental results in [42], it takes over 2000 seconds to fully recover after applying 60 seconds substrate bias. Moreover, this recovery time is related to the applied bias amplitude, bias duration and device temperature.

For the dynamic positive substrate bias, the resetting substrate lifts up the energy band, as shown in Fig. 3.3(c). As mentioned previously in this section, there are accumulated electrons in the buffer layer during static positive substrate bias. After removing the applied positive electric field stress, these electrons makes the energy band of the buffer layer higher than that at the unstressed state. Thus, the electrons will have higher energy and become unstable. Without the external electric field stress, the electrons transition will occur. These electrons tend to move from the top of the buffer to the bottom for the relatively even distribution. Correspondingly, the positive charges will appear on the top of the buffer. These positive charges attract the electrons in 2DEG trapped into the buffer layer. Therefore, the 2DEG electron density reduces, and  $R_{\text{dson}}$  degradation happens. The  $R_{\text{dson}}$  degradation will become more severe over time at the beginning. It is because the electrons trapping process takes time. As shown in Fig. 3.3(d), the  $R_{\text{dson}}$  degradation reaches most severe level after a long time. After that, the  $R_{\text{dson}}$  recovery process gradually starts. According to the experimental results in [42], this recovery starts at around 1 to 10 seconds after removing the positive bias.

### 3.1.2 Solutions of $R_{\text{dson}}$ Degradation

As mentioned in Section I, trench technology has been verified by EPC for low voltage monolithic GaN half-bridge ( $\pm 200$  V). For high voltage (600 V) application, the state-of-the-art solution to suppress the substrate bias effect is basically substrate bias voltage manipulation method. In this section, the substrate bias voltage manipulation method will be summarized and its drawbacks will be explained. After that, the

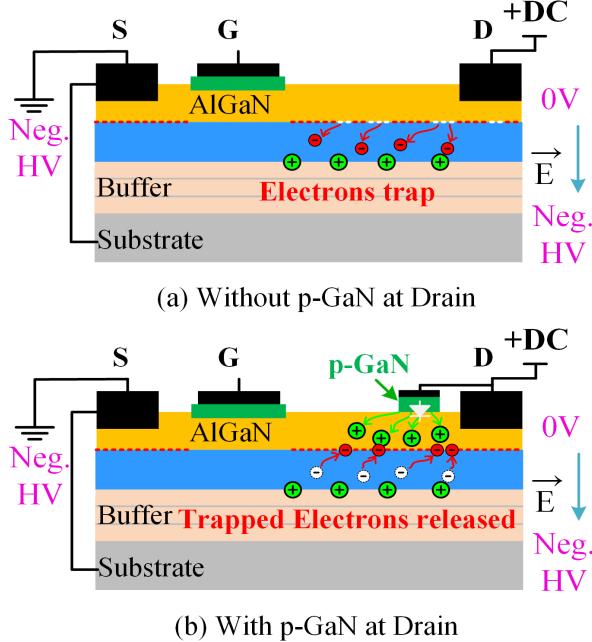
proposed holes injection method will be elaborated in detail.

### a. Substrate Bias Voltage Manipulation

The method of manipulating the substrate bias voltage has been widely investigated by the previous work [42, 58, 59]. The basic idea of this method is to change the substrate voltage potential by changing the substrate resistor-capacitor connection configurations, thereby decreasing the substrate bias amplitude. Although this method improves the device operation voltage, the device voltage rating cannot be fully utilized. It is because for most of the 600 V/20 A GaN power transistors used in previous work, the failure due to severe  $R_{dson}$  degradation occurs at a substrate bias of around 200 V. Thus, even though the substrate voltage is lifting up to half of dc-link voltage, the dc-link voltage can only reach 400 V. Moreover, the non-zero substrate voltage introduces substrate bias effect for the low-side device. It should be noted that this method is not practical, because the dynamic change of the substrate voltage makes it hard to integrate multiple phase-legs in a single substrate.

### b. Hole Injections

The basic idea of holes injection method is to inject positive charges (holes) at the top of 2DEG, thereby, compensating the attraction of electrons by the positive charges in the buffer layer. This idea has been validated in single GaN devices [56]. For the single GaN device, the source is connected to substrate, so no substrate bias issue happens. However, at off state, the drain side is subjected to a negative substrate bias, as shown in Fig. 3.4(a). When the device turns on, the dynamic negative substrate bias effect occurs. By implementing additional p-GaN region at drain side, additional holes are injected, and the trapped electrons in the buffer layer are effectively released. The reason for the effective holes injection through the p-GaN is that the p-GaN is

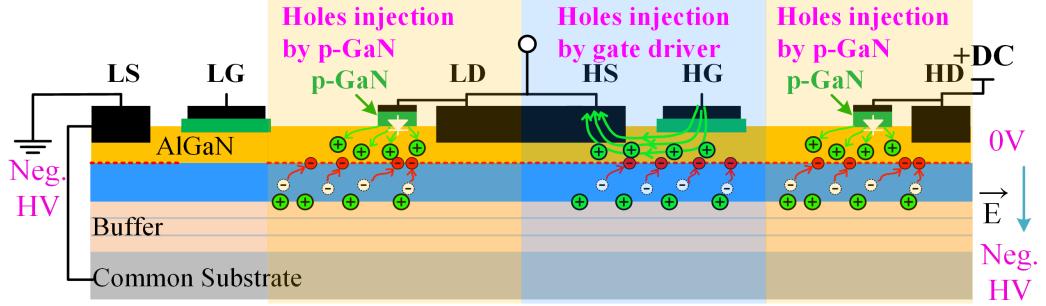


**Figure 3.4:** Holes Injection by p-GaN at Drain Region for Single GaN Transistors.

positively biased (dc-link voltage) at off state, like a PN junction shown at the p-GaN region of Fig. 3.4(b). The experimental results showed complete elimination of the  $R_{dson}$  degradation phenomena for the single GaN transistor [56].

For the monolithically integrated GaN half-bridge, if the common substrate is grounded, the source region of the high-side device will experience static negative bias effect. But it is not effective for injecting holes through p-GaN at source region. The reason is that the p-GaN will not have sufficient positive bias voltage.

During on state, gate current can be controlled by the gate driver. Therefore, the holes injection can be achieved by injecting more current through gate contact, as shown in Fig. 3.5. The additional gate current increases the positive charges at the source region, attracting the trapped electrons transit back to 2DEG. Thus, the  $R_{dson}$  degradation is mitigated. It should be noted that the gate current cannot be too large, otherwise the gate overcurrent thermal failure may occur. Thus, the gate

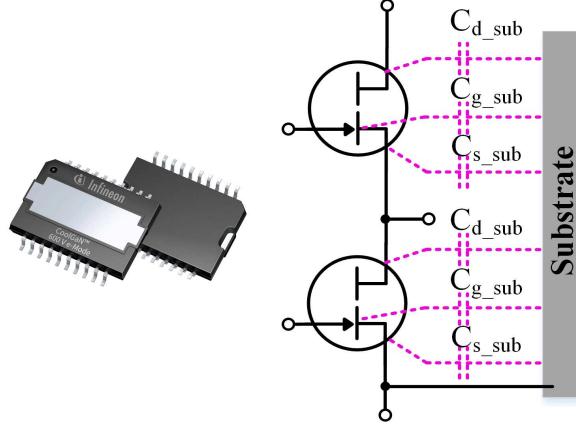


**Figure 3.5:** Holes Injection from the High-side Gate Contact at High-side On State.

current level should be carefully modulated, and additional gate current should only be injected at problematic period ( $R_{dson}$  degradation period) to avoid thermal issue. For the half-bridge configuration, there are two switching states (hard-switching and soft-switching). For each switching state, the problematic period is different. In Section III, the holes injection strategy will be demonstrated for both hard-switching scenario and soft-switching scenario.

### 3.2 $R_{dson}$ Degradation Phenomena Analysis and Its Basic Solutions at Different Operating Conditions in Monolithic GaN Half-bridge

In this section, the monolithic GaN half-bridge under test will be introduced firstly. After that, the  $R_{dson}$  degradation phenomena for soft-switching scenario and hard-switching scenario will be demonstrated. The main difference of two switching conditions is the load current direction when the high-side switch turns on. This current direction is found to play an important role in the  $R_{dson}$  degradation. Based on the phenomena, the corresponding gate current modulation strategies are proposed, respectively.



**Figure 3.6:** Monolithic GaN Half-bridge Under Test and Its Circuit Model.

### 3.2.1 Device Under Test (DUT)

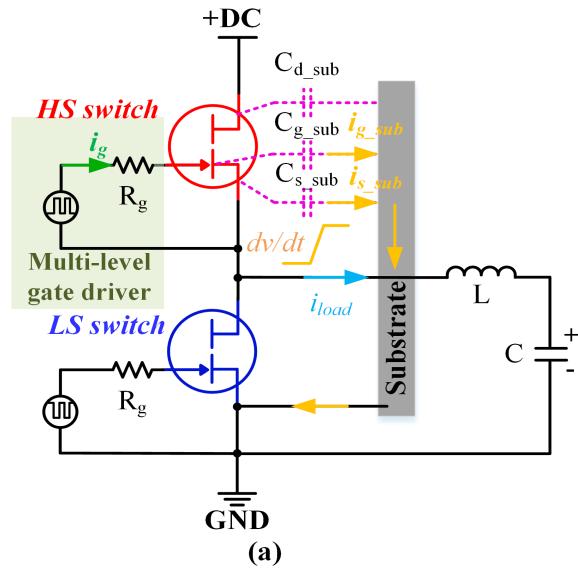
The device used in this research is a normally-off GaN Gate Injection Transistor (GIT) from Infineon Technologies, with intentionally separated source and substrate. The same discrete die with connected source and substrate has been used in a commercial discrete device [158]. The voltage and current rating of the half-bridge sample is 600 V/20 A. The steady on state gate current for this GIT is 20 mA, which is corresponding to the  $V_{gs}$  voltage of 3.5 V [158]. The picture and circuit model of the monolithic GaN half-bridge are shown in Fig. 3.6. It should be noted that there are gate/drain/source-to-substrate parasitic capacitors in the common substrate configuration. These parasitic capacitors will induce displacement current during switching  $dv/dt$  transient. The impact of these displacement current will be analyzed in the following paragraphs.

### 3.2.2 Soft-switching Scenario and Corresponding Solution

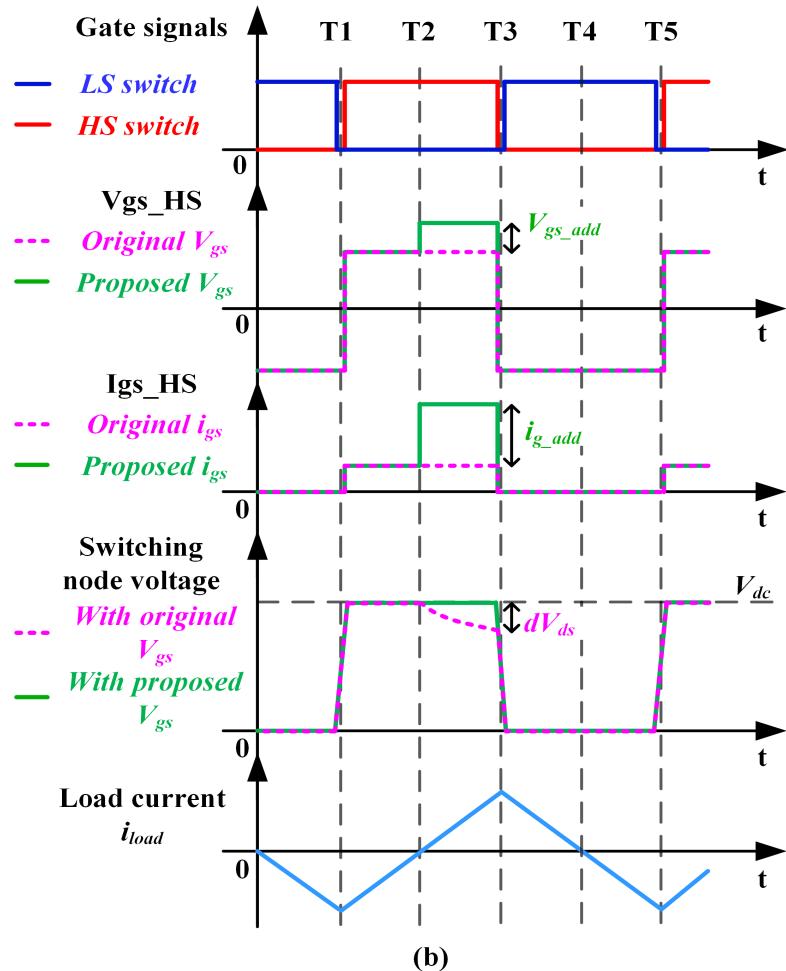
The schematic of the soft-switching test and its typical waveforms are shown in Fig. 3.1. The switch node of the half-bridge is connected to a LC network to generate

an alternating inductive load current. As shown in Fig. 3.7(b), at the first half of the high-side device on period (T1-T2), the load current is injecting into the source region of the high-side switch. In Fig. 3.7(b), the switch node voltage is near dc-link voltage, which represents that there is little voltage drop on the  $R_{dson}$  of high-side device. The  $R_{dson}$  degradation does not occur at this period. As shown in Fig. 3.8, this phenomenon can be explained that from T1 to T2, the load current injecting into the high-side device provides additional holes to the source region. These additional holes attract the trapped electrons releasing back to 2DEG. Thus, the  $R_{dson}$  degradation is suppressed. At the second half of the high-side switch on period (T2-T3), the switch node voltage drops dramatically. It is because the load current (original holes supplier) changes direction, no longer injecting holes to the source region. Thus, the electrons trap in the buffer layer again, and the  $R_{dson}$  degradation happens. The degradation level increases with the bias voltage amplitude.

When the direction of the load current changes during T2 to T3 in Fig. 3.7(b), the additional holes cannot no longer be provided from the load current. If the gate current can be injected during this time to continue providing additional holes to the source region, the  $R_{dson}$  degradation should be mitigated. The proposed gate voltage and gate current profile is plotted in solid green line in Fig. 3.7(b). At the first half on period (T1-T2), the gate current level is the same as the original case (dashed purple line). When the device current changes direction at T2, the additional gate current will be injected to suppress the static negative substrate bias effect. The detailed implementation considerations and gate current amplitude calculations will be included in section IV.

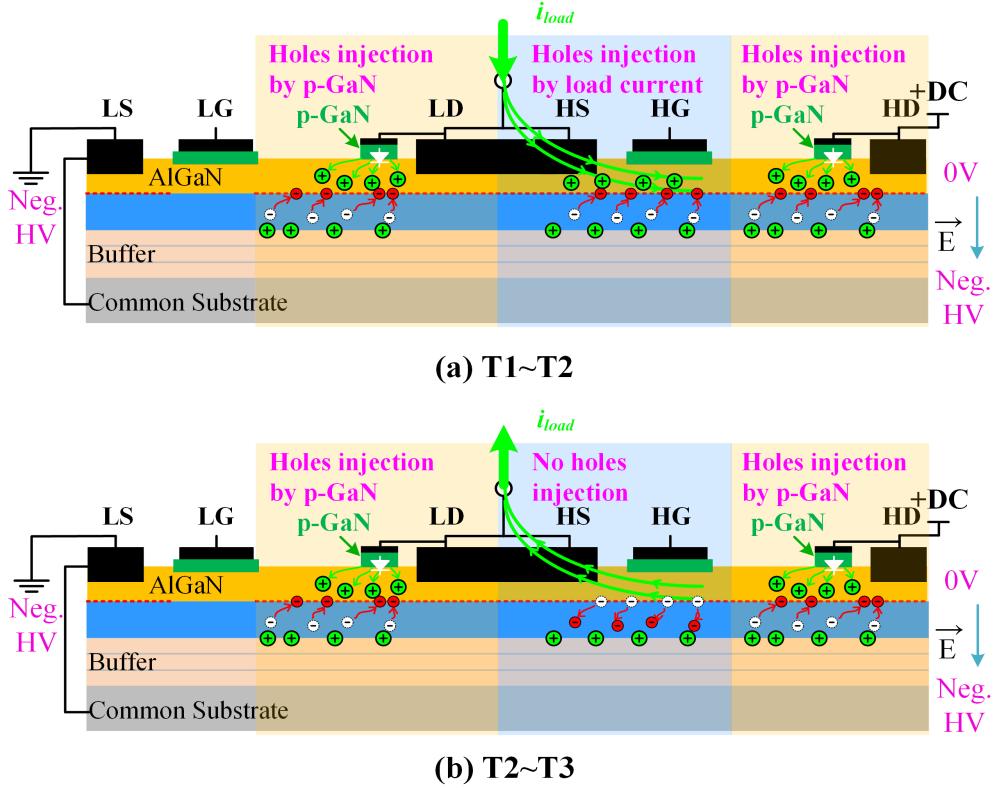


(a)



(b)

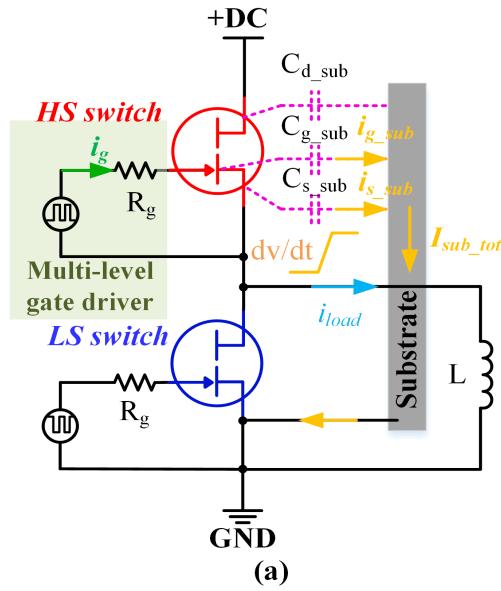
**Figure 3.7:** Schematic of the Soft-switching Test and Its Typical Waveforms.



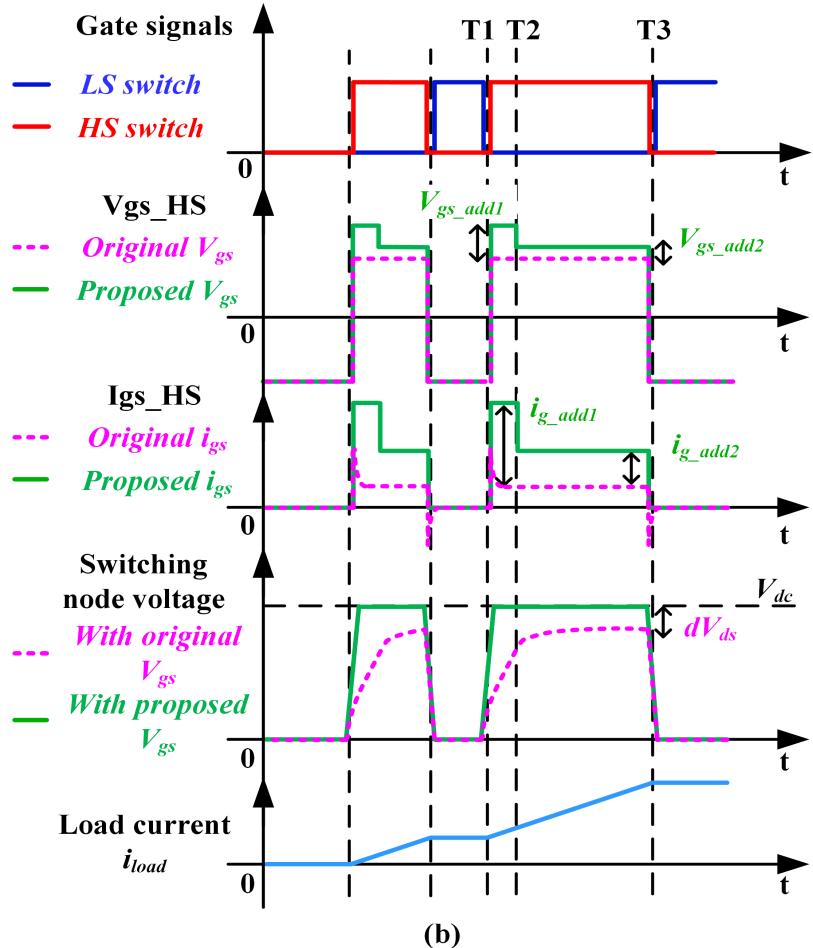
**Figure 3.8:** Electrons Trapping Phenomena Under Soft-switching Condition Without Proposed Gate Current Injection Scheme.

### 3.2.3 Hard-switching Scenario and Corresponding Solution

The schematic of the hard-switching test and its typical waveforms are shown in Fig. 3.9. The high-side device current is uni-directional, from drain to source. There are not additional holes supplied from the load current side. Therefore, the  $R_{ds(on)}$  degradation happens at the beginning of the high-side device turn-on period. The  $V_{ds}$  voltage drop of high-side switch is the subtraction of dc-link voltage and switch node voltage, as the dashed purple line shown in Fig. 3.9(b). This voltage drop represents the  $R_{ds(on)}$  of the high-side switch. From T2 to T3 in Fig. 3.9(b), the  $V_{ds}$  voltage drop of high-side switch will be big at the beginning and gradually decrease. It is because at the beginning, the  $V_{ds} dv/dt$  induces the gate-to-substrate displacement current.



(a)

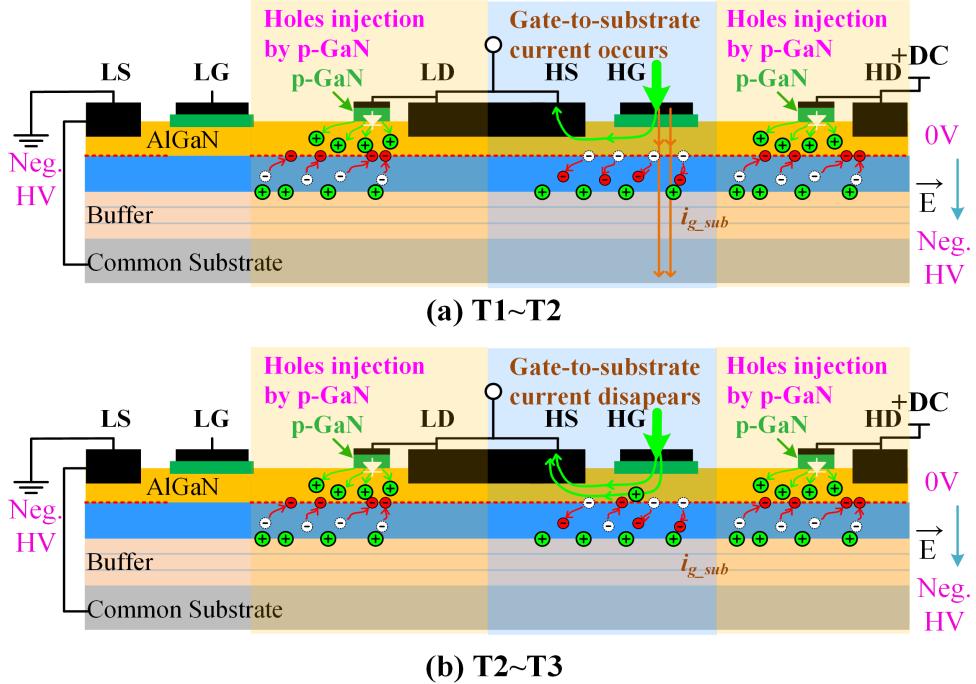


(b)

**Figure 3.9:** Schematic of the Hard-switching Test and Its Typical Waveforms.

Thus, one part of the gate current flow through the gate-to-substrate capacitor to the substrate, as  $I_{g,sub}$  shown in Fig. 3.9(a). This process in device level without proposed gate current injection scheme is shown in Fig. 3.10. During the high-side switch turn-on transient time (T2-T3), the effective holes providing to the source region are only part of the gate current. After the  $V_{ds} dv/dt$  transient (T3-T4), all of the gate current (holes) flows to the source region. Since more holes are injected from the gate to the source region, the  $R_{dson}$  degradation level decreases. Without proposed gate current scheme, the  $R_{dson}$  degradation is big and lasts for the whole on state. It will introduce huge conduction loss and may cause thermal failure of the high-side device.

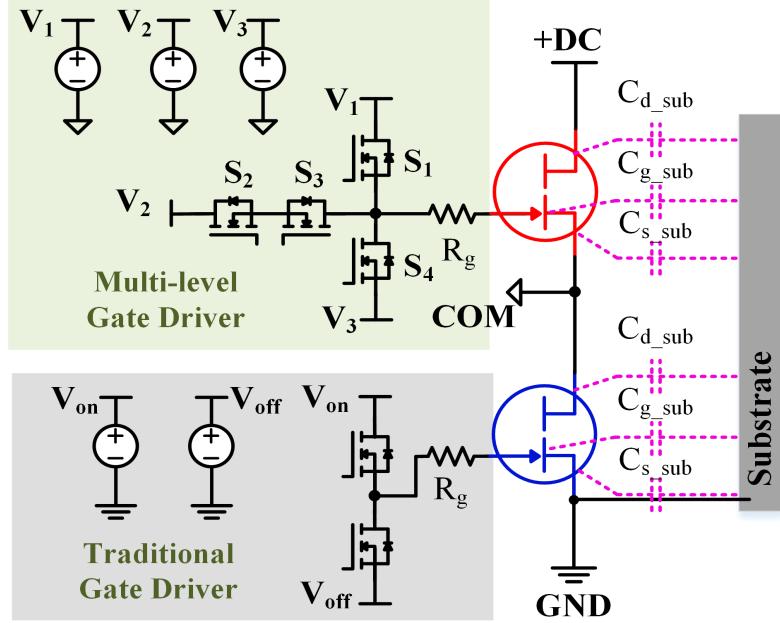
This phenomenon can be solved by injecting large gate current at the whole turn-on period of high-side switch. At the beginning of the turn-on process, because of the  $V_{ds} dv/dt$  transient, part of the gate current flows to the substrate, making the effective gate-to-source current small. Thus, a higher gate current should be injected to compensate the transient gate-to-substrate displacement current, as the solid green line shown in Fig. 3.9(b). Afterwards, a relatively small gate current can be injected to provide sufficient holes to the source region. The main consideration of decreasing the gate current after switching transient is the gate thermal stress. If the gate current amplitude remains high throughout the whole on period, the  $R_{dson}$  of the device will be smaller, but the gate may experience thermal breakdown. The proposed gate current modulation profile is plotted as the solid green line in Fig. 3.9(b). Basically, the gate current amplitude will be higher than that of low-side switch to suppress the static negative substrate bias effect. The design of the current amplitude should be based on the device gate thermal stress and the induced gate-to-substrate displacement current. The detailed design guideline of the additional gate current amplitude and time length will be presented in Section 3.3.



**Figure 3.10:** Electrons Trapping Phenomena Under Hard-switching Condition Without Proposed Gate Current Injection Scheme.

### 3.3 Operation Principle and Practical Implementation of Proposed Multi-level Gate Driver

In this section, a multi-level gate driver to achieve the proposed gate current profile will be demonstrated in detail. Although the higher gate current leads to smaller  $R_{dson}$  degradation, the gate thermal failure is found if the injected gate current is too big. Therefore, the gate thermal failure will be investigated to determine the upper limit of the gate current root-mean-square (RMS) value. Afterwards, the gate current design guideline will be explained for soft-switching scenario and hard-switching scenario, respectively. Finally, the components selection and practical hardware design considerations are present.



**Figure 3.11:** Schematic of Proposed Three-level Gate Driver.

### 3.3.1 Multi-level Gate Driver Operation Principle

The proposed multi-level gate driver is shown in Fig. 3.11. It can basically output three gate voltage levels depending on the gate driver power supply. Based on the gate current vs. gate voltage curve of the single GaN GIT sample in [158], if the gate voltage and gate resistor are determined, the gate current value can be easily acquired. The switching states for the three levels are listed in Table 3.1.

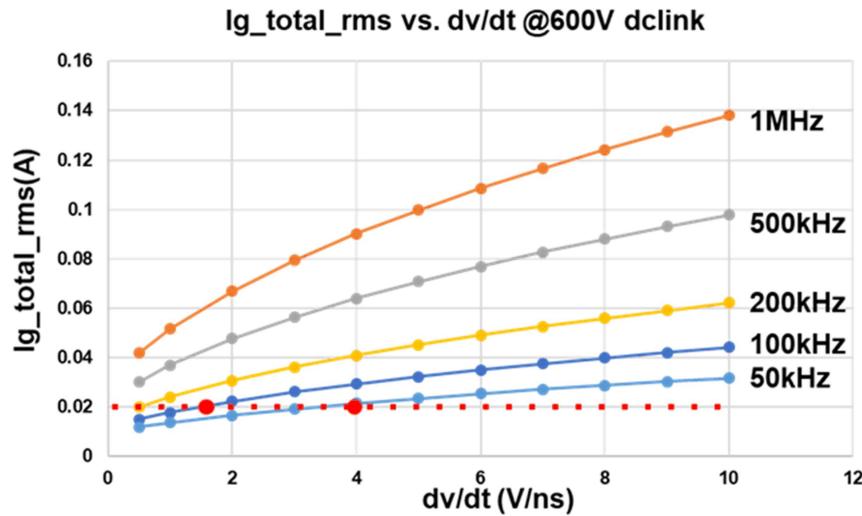
**Table 3.1:** Switching States of Proposed Three-level Gate Driver.

Switching State	$S_1$	$S_2$	$S_3$	$S_4$	Output Voltage
<b>ON State 1</b>	1	0	0	0	$V_1$
<b>ON State 2</b>	0	1	1	0	$V_2$
<b>OFF State</b>	0	0	0	1	$V_3$

### 3.3.2 Practical Implementation Considerations

In the monolithic GaN half-bridge configuration, the switch node  $dv/dt$  is applied to the high-side gate to substrate parasitic capacitor. This  $dv/dt$  will draw large displacement current from the gate. The gate-to-substrate parasitic capacitance of the high-side switch is 80pF, measured by the Impedance Analyzer.

#### a. Gate Thermal Failure Investigation



**Figure 3.12:** Gate Total RMS Current  $I_{g,\text{rms}}$  Relationship With Switching Node  $dv/dt$  and Switching Frequency.

As mentioned above, the additional gate current injection can improve the  $R_{\text{dson}}$  of the channel. However, the gate cannot take infinite gate current because there will be a thermal gate current limit. Therefore, the gate current thermal failure is investigated by injecting different gate current amplitude and current pulse length. The theoretical calculated data (solid line) and test data (red dashed dots) are shown in Fig. 3.12. The gate current comprises of two parts, the gate-to-source current  $I_{gs}$  and the gate-to-substrate current  $I_{g,\text{sub}}$ . The  $I_{gs}$  is determined by gate voltage  $V_{gs}$

and the  $I_{g,\text{sub}}$  is determined by the gate-to-substrate parasitic capacitance and switch node  $dv/dt$ . The thermal failure is related to the RMS value of the total gate current  $I_{g,\text{rms}}$ .

$$I_{g,\text{rms}} = \sqrt{I_{\text{gs},\text{rms}}^2 + I_{\text{g},\text{sub},\text{rms}}^2} \quad (3.1)$$

$$I_{\text{gs},\text{rms}} = f(V_{\text{gs}}) \quad (3.2)$$

$$I_{\text{g},\text{sub},\text{rms}} = \frac{\sqrt{\int_0^{T_{sw}} (C_{g,\text{sub}} \cdot \frac{dV_{ds}}{dt})^2 dt}}{T_{sw}} \quad (3.3)$$

$$W_{\text{g},\text{loss}} = \sqrt{\int_0^{T_{sw}} (I_{\text{gs},\text{rms}}^2 \cdot R_{\text{g},\text{term}}) dt} \quad (3.4)$$

where  $I_{g,\text{rms}}$  is the rms value of total gate current,  $I_{\text{gs},\text{rms}}$  is the rms value of gate-to-source current,  $I_{\text{g},\text{sub},\text{rms}}$  is the rms value of total gate-to-substrate current,  $C_{g,\text{sub}}$  is the gate-to-substrate capacitance,  $T_{sw}$  is the switching period,  $W_{\text{g},\text{loss}}$  is the energy dissipated at gate,  $R_{\text{g},\text{term}}$  is the gate internal resistance, which is related to the substrate-to-channel bias voltage and the gate material.

The gate rms current is changed by changing the switching frequency, switch node  $dv/dt$  or external gate resistor. All the experimental results shows that at 600 V dc-link voltage, if the gate total rms current is bigger than 0.021 A, the high-side device will have gate thermal breakdown. As a result, the gate-source-substrate is short-circuit.

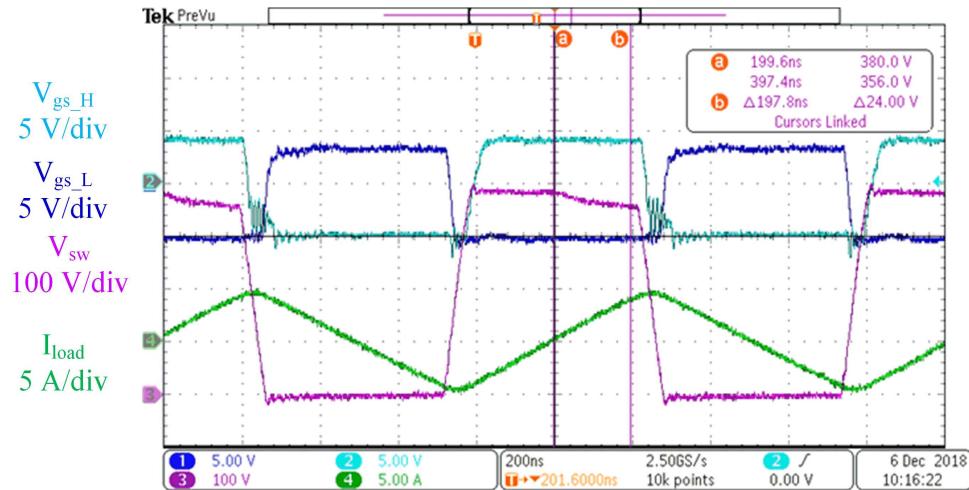
## b. Gate Current Amplitude Design

The gate current amplitude would be designed based on the upper limit of the gate total rms current. For different scenarios, the time length of the high level gate current is different.

At soft-switching scenario, the high level gate current should be applied whenever the  $I_{ds}$  flow from source to drain. Thus, the total gate rms current should be calculated per the converter operation condition. At hard-switching scenario, the high level gate current should be applied only at the beginning of the on state to help release the trapped electrons.

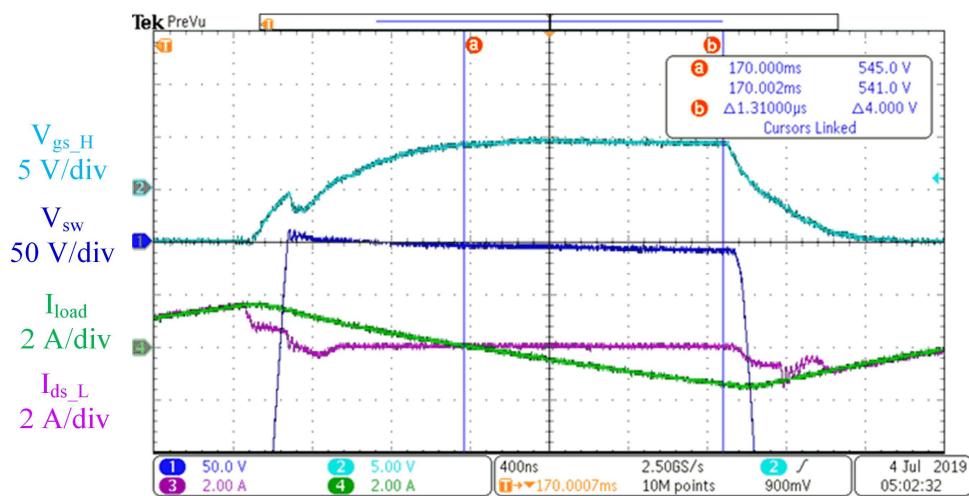
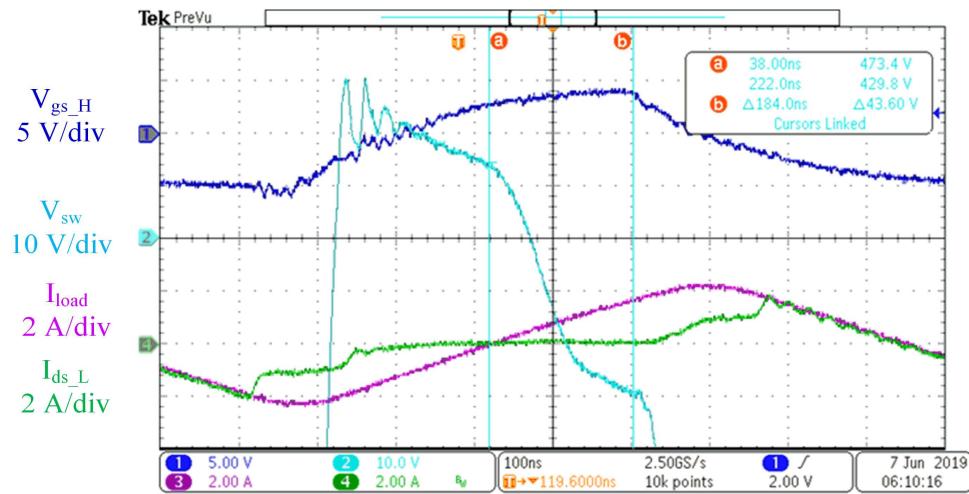
### 3.4 Experimental Results Analysis

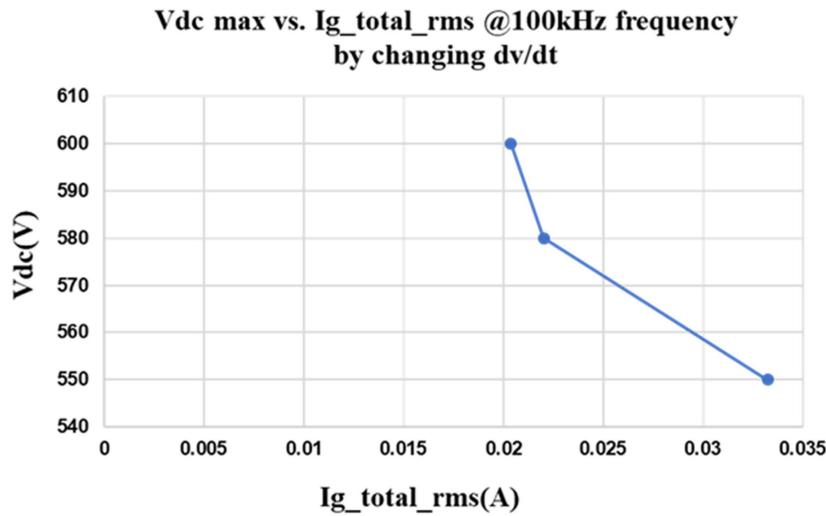
#### 3.4.1 Soft-switching Scenario



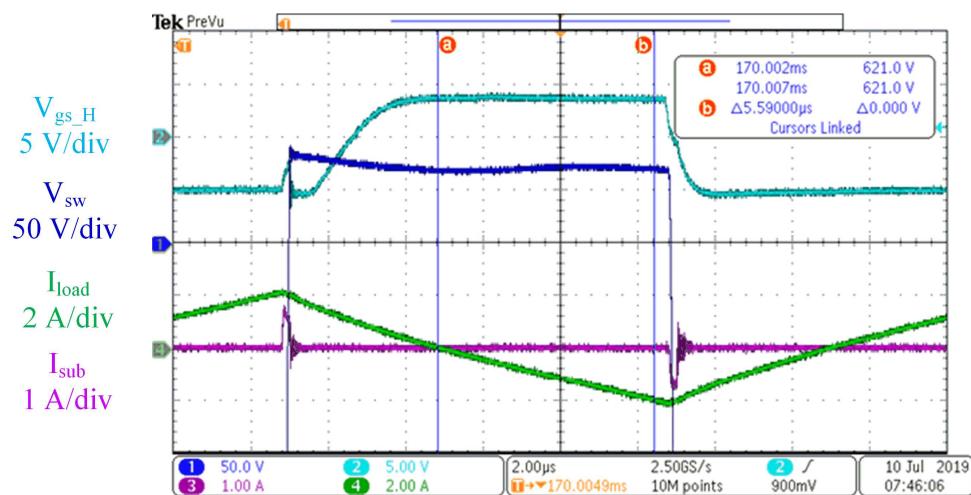
**Figure 3.13:** Soft-switching Scenario at 380 V Dc-link Voltage With One Level Low Gate Current.

The soft-switching test is conducted according to Fig. 3.7(a). When the single level gate on-state gate current is applied, the switch node voltage is normal and keep nearly equal to the dc-link voltage at the forward load current direction (channel current from drain to source). There is a large voltage drop when the current changes direction. In Fig. 3.13, the equivalent  $R_{dson}$  of the high-side device is around  $6 \Omega$  at only 380 V dc-link voltage, which generates large amount of losses. As the dc-link voltage increases as Fig. 3.14, the voltage drop becomes bigger and the equivalent





**Figure 3.16:** Relationship Between Maximum Dc-link Voltage and Gate Total RMS Current.



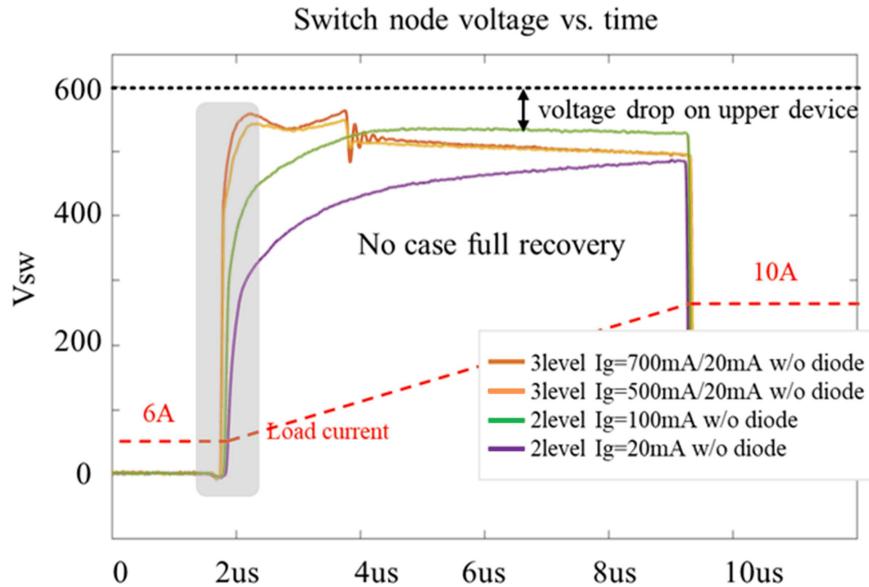
**Figure 3.17:** Soft-switching Scenario at 600 V Dc-link Voltage With Proposed Three Level Gate Current.

$R_{dson}$  reaches  $24 \Omega$  at  $480$  V dc-link voltage. The device fails if the dc-link voltage increases further. It is because the huge conduction loss is generated even at very low load current level. When the high gate current is injected during the reverse load current period, the  $R_{dson}$  degradation is largely mitigated. However, since the gate rms current is too big, the gate is breakdown due to the high gate contact temperature. The device gate fails at  $540$  V, as shown in Fig. 3.15. Thus, the series of gate second level current amplitude is investigated. The relationship of gate current and maximum dc-link voltage is shown in Fig. 3.16. If the gate rms current is under  $0.021$  A, the dc-link voltage can successfully reach the device rating voltage without failure. Fig. 3.17 shows one case of the typical experiment waveforms with additional gate current injection. With lower than  $0.021$  A gate total rms current, the dc-link voltage can reach  $620$  V without any gate failure. Therefore, the proposed method can mitigate the  $R_{dson}$  degradation caused by the substrate bias and keep the device in safe operation area.

### 3.4.2 Hard-switching Scenario

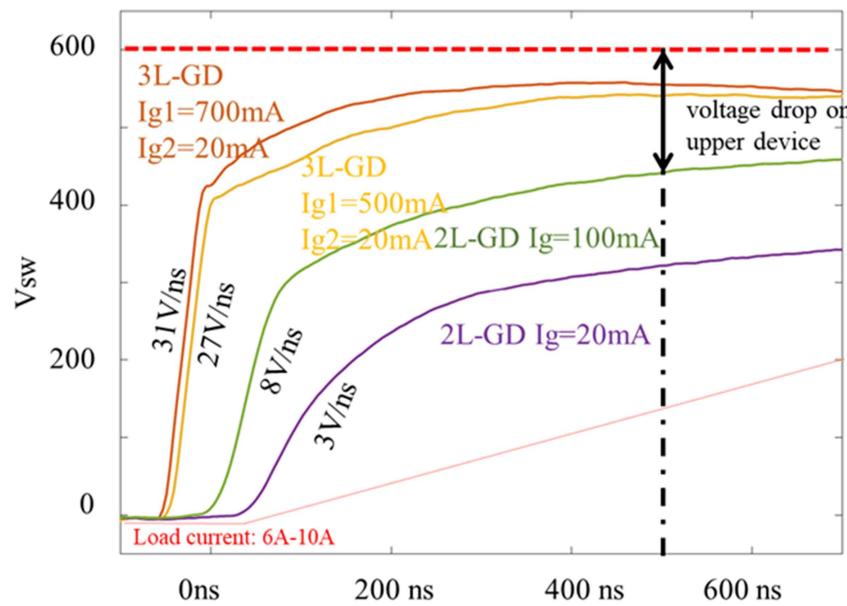
The hard-switching test is conducted according to Fig. 3.9(a). Fig. 3.18 shows the experimental results when the substrate is directly grounded. Since this is the double pulse test, the thermal stress is low and the voltage drop can be over  $100$  V without failure. For the traditional two level gate driver, there is a very large voltage drop ( $\gtrsim 150$  V) when the gate current is at the normal level of single device ( $20$  mA). Thus, the equivalent  $R_{dson}$  of the high-side channel is several tens of ohms. The  $R_{dson}$  degradation gradually recovers as the on-state time increases. However, since the gate current is at normal single device driving level, which is not sufficient for the monolithic high-side switch, the  $R_{dson}$  is still very large at  $10 \mu s$  after turn-on. When the gate current is increased to  $100$  mA, the  $R_{dson}$  degradation is improved. However,

the gate current cannot increase further because this high gate current is applied during the whole on period. When the three level gate current is applied, the gate current can be 700 mA at the start of turn-on and decreases to 20 mA afterwards. This three level gate current releases the stress of the gate and meanwhile helps the  $R_{dson}$  recovery. The  $dv/dt$  of the switch node voltage increases 10 times when the three level gate current is applied, as shown in Fig. 3.19. Although this three level gate current strategy can help recover the  $R_{dson}$  of high-side channel, the  $R_{dson}$  is still large and unacceptable.

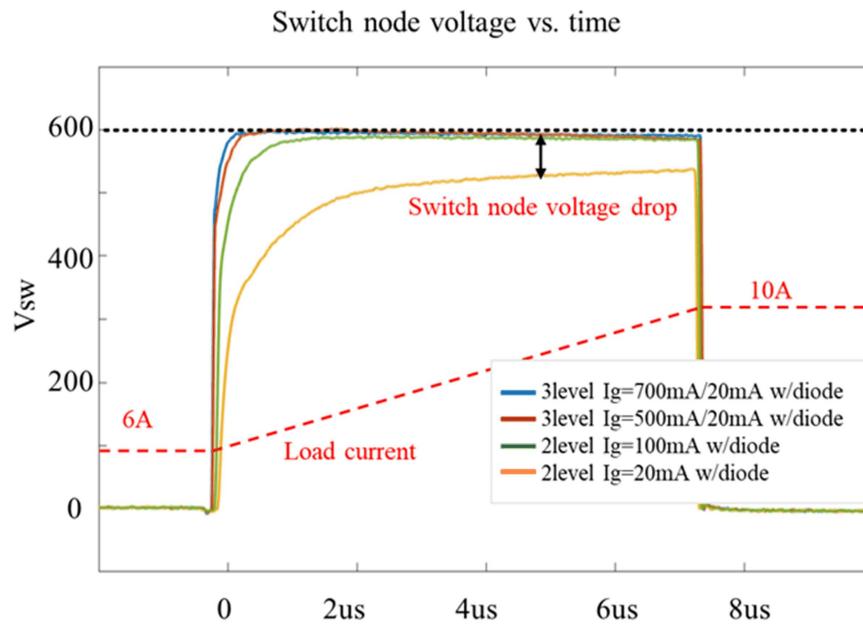


**Figure 3.18:** Switching Node Voltage at High-side Turn-on With Grounded Substrate Under Hard-switching Scenario.

In order to fully recover the  $R_{dson}$  degradation, a diode is inserted between substrate and ground. This diode can elevate the voltage potential of the substrate when the high-side device turns on, because the high-side to substrate displacement current charges the junction capacitance of this diode during the switch node  $dv/dt$  transient. In this way, the voltage bias between high-side channel and the substrate is reduced. As shown in Fig. 3.20, the  $R_{dson}$  degradation can be further mitigated



**Figure 3.19:** Zoom-in View of Switch Node Voltage at High-side Turn-on With Grounded Substrate Under Hard-switching Scenario.



**Figure 3.20:** Switch Node Voltage During High-side Turn-on With Inserted Blocking Diode Between Substrate and Ground Under Hard-switching Scenario.

by the inserted diode. Because the junction capacitor of the diode is actually used in this method, it would be also effective if the capacitor is inserted. However, it should be noted that the diode (P-N junction) is easy to be inserted between substrate and ground through semiconductor process. Therefore, the diode insertion is better than the capacitor insertion. To sum, the three level gate current is not sufficient to fully recover the  $R_{dson}$  degradation. With the diode insertion between substrate and ground, the voltage bias of substrate and ground is deceased. Therefore, the three level gate current with diode insertion can fully solve the  $R_{dson}$  degradation issue for the hard-switching scenario.

### 3.5 Conclusions

In this chapter, the 2nd level monolithic integration of GaN GITs is investigated. Because of the lateral structure, the multiple GaN transistors are convenient to integrate in a single substrate. This integration can minimize the parasitic inductance in a large extent and saves processing steps of semiconductors. The substrate of the single device is usually connected to the source contact, avoiding any large substrate voltage between gate and substrate. Half-bridge integration with single substrate faces substrate bias effect because the high-side gate will have dc-link voltage bias during the on-state. With this dynamic or static substrate bias, the electrons trap occurs at the high-side 2DEG and the conduction path becomes highly resistive. This is called  $R_{dson}$  degradation. This chapter investigates the circuit solutions of this issue. It is found that excessive gate current injection during the  $R_{dson}$  degradation time can help improve the 2DEG conduction resistance. However, the gate material will thermal breakdown if the gate current is too big. Therefore, the three level gate driver is proposed. The high-level current is only at the problem area and the normal gate current is applied at the rest of the on state, which mitigates the thermal stress

of the gate. The causes of the electrons trap are different at hard-switching scenario and at soft-switching scenario. Thus, two different gate driving profiles are proposed for these two scenarios respectively. The additional gate current can completely solve the  $R_{\text{dson}}$  degradation at soft-switching scenario. As for the hard-switching scenario, only high gate current is not enough. With additional semiconductor PN junction between substrate and ground, the bias between high-side gate to substrate reduces from dc-link voltage to nearly half of the dc-link voltage. In this way, the proposed three level gate driving scheme can fully recover the  $R_{\text{dson}}$  degradation at hard-switching scenarios.

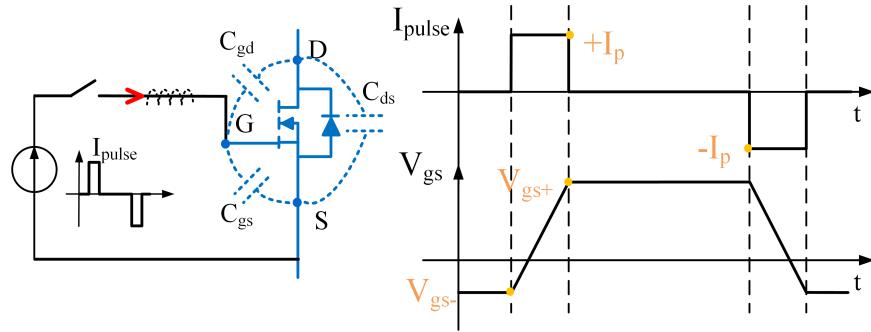
The circuit solution of the monolithic GaN half-bridge provides a useful understanding of the  $R_{\text{dson}}$  degradation issues. The future work would be focused on the GaN semiconductor technological improvement. The findings in this research provides constructive directions to improve the technological design of the GaN transistors. The potential solutions in semiconductor point of view could be 1. Improve the GaN buffer quality to reduce the electrons trapping into the buffer; 2. Insert P-N junction between the low-side source (ground) and substrate; 3. Increase the buffer thickness to reduce the gate to substrate capacitance; 4. Improve the gate materials to sustain higher gate rms current.

## VOLTAGE BALANCING AND SHORT CIRCUIT PROTECTION FOR SERIES-CONNECTED SiC MOSFETs

### 4.1 Voltage Balancing for Series-connected SiC MOSFETs

#### 4.1.1 Voltage Balancing Strategy 1: A Multi-winding Transformer Based Current Source Gate Driver with Highly Synchronized Gate Voltages

##### A. Basic Ideas of CS-GD



**Figure 4.1:** Basic Current Source Gate Driver Principles.

Fig. 4.1 shows the basic idea of the current source gate driver: The bi-polar pulse current charges and discharges  $C_{gs}$ . The pulse current amplitude and pulse width should be determined. The current pulse amplitude depends on the required  $V_{ds}$   $dv/dt$  if the drain-source current  $I_{ds}$  is determined. It is because the gate current at miller plateau voltage is the major factor that decides the  $dv/dt$  [159]. Therefore, if the required  $V_{ds}$   $dv/dt$  is designed based on the system considerations [160, 161], such

as EMI, system efficiency and the voltage overshooting limit, the corresponding gate current amplitude can be decided by two ways:

- 1 Calculate the gate current level at miller plateau voltage according to the curve of “ $V_{ds}$  rising/falling time vs. gate resistor” in the SiC device datasheet [150]. Gate current level at miller plateau voltage can be derived [159]:

$$\begin{cases} I_{gp,on} = \frac{V_{gs+} - V_{Miller}}{R_{g,on} + R_{int}} \\ I_{gp,off} = \frac{V_{Miller} - V_{gs-}}{R_{g,off} + R_{int}} \end{cases} \quad (4.1)$$

where  $I_{gp,on}/I_{gp,off}$  is on/off gate current when SiC MOSFET  $V_{gs}$  is at on/off miller plateau voltage;  $V_{gs+}/V_{gs-}$  is the on/off gate driving voltage;  $V_{Miller}$  is the miller plateau voltage;  $R_{g,on}/R_{g,off}$  is the on/off gate resistor;  $R_{int}$  is the device internal gate resistor.

The corresponding  $dv/dt$  can be calculated based on the datasheet test condition:

$$\begin{cases} (dv/dt)_{on} = \frac{V_{dc} \times 80\%}{t_f} \\ (dv/dt)_{off} = \frac{V_{dc} \times 80\%}{t_r} \end{cases} \quad (4.2)$$

where  $t_f$  and  $t_r$  are  $V_{ds}$  falling and rising time [150], respectively;  $V_{dc}$  is the dc-link voltage.

Therefore, at certain drain-source current level, the relationship between gate current at miller plateau voltage and  $V_{ds} dv/dt$  can be derived. Once the system  $dv/dt$  and  $I_{ds}$  are known, the gate current amplitude can be calculated.

- 2 Characterize the relationship between gate current and  $V_{ds} dv/dt$  using a double pulse test circuit [32] at given system operating voltage and current. By changing the gate pulse current value, the desired  $V_{ds} dv/dt$  can be acquired. This is similar to adjusting the gate resistance in a voltage source gate driver.

Another factor that affects the gate current amplitude is the miller current cancellation function. The expected effect is that  $V_{gs}$  can maintain a linear rise even at the original miller plateau. In this case, the gate current needs to have the same amplitude as the miller current, which is bigger than the  $V_{ds} dv/dt$  required gate current. In order not to affect the original designed  $dv/dt$ , an external  $C_{gs,ext}$  has been added to keep the current flowing into the real gate-source of the device the same as before. The final pulse current amplitude is expressed as 4.34.4:

$$I_{pulse} = C_{gd} \times (dV_{ds}/dt)_{max} \quad (4.3)$$

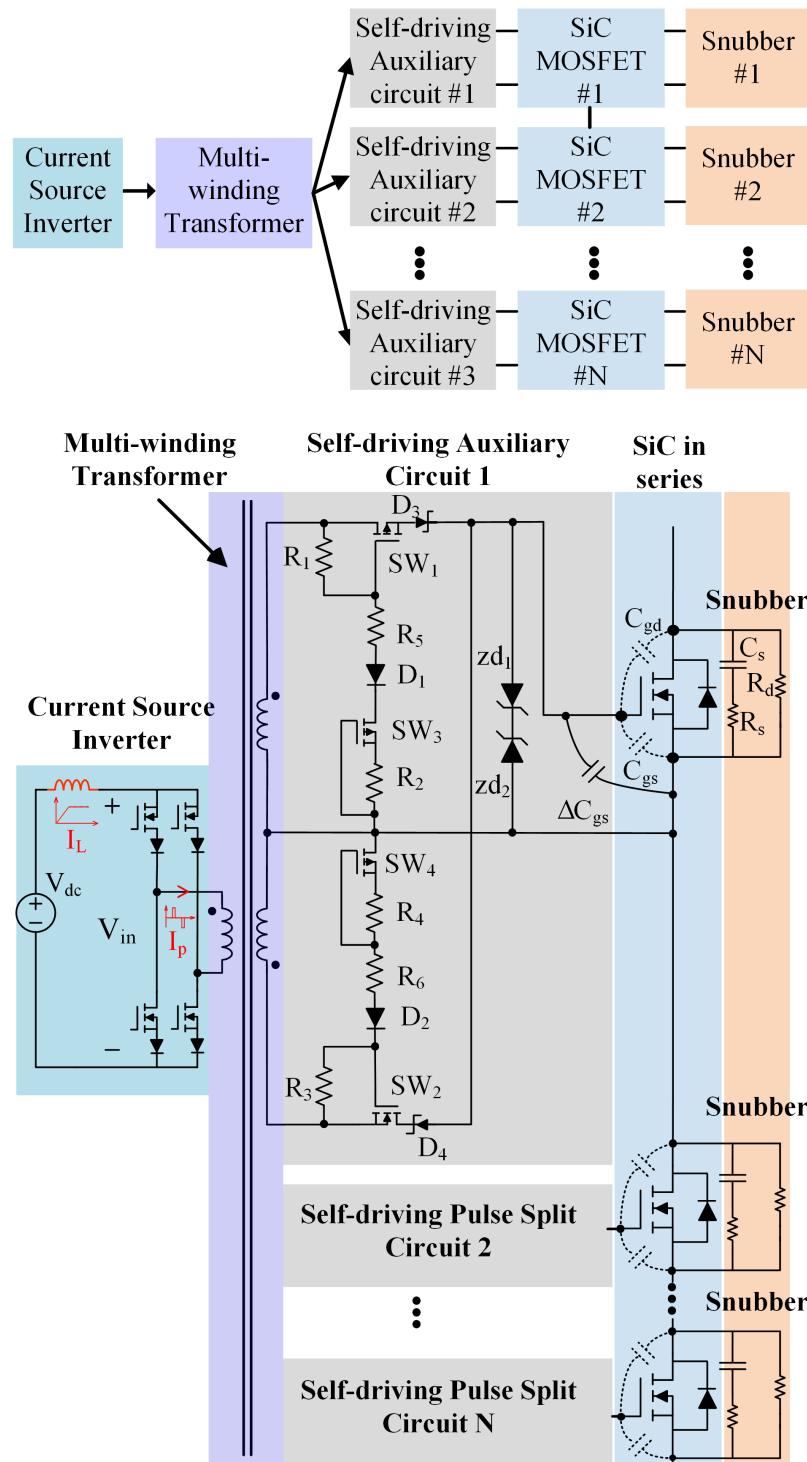
$$I_g = I_{pulse} \times \frac{C_{gs}}{C_{gs} + C_{gs,ext}} \quad (4.4)$$

where  $I_{pulse}$  is the final pulse current amplitude;  $I_g$  is the current flow into the device gate;  $C_{gd}$  is the miller capacitance;  $C_{gs}$  is the device gate source capacitance;  $C_{gs,ext}$  is the external gate-source capacitance.

The pulse width should be the  $V_{gs}$  rising and falling time. However, the problem of current source driver is that the gate voltage is not clamped. Therefore, two Zener diodes are used for positive and negative gate voltage clamping. The current pulse width should be long enough to guarantee that Zener diode enters the breakdown region (voltage clamping region).

## B. Proposed CS-GD circuit

Fig. 4.2 shows the proposed topology of the series-connected SiC MOSFETs block. It consists of four parts: The first part is current source inverter (CSI), in which the dc-link current is formed by a voltage source in series with an inductor. The CSI will generate current pulses. The second part is a multi-winding transformer with one primary winding and two secondary windings for each device channel. The third part



**Figure 4.2:** Topology of the Proposed Series-connected SiC MOSFETs Block.

is the self-driving auxiliary circuit. This circuit can conduct positive and negative current pulses and block the  $C_{gs}$  from discharging. The fourth part is the snubber circuit. It is used to compensate the power loop differences and device part-to-part difference.

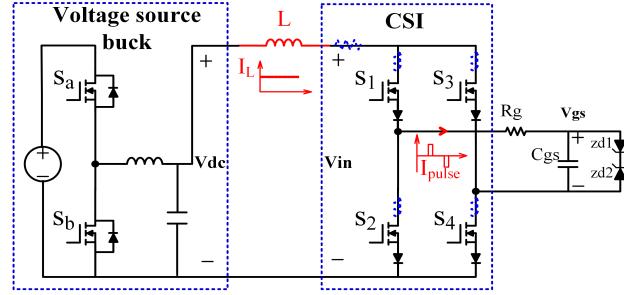
The following three subsections will explain the operation principle of CSI, multi-winding transformer and self-driving auxiliary circuit, respectively.

## 1 CSI Operation Principle

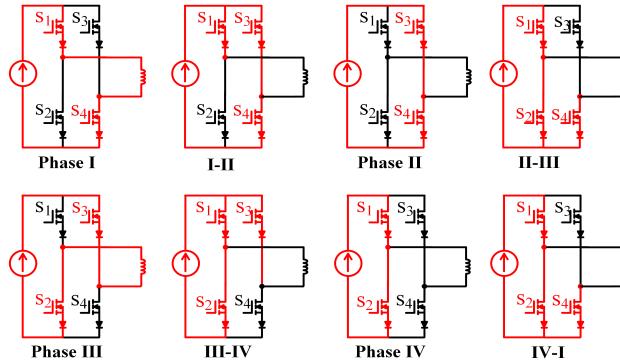
The CSI generates the positive and negative current pulses with desired amplitude and pulse width. The current pulse generation consists of two stages: 1. Inductor current  $I_L$  pre-charge; 2. Pulse generation. The equivalent load for the CSI is shown in Fig. 4.3(a). A buck converter is used to provide  $V_{dc}$ . The CSI has four switching states: two active states (diagonal switches on) which generates positive and negative pulses and two zero states (shoots through anyone of the phase legs).

At pre-charge stage, the CSI is at zero state where  $V_{dc}$  charges the inductor  $L$  to the designed current value  $I_L$ . After that, the CSI enters pulse generation stage. The operation procedure at this stage can be divided into four parts, as shown in Fig. 4.3(b):

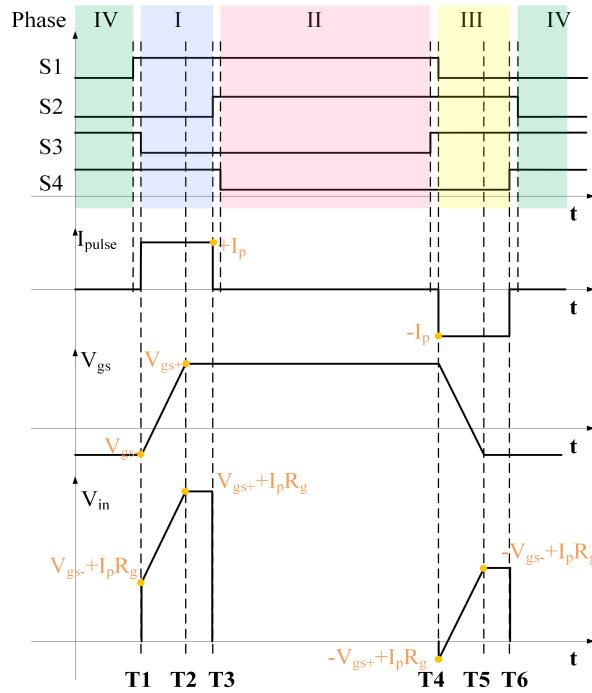
- 1) T1-T2: S1,S4 on and S2,S3 off. The positive current is charging  $C_{gs}$ . The voltage at the CSI input terminal  $V_{in}$  is the sum of  $V_{gs}$  and the voltage drop on the gate loop equivalent resistance  $R_g$ .
- 2) T2-T3: S1,S4 on and S2,S3 off. The  $V_{gs}$  reaches steady on-state voltage  $V_{gs+}$  at T2. The switching state does not change. The CSI continues providing positive current to  $C_{gs}$ , and  $V_{in}$  is still the sum of  $V_{gs}$  and the voltage drop on



(a) Equivalent circuit transformer secondary side converted to primary side



(b) CSI complete operation phases including deadtime



(c) CSI driving signals, input voltage  $V_{in}$  and SiC gate voltage

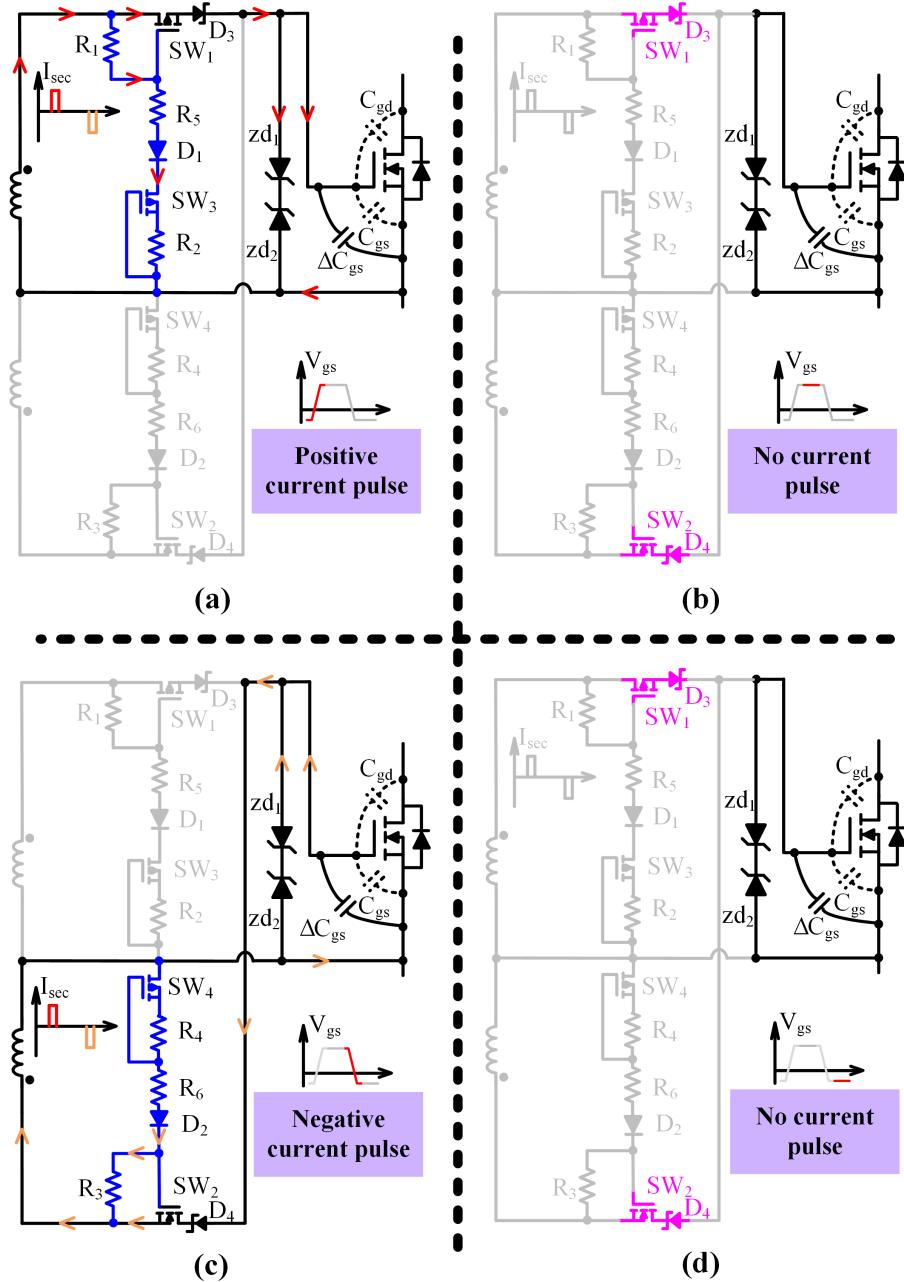
Figure 4.3: CSI Equivalent Circuit and Its Typical Waveforms.

$R_g$ . During this time period, the Zener diode zd2 conducts the pulse current and clamps the gate voltage.

- 3) T3-T4: S1,S2 on and S3,S4 off. The CSI does not output current at zero state. S1 and S2 are turned on to bypass the dc-link inductor current. The  $V_{in}$  is zero volt.
- 4) T4-T5: S2,S3 on and S1,S4 off. The CSI outputs negative current and  $C_{gs}$  is discharged linearly. The  $V_{in}$  becomes the sum of  $-V_{gs}$  and the voltage drop on the gate loop equivalent resistance  $R_g$ .
- 5) T5-T6: S2,S3 on and S1,S4 off. The CSI continues outputting negative current and the  $V_{gs}$  is clamped to the steady off-state voltage  $V_{gs^-}$  by Zener diode zd1. Since the switching state does not change, the  $V_{in}$  is still the sum of  $-V_{gs}$  and the voltage drop on  $R_g$ .
- 6) T6-T1: S3,S4 on and S1,S2 off. The CSI enters another zero state, and the  $V_{in}$  is clamped to zero volt by S3 and S4.

## 2 Multi-winding Transformer Operation Principle

The transformer used in this circuit is a multi-winding transformer for pulse operation and with high voltage insulation. There is one primary winding, and the number of secondary windings equals to the number of devices in the series-connected string. The turns ratio between the primary winding and each secondary winding is 1:1. The main function of the transformer is to equally transmit the bipolar pulse current to the gate of each SiC MOSFET. Meanwhile, it provides isolation among secondary windings and isolation between primary winding and each secondary winding. The design guideline of this special transformer will be explained in the next section.



**Figure 4.4:** Operation Principle of Secondary Self-driving Current Split Circuit.

### 3 Self-driving Auxiliary Circuit Operation Principle

If the secondary winding of the transformer is directly connected to the gate of SiC MOSFET, the  $V_{gs}$  cannot maintain steady state. It is because  $C_{gs}$  can be discharged through the transformer secondary winding. Thus, a switch should be implemented on the gate path to conduct pulse current and to block the  $C_{gs}$  discharging path. However, this active switch requires an isolated gate driver and an isolated power supply with an isolation level of kilo-volts. Additional synchronization error will be introduced by different propagation delay of the auxiliary driving circuit. To overcome this problem, a self-driving active switch circuit is proposed. The self-driving signal is generated by the existing current pulse, and no additional isolated gate driver and power supply are needed. The bipolar current pulses cannot generate uniform self-driving turn-on signals. Thus, the positive and negative current pulses are separated, and two self-driving switches are implemented for positive and negative current, respectively.

The proposed self-driving auxiliary circuit with four states is shown in Fig. 4.4. It is composed of two active switches and two symmetrical auxiliary gate driving circuits.

In Fig. 4.4, the diode  $D_1$  and  $D_1$  separate the positive and negative current pulses. The positive current pulse, as shown by red arrow, can only flow through the network in Fig. 4.4(a). The negative current pulse, as shown by orange arrow, can only flow through the network in Fig. 4.4(c). The normal operation procedure is explained as (a)(b)(c)(d) in Fig. 4.4:

#### 1) Normal Operation Procedure

- (a) Positive current self-driving operation The positive current pulse flows through the auxiliary gate network  $R_1-R_5-D_1-SW_3-R_2$ . The voltage drop on  $R_1$  forms

a negative gate driving voltage which turns on the P-channel MOSFET  $SW_1$ . This process happens during the current pulse rising edge. Once  $SW_1$  turns on, the main current will flow through  $SW_1-D_3$  to the gate of the SiC MOSFET. This auxiliary gate branch should not draw much main current. So, the depletion MOSFET  $SW_3$  and  $R_2$  are used to form a current limit unit. The current flowing through this unit will remain constant once the voltage across the unit exceeds certain voltage [132, 162]. The detailed design guideline will be shown in next section. The positive gate current will charge  $C_{gs}$  until the Zener diode zd2 clamps the gate voltage.

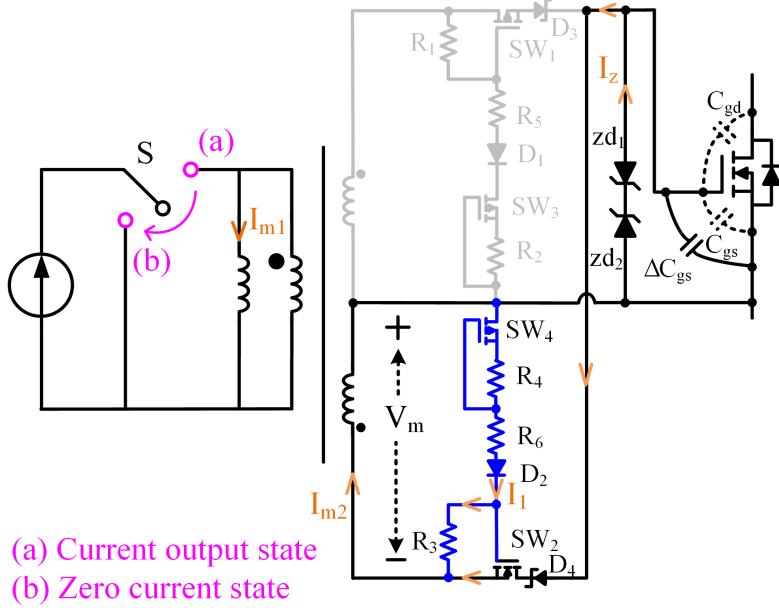
(b) Discharging path blocking After the positive current pulse, there is no current flowing through the auxiliary gate network  $R_1-R_5-D_1-SW_3-R_2$ . Thus, the gate voltage of  $SW_1$  is zero and  $SW_1$  is turned off automatically. During this time period, the  $SW_1-D_3$  and  $SW_2-D_4$  block the  $C_{gs}$  discharging path.

(c) Negative current self-driving operation Similarly, the negative current, as shown in orange in Fig. 4.4(c), flows through the auxiliary gate driving network  $R_3-D_2-R_6-R_4-SW_4$ . The voltage across  $R_3$  serves as the gate driving voltage of N-channel MOSFET  $SW_2$ . Once  $SW_2$  turns on, most of the negative current will flow through  $SW_2-D_4$  to  $C_{gs}$  of the SiC MOSFET. The current limit unit  $SW_4-R_4$  is the same as the  $SW_3-R_2$ .

(d) Discharging path blocking After the negative current pulse, the  $V_{gs}$  of the SiC MOSFET is at off-state gate voltage. Similar as state (b), once the pulse current disappears, the  $SW_2$  will be turned off automatically. The  $SW_2-D_4$  and  $SW_1-D_3$  will block the  $C_{gs}$  discharging path.

## 2) Transient Analysis (magnetizing current damping)

The  $R_5$  and  $R_6$  in the auxiliary gate driving circuit are to damp the transformer



**Figure 4.5:** Equivalent Circuit During the Transition From Positive Current Output State to Zero Current State (From a to b).

magnetizing current. This damping process happens during the transition from state (a) to state (b) and from state (c) to state (d), and it can be explained by the equivalent circuit after the pulse current. Fig. 4.5 shows the transition from state (a) to state (b).

The de-magnetizing process is explained as follows: At the positive pulse period (state a), the voltage across the transformer magnetizing inductor  $L_m$  is positive, and the magnetizing current  $I_{m1}$  will increase. Right after the positive pulse, S switches to state b, and the magnetizing current  $I_{m1}$  on the primary side decays to zero. Due to the flux continuation of the transformer, a current  $I_{m2}$  flowing into the dot is induced at the secondary winding. The direction of  $I_{m2}$  is the same as that of the negative current pulse. Thus,  $I_{m2}$  will flow through  $R_3$  and build up a positive gate voltage for  $SW_2$ . Because the magnetizing current is relatively small compared with the current pulse, the gate voltage of  $SW_2$  is

not high enough to fully turn on the device. The  $SW_2$  will work in saturation region and be partially on. Hence, the circuit  $SW_2 - D_4$  conducts part of the magnetizing current  $I_{m2}$ . The  $C_{gs}$  of the SiC MOSFET may be discharged, and the  $V_{gs}$  will drop. To mitigate this discharging effect, a reverse voltage  $V_m$  needs to be applied to the transformer winding to quickly diminish the magnetizing current in the negative current path. The  $V_m$  is equal to the voltage across the auxiliary gate branch (blue color in Fig. 4.5). Therefore, an additional resistor  $R_6$  is added in the auxiliary gate path to increase  $V_m$  and force the magnetizing current to drop faster. In this way, the  $C_{gs}$  discharging time is reduced.  $R_5$  in the positive auxiliary gate path is for the same reason.  $R_5$  and  $R_6$  can be in hundred  $\Omega$  range to form a reverse winding voltage to help damping the transformer magnetizing current. Since  $SW_2$  works in the saturation region, there is a relatively big voltage drop on  $SW_2$ . This is the reason that  $V_{gs}$  of the SiC MOSFET is not directly applied to the transformer winding during the magnetizing current damping. The Zener diode  $zd2$  works in breakdown region to provide a low impedance path for the discharging current. However, with the discharging current, Zener diode can only work at breakdown region for limited time [163]. Therefore, the magnetizing current should be quickly eliminated before Zener diode quits the breakdown region.

## C. Design Guideline of Proposed Circuit

### 1. CSI Design Guideline

For the CSI operation, three parameters should be determined: the input voltage  $V_{dc}$ , the pre-charge time  $T_{pre}$  and the inductor value  $L$ .

#### 1.1 Input Voltage $V_{dc}$ Design

A buck converter is used to provide  $V_{dc}$ . The value of  $V_{dc}$  depends on the volt-second balance of inductor L during one switching period. Since the detailed waveform of  $V_{in}$  in one switching period  $T_{sw}$  is known, as shown in Fig. 4.3(b),  $V_{dc}$  should be equal to the cycle-by-cycle average (CCA) value of  $V_{in}$  to guarantee the volt-second balance:

$$\int_0^{T_{sw}} (V_{dc}(t) - V_{in}(t)) dt = 0 \quad (4.5)$$

$$V_{dc} = \frac{1}{T_{sw}} \int_0^{T_{sw}} V_{in}(t) dt = \overline{V_{in}} \quad (4.6)$$

Based on the Fig. 4.3(b), the CCA value of  $V_{in}$  can be derived:

$$\overline{V_{in}} = \frac{2I_p R_g (T_x + T_z) + (V_{gs+} + V_{gs-}) T_z}{2(T_x + T_0 + T_z)} \quad (4.7)$$

$$T_{sw} = 2(T_x + T_0 + T_z) \quad (4.8)$$

where  $I_p$  is pulse current amplitude;  $R_g$  is the equivalent gate loop resistance;  $T_x$  is the  $V_{gs}$  rising/falling time of the SiC MOSFET (T1-T2 or T4-T5);  $T_z$  is the Zener diode clamping time (T2-T3 or T5-T6);  $T_0$  is the time without current (T3-T4 or T6-T1);  $T_{sw}$  is the switching period.

According to 4.6 4.7 4.8,  $V_{dc}$  is determined by the current pulse amplitude, pulse width, and pulse frequency. Once these three parameters change, the voltage source buck converter can be closed-loop controlled to change the output voltage  $V_{dc}$  accordingly to fulfill the inductor volt-second balance requirement.

## 1.2 Pre-charge Time $T_{pre}$ Design

The volt-second balance of the inductor ensures that the average inductor current remains at its initial value. And the initial inductor current is generated

through pre-charging. At the pre-charge stage, CSI is at zero state to let  $V_{dc}$  charge the inductor to the desired current value  $I_L$ . Since the current drives all the devices in one series string, its amplitude needs to be the sum of all the secondary gate currents. Thus, the pre-charge time can be expressed as:

$$T_{pre} = \frac{LI_p}{V_{dc}} \quad (4.9)$$

Where  $T_{pre}$  is the pre-charge time;  $I_p$  is the amplitude of the desired inductor current as expressed in 4.10.

$$I_p = N \times I_{pulse} \quad (4.10)$$

where  $N$  is the number of series-connected devices;  $I_{pulse}$  is the desired gate current amplitude determined by 4.14.24.34.4.

### 1.3 Dc-link Inductor Design

The inductor value is determined by the current ripple limit as expressed in 4.11.

$$L = \frac{V_{dc} \times T_0}{\Delta I_L} \quad (4.11)$$

where  $\Delta I_L$  is the inductor current ripple. Typically, the current ripple is  $\pm 5\%$  of the average current.

### 1.4 Design Considerations

An output voltage controlled buck converter is used to generate  $V_{dc}$ . The output current controlled buck converter is not suitable to provide dc-link for CSI. It is because the CSI input needs a constant voltage instead of a constant current to maintain the inductor volt-second balance. If the current-controlled buck converter provides  $V_{dc}$ , this  $V_{dc}$  can be regulated to an arbitrary value during

the load transient. It is because the regulation target of the current controlled buck converter is the output current, not the output voltage. If  $V_{dc}$  does not satisfy the volt-second requirement, the inductor current will change, and the buck converter needs to regulate again. Although it may finally stay at certain steady state with both correct current and voltage, it takes a long time. In addition, the transition from pre-charge stage to pulse operation stage is an abrupt load change (load from short circuit to  $C_{gs}$ ). The input voltage  $V_{dc}$  cannot change fast enough to make the inductor volt-second balance within one switching cycle after the transition. The output voltage-controlled converter can eliminate the dynamic transition oscillation, because  $V_{dc}$  is calculated in advance to make the inductor achieve volt-second balance in each switching cycle even at the start of the pulse operation state. However, unlike the flexible pre-charge time of current-controlled converter, voltage-controlled converter's pre-charge time should be carefully designed.

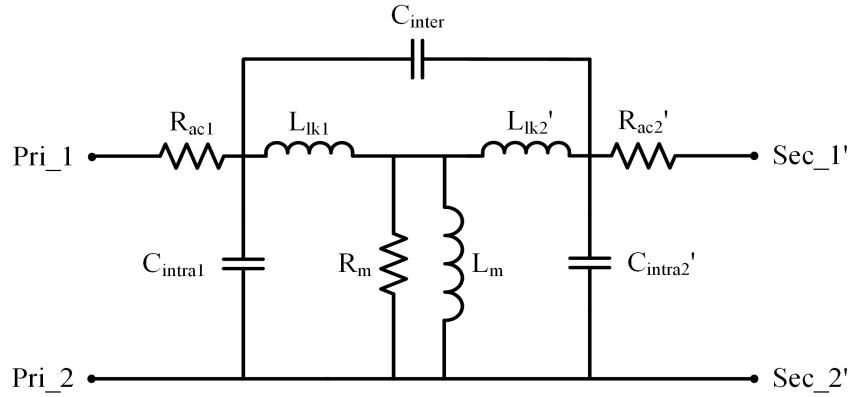
## 2. Multi-winding Transformer Design Guideline

### 2.1 Transformer Circuit Parameters' Influence on the Performance of Proposed CS-GD.

The lumped circuit model of a two-winding transformer is shown in Fig. 4.6. Although the transformer employed in the proposed CS-GD has three windings, the two secondary windings operate alternately. To simplify the analysis, a two-winding model is used [79]. The circuit parameters of the transformer and their effects on the proposed CS-GD are summarized as follows.

#### a. Loss related parameters.

$R_{ac1}$  and  $R_{ac2}$ ' represent the primary winding ac resistance and the secondary winding ac resistance referred to the primary side, respectively. Their values



**Figure 4.6:** Lumped Circuit Model of A Two-winding Transformer.

are related to the transformer winding loss. According to the operation of the transformer, only the pulse current flows in the winding, so the winding loss is not a big concern for this transformer.

$R_m$  reflects the transformer core loss. Based on the operation principle, the volt-second is applied to the transformer only within a very short pulse duration. Right after the pulse duration, the reverse volt-second is applied to demagnetize the transformer. Therefore, flux swing in the core is small. As long as the high-frequency ferrite core material and sufficient core cross-section area are employed, the core loss should not be a problem, either.

#### b. Magnetizing inductance.

$L_m$  represents the magnetizing inductance of the transformer. According to CS-GD operation principle, the magnetizing current will reduce the amplitude of the pulse current. Therefore, the magnetizing inductance should be designed as large as possible. For the gapped-core transformer, the reluctance of the airgap is dominant in the loop. Hence, the airgap of the core should be minimized. Meanwhile, employing more turns will boost the magnetizing inductance as

well.

c. Leakage inductance.

$L_{lk1}$  and  $L_{lk2}$ ' represent the primary side leakage inductance and the secondary side leakage inductance referred to the primary side, respectively. Leakage inductance is a critical parameter to achieve synchronized gate driving for the series-connected SiC MOSFETs. It is because there will be voltage drop across the leakage inductance during the  $di/dt$  transient. Although the leakage inductance only influences the rising and falling edge of the pulse current, the difference in the leakage inductance may result in different gate-to-source voltage rise timing for the series-connected SiC MOSFETs. Therefore, for the three series-connected channels, the leakage inductance should be kept as similar as possible and as small as possible.

However, the insulation distance between the primary winding and the secondary winding has to be considered as well, especially for the medium voltage applications. It should be noted that by reducing the distance between the primary winding and secondary winding, the leakage inductance can be cut down. Because more flux will be collected by the secondary winding, and the magnetic coupling coefficient becomes higher. Therefore, there is a trade-off between the insulation distance and the leakage inductance value. Technically, the insulation distance between the primary winding and the secondary winding can be reserved as the minimum distance which satisfies the insulation requirement. However, in this way, the distances between the primary winding and three secondary windings for the three series-connected channels will be different, because the insulation voltage levels are different for the three channels. Therefore, it is preferred to reserve the same insulation distance between the

primary winding and three secondary windings. This distance should be at least equal to the minimum distance which satisfies the insulation voltage level of the top device (the whole dc-link voltage). It is reasonable to sacrifice a little bit of leakage inductance value to obtain the parameter consistency of different channels.

d. Intra-winding capacitance.

$C_{\text{intra}1}$  and  $C_{\text{intra}2}$ ' represent the intra-winding capacitance of the primary winding and the intra-winding capacitance of the secondary winding referred to the primary side. The intra-winding capacitance should be minimized, because it is paralleled with the input capacitance of the device, hence, part of the pulse current will be drawn. Meanwhile, oscillations may occur due to the resonance between the intra-winding capacitance and the transformer leakage inductance, which will degrade the circuit performance. The simple and effective ways to cut down the intra-winding capacitance include reducing the overlapping area between the adjacent turns of each winding and increasing the distance between the adjacent turns of each winding. Meanwhile, single layer winding structure should be employed to avoid the layer-to-layer intra-winding capacitance. There are other approaches which manipulate the electric field density within each winding [164, 165].

e. Inter-winding capacitance.

$C_{\text{inter}}$  represents the total inter-winding capacitance between the primary winding and the secondary winding. This parameter reflects the  $dv/dt$  immunity of the gate driver. Therefore, it should be minimized as well. The inter-winding capacitance can be effectively reduced by increasing the distance between the primary winding and the secondary winding. However, the leakage inductance

will be increased. As mentioned in the discussion of leakage inductance part, the consistency of the leakage inductance is more important than the magnitude of the leakage inductance. The insulation distance for the three series-connected channels should be kept the same, and this distance can be further increased if the inter-winding capacitance needs to be cut down.

## 2.2 Design and Optimization of the Transformer in the Proposed CS-GD.

The multi-winding transformer design is based on the multi-objective optimization process elaborated in [51, 166, 167].

### 3. Secondary Self-driving Circuit Design Guideline.

The self-driving circuit has positive current and negative current networks. Each network has two branches: auxiliary gate driving branch and pulse current conduction branch. Since the positive current network and the negative current network are symmetrical, the following design guideline will use positive current network as an example.

#### 3.1 Gate Driving Auxiliary Branch Design.

The gate driving auxiliary circuit for positive current pulse is  $R_1 - R_5 - D_1 - SW_3 - R_2$ , as shown in blue color in Fig. 4.4(a).

##### a) Current limit unit $SW_3 - R_2$ design

The depletion MOSFET  $SW_3$  and  $R_2$  are used to form a current limit unit. The current limit value can be tuned by  $R_2$  per 4.12 [132, 162].

$$I_D = I_{DSS} \times \left(1 - \frac{I_D \cdot R_2}{V_{gs,th}}\right)^2 \quad (4.12)$$

where  $I_{DSS}$  is the on-state drain source current at  $V_{gs}$  equal to 0V;  $V_{gs,th}$  is the threshold voltage of the depletion MOSFET.

In order to make most of the pulse current flow into the gate of the SiC MOSFET, the current limit value  $I_D$  is set to be 200 mA.

b)  $R_1$  and  $D_1$  design

Per the current limit value, the gate resistor  $R_1$  can be designed to avoid  $SW_1$  gate overvoltage. The gate resistor  $R_1$  can be  $30 \Omega$ . Thus, the on-state gate voltage of  $SW_1$  is -6 V which guarantees a safe turn-on of  $SW_1$ . The diode  $D_1$  is to prevent negative pulse current from flowing into the gate driving circuit.

c)  $R_5$  design

The  $R_5$  in the positive auxiliary gate driving branch and  $R_6$  in the negative auxiliary gate driving branch are for the damping of transformer magnetizing current after the current pulse disappears. Suppose the Zener diode will remain in breakdown region for  $T_b$  time after the current pulse. From Fig. 4.3, the positive pulse volt-second  $VT$  applied to the transformer magnetizing inductor  $L_m$  can be derived and the magnetizing current  $I_{m1}$ ,  $I_{m2}$  can be calculated:

$$VT = \frac{V_{gs+} + V_{gs-}}{2} \times T_1 + V_{gs+} \times T_Z + I_P R_g \times (T_1 + T_Z) \quad (4.13)$$

$$I_{m1} = I_{m2} = \frac{VT}{L_m} \quad (4.14)$$

The time  $T_{damp}$  for the magnetizing current decaying to zero should be less than  $T_b$ :

$$\frac{L_m I_{m1}}{V_m} = T_{damp} < I_b \quad (4.15)$$

Per 4.15, winding voltage  $V_m$  can be determined and the resistor  $R_6$  can be calculated by 4.16:

$$V_m \approx I_1 \times R_6 \quad (4.16)$$

where  $I_1$  is the current flowing through the auxiliary gate branch. It should be noted that after the implementation of  $R_6$ , the  $C_{gs}$  of the SiC MOSFET basically will not be discharged. Therefore, the magnetizing current flowing through  $SW_2-D_4$  is negligible, and  $I_1$  is approximately equal to  $I_{m2}$ .

### 3.2 Current Conduction Branch $SW_1-D_3$ Design.

The diode  $D_3$  guarantees that only the positive current can flow through this path. The  $SW_1-D_3$  forms a voltage bidirectional and current unidirectional switch unit. This switch can conduct positive current when  $SW_1$  turns on and block the discharging path when  $SW_1$  turns off. Because the on-state gate voltage is negative (voltage across  $R_1$ ),  $SW_1$  should be a P-channel MOSFET. For the diode  $D_3$ , Schottky diode is selected because of its fast reverse recovery characteristics. The pulse current rating of  $SW_1$  and  $D_3$  should be bigger than the gate current amplitude. The voltage rating of  $SW_1$  and  $D_3$  should be bigger than maximum  $V_{gs}$  of the SiC MOSFET, because in the discharging path block state, as shown in Fig. 4.4(b)(d), the  $V_{gs}$  of SiC MOSFET is applied directly to  $SW_1-D_3$ . The design considerations for components in the negative current branch are the same as those in the positive current branch. The only difference is the on-state gate voltage of  $SW_2$  is positive, so  $SW_2$  is a N-channel MOSFET.

## 4. Snubber Circuit Design Guideline.

The function of the snubber circuit is to compensate the device  $V_{ds}$  difference in the series string. This voltage difference is caused by three factors:

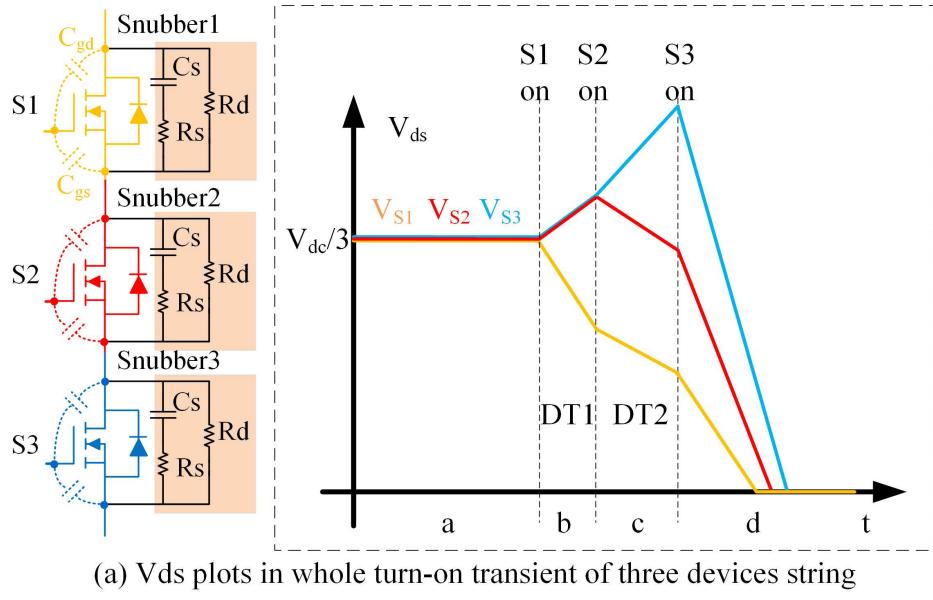
- a. Gate driving signals difference.
- b. Power loop difference, including parasitic capacitance and inductance in the power loop.

- c. Device part-to-part parameter spread caused by fabrication process [74, 77], such as parasitic capacitance ( $C_{iss}$ ,  $C_{oss}$  and  $C_{rss}$ ), anti-parallel diode parameters and gate threshold voltage.

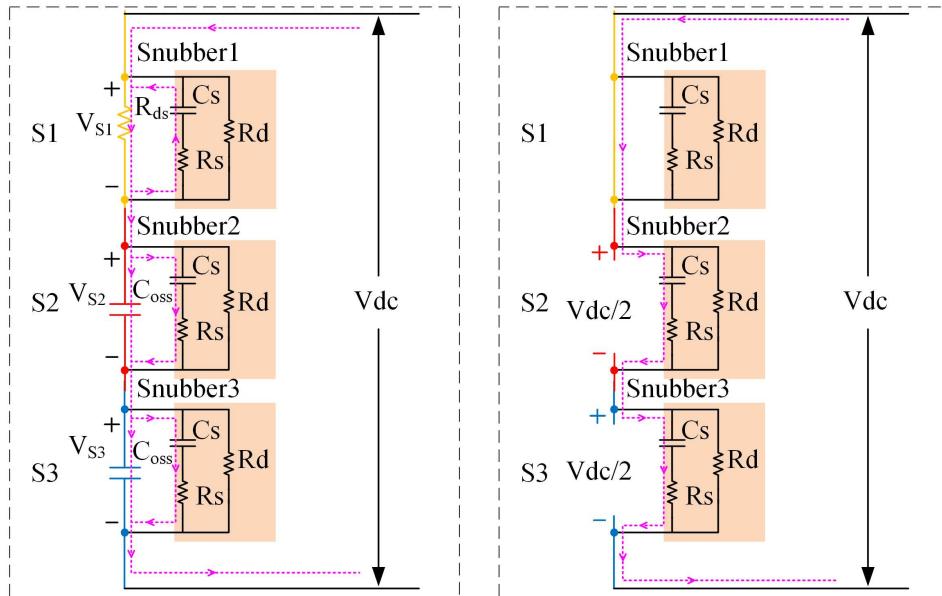
The proposed CS-GD can guarantee highly-synchronized gate driving signals, but the power loop difference and device part-to-part difference are inevitable. Thus, the snubber is still necessary. By implementing the highly synchronized  $V_{gs}$ , the snubber can be designed only based on power loop difference and device tolerance. Therefore, the snubber loss and size can be reduced. The snubber circuit design constraints can be summarized below:

1. The device drain-source voltage does not exceed the defined maximum allowed drain-source voltage.
2. The snubber discharge time should be smaller than the minimum pulse width of the device which means the snubber can be fully discharged when the switch is on.
3. The snubber loss should be minimized which means the capacitor should be minimized [168].
4. The sum of RC discharge current and load current should not exceed the device maximum pulse current rating.

Based on the above four constraints, the snubber circuit parameters can be determined. On top of the design, the snubber parallel resistor  $R_d$  is used to equalize the steady state  $V_{ds}$ . Hence,  $R_d$  can be relatively big to minimize the steady state snubber loss. An example calculation of  $R_s$  and  $C_s$  is shown in the following paragraphs. Afterwards, the design guideline for expanding the series string to more levels will be provided.



(a)  $V_{ds}$  plots in whole turn-on transient of three devices string



(b) Actual charging path

(c) Simplified charging path  
in worst-case

**Figure 4.7:** Turn-on Process of Three Series-connected Devices String.

To support for the example calculation, three series-connected SiC MOSFETs will be used as base. Suppose S1 turns on first. Then, S2 turns on after  $dT_1$  time, and after  $dT_2$  time, S3 turns on. The following calculations are based on two assumptions:

1. The device equivalent  $R_{dson}$  at switching transient is much larger than  $R_s$ , thus the voltage of the capacitor  $C_s$  can represent device  $V_{ds}$ .
2. The snubber is designed in worst-case where the final steady state voltage source is used to charge the RC snubber ( $V_{dclink}/2$  charges S2,S3 snubbers when S1 turns on,  $V_{dclink}$  charges S3 snubber when S2 turns on) and the device output capacitance  $C_{oss}$  is zero.

The turn-on process is divided into four parts (a, b, c, and d) in Fig. 4.7(a):

- a. S1, S2 and S3 are off. The steady off-state  $V_{ds}$  is equally shared because of parallel resistor  $R_d$ .

$$V_0 = V_{ds,S1,0} = V_{ds,S2,0} = V_{ds,S3,0} = V_{dc}/3 \quad (4.17)$$

where  $V_{ds,S1,0}$ ,  $V_{ds,S2,0}$  and  $V_{ds,S3,0}$  are the steady state drain-source voltage of S1, S2 and S3.

- b. S1 turns on, S2 and S3 are off.

At this state, the actual process is that dc-link voltage charges S2 and S3 through S1 network which is shown in Fig. 4.7(b). During switching transient, the  $R_{dson}$  of S1 is changing and is much bigger than  $R_s$ . The actual charging voltage of S2 and S3 is smaller than  $V_{dclink}$  because there is still voltage drop  $V_{S1}$  on S1, as shown in Fig. 4.7(b). And this charging voltage is applied to the parallel network of  $C_{oss}$  and the snubber circuit simultaneously.

Based on the worst-case assumption, it is supposed that the whole dc-link voltage is applied to the S2-S3 network, and the  $C_{oss}$  of S2 and S3 are zero, as shown in Fig. 4.7(c). Because this will lead to fastest charging process and largest  $V_{ds}$  difference. At the end of this state,  $V_{ds}$  of S2 and S3 is:

$$V_1 = V_{ds,S2,1} = V_{ds,S3,1} = \frac{V_{dc}}{3} + \left( \frac{V_{dc}}{2} - \frac{V_{ds}}{3} \right) \times \left( 1 - e^{-\frac{dT_1}{R_s C_s}} \right) \quad (4.18)$$

where  $V_{ds,S2,1}$  and  $V_{ds,S3,1}$  are the drain-source voltages of S2 and S3 after S1 turns on.

c. S1 and S2 turn on, S3 is off.

During DT2 time, the dc-link voltage will charge S3. At the end of state c, the  $V_{ds}$  of S3 is:

$$V_2 = V_{ds,S3,2} = V_1 + (V_{dc} - V_1) \times \left( 1 - e^{-\frac{dT_2}{R_s C_s}} \right) \quad (4.19)$$

where  $V_{ds,S3,2}$  is the drain-source voltage of S3 after S1 and S2 turn on. The largest  $V_{ds}$  happens before the last device turns on. So, the constraint 1 can be expressed as 4.20.

$$V_2 < V_{ds,max} \quad (4.20)$$

where  $V_{ds,max}$  is the maximum allowable device drain-source voltage, which is usually 50%-60% of the device voltage rating for the reliability requirement [79]. In this example, If the delay time  $dT_1$  and  $dT_2$  are both 5 ns, and the maximum allowable  $V_{ds}$  difference is 20% of the average value, the  $R_s C_s$  time constant can be calculated as 4.21 per 4.184.194.20.

$$R_s C_s > 60ns \quad (4.21)$$

Constraint 4 can be expressed using 4.22.

$$I_{load} + \frac{V_{ds,max}}{R_s} < I_{pulse,rating} \quad (4.22)$$

Where  $I_{\text{pulse, rating}}$  is the pulse current rating of SiC MOSFET;  $I_{\text{load}}$  is the maximum load current. For a 2 kV system, the 20% maximum allowable voltage difference leads to 800 V  $V_{\text{ds,max}}$  per 4.23.

$$V_{\text{ds,max}} = \frac{V_{\text{dclink}}}{3} \times (1 + 20\%) \quad (4.23)$$

If the 1.2 kV/60 A SiC MOSFET C2M0040120D [150] is used, its pulse current rating is 160 A, and the maximum load current is supposed to be 60 A. Per 4.22 and 4.23, the  $R_s$  can be limited by 4.24.

$$R_s > 8\Omega \quad (4.24)$$

The  $RC$  snubber circuit makes device equivalent  $C_{\text{oss}}$  bigger, thereby slowing the change of  $V_{\text{ds}}$ . The performance of the snubber circuit is more effective with smaller  $R_s$  and bigger  $C_s$ . But the capacitor  $C_s$  which is related to the stored energy determines the snubber loss and size [79, 168]. It is because when the device turns on, the capacitor stored energy will be dissipated. Thus, in this case, 10  $\Omega$  is a suitable trade-off value of  $R_s$ . The corresponding  $C_s$  is 6 nF.

Expanding to the general case with number of N devices in a series string, the  $V_{\text{ds}}$  delay times ( $dT_1, dT_2$  to  $dT_N$ ) and the maximum allowable device voltage  $V_{\text{ds,max}}$  should be determined on top of the design. The  $dT_1, dT_2$  to  $dT_N$  without snubber circuit can be measured by experiments and the  $V_{\text{ds,max}}$  can be determined by 4.25.

$$V_{\text{ds,max}} = \frac{V_{\text{dclink}}}{N} \times (1 + k) \quad (4.25)$$

where N is the number of devices in a series string;  $V_{\text{dclink}}$  is the system dc-link voltage;  $k$  is the allowable voltage difference ratio referred to average off-state

voltage on each device. Through the procedure below, the snubber parameters can be calculated.

1. The  $V_{ds}$  of the last turn-on device can be calculated step by step like the procedure a-b-c in the example.
2. Based on 4.20,  $R_s C_s$  time constant can be calculated.
3. Per the pulse current limit constraint 4.22,  $R_s$  minimum value is determined.
4. According to trade-off between the snubber performance and the snubber loss,  $R_s$  is selected with some margin and the corresponding  $C_s$  can be calculated by 4.20.

The designed snubber can be evaluated in three aspects:  $V_{ds}$  voltage sharing, loss and size. Using the proposed design guideline, the actual  $V_{ds}$  difference is supposed to be smaller than pre-set  $V_{ds,max}$  because the estimated worst-case in the calculation will not be fulfilled in the real application. In terms of loss and size, the  $R_s C_s$  snubber loss is as 4.26 [79, 150]:

$$P_{\text{sub,loss}} = C_s \times \left(\frac{V_{\text{dclink}}}{N}\right)^2 \times f_{zw} \quad (4.26)$$

The snubber size is proportional to the snubber loss. Because the snubber loss is dissipated through  $R_s$  [79], the power rating of  $R_s$  should be larger than the snubber loss  $P_{\text{sub,loss}}$ .

## D. LTSPICE Simulation Results

The LTSPICE simulation of the double pulse tester [32] is conducted with the block of three series-connected SiC MOSFETs. The performance of VS-GD and CS-GD

are compared, and the operation principle of the CS-GD is verified. This section will take turn-on process as an example to explain the simulation results.

**Table 4.1:** Components Used in Simulation and Experiment.

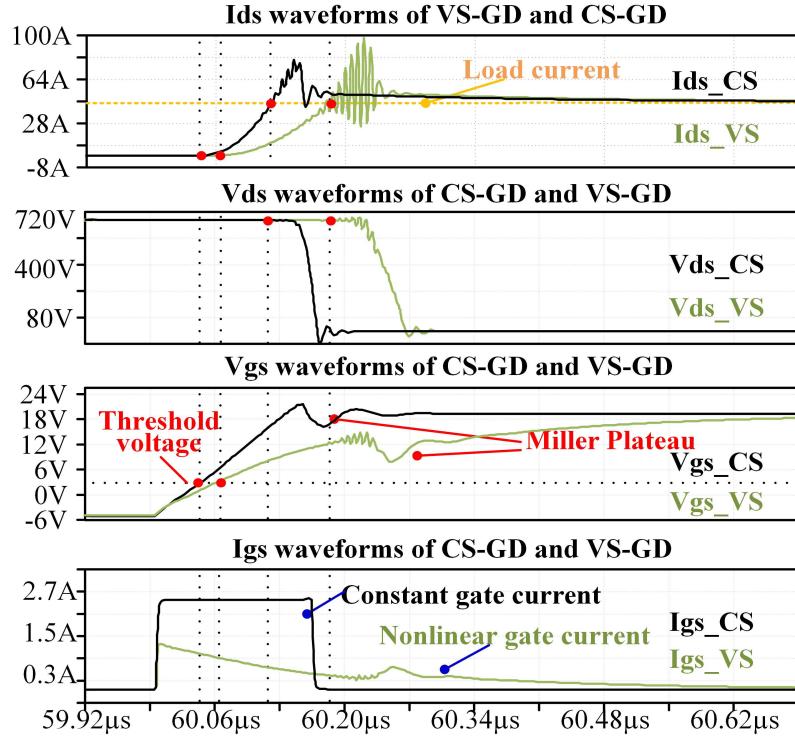
Components	Part Number
CSI MOSFET	IRFH5306
CSI diode	TSP10U45S
CSI gate driver	ADUM4120
Self-driving P-MOS $SW_1$	RQ5H020SP
Self-driving N-MOS $SW_2$	RSR030N06TL
Depletion MOSFET $SW_3, SW_4$	BSS159N
Schottky Diode $D_3, D_4$	RB168VYM-60
Zener diode zd1	UDZV10B
Zener diode zd2	KDZV4_7B
Diode $D_1, D_2$	DAN222WM
$R_1, R_3$	$30\ \Omega$
$R_2, R_4$	$1.3\ \Omega$
$R_5, R_6$	$200\ \Omega$

The components' SPICE models used in the simulation are listed in Table 4.1. These are also the actual components used in the prototype.

## 1. CS-GD and VS-GD Comparison

### 1) $V_{gs}$ Linearity

Fig. 4.8 shows the CS-GD and VS-GD comparison of gate voltage and current in turn-on transient. The gate resistor, external  $C_{gs}$  and gate loop parasitic inductance are the same for both CS-GD and VS-GD. The gate driving voltage is +20 V/-5 V. Because the gate current of CS-GD driven device is bigger than

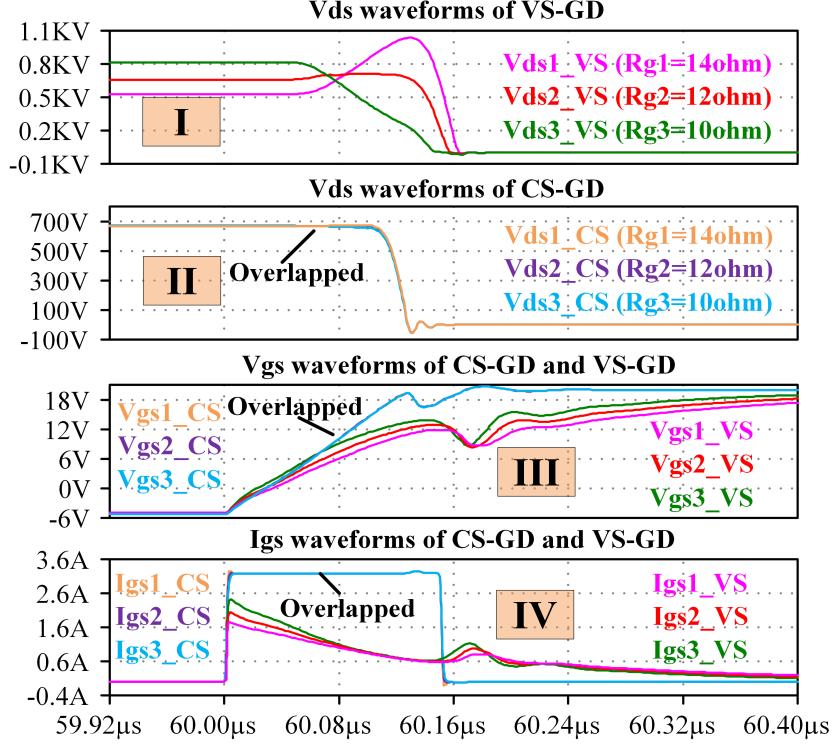


**Figure 4.8:** Turn-on Process of CS-GD and VS-GD With Same Gate Loop Parameters.

that of VS-GD driven device, the  $I_{ds}$   $di/dt$  and  $V_{ds}$   $dv/dt$  of the device driven by CS-GD is higher than the VS-GD counterpart. The  $V_{gs}$  of CS-GD ( $V_{gs,CS}$  in Fig. 4.8) shows a linear rising edge because of the constant gate current ( $I_{gs,CS}$  in Fig. 4.8). The miller plateau voltage is close to the  $V_{gs}$  steady state voltage. Because gate current of CS-GD is large, the miller current can be compensated by the gate current. In contrast, the  $V_{gs}$  of VS-GD ( $V_{gs,VS}$  in Fig. 4.8) shows a nonlinear rising slope with relatively low gate current ( $I_{gs,VS}$  in Fig. 4.8). This gate current cannot compensate the miller current, and  $V_{gs}$  is distorted before the device is fully turned on. The gate voltage of VS-GD presents a nonlinear and distorted waveform due to its nonlinear RC charging process and low gate current.

## 2) Sensitivity to Gate Loop Difference

### a. Gate Resistance Difference



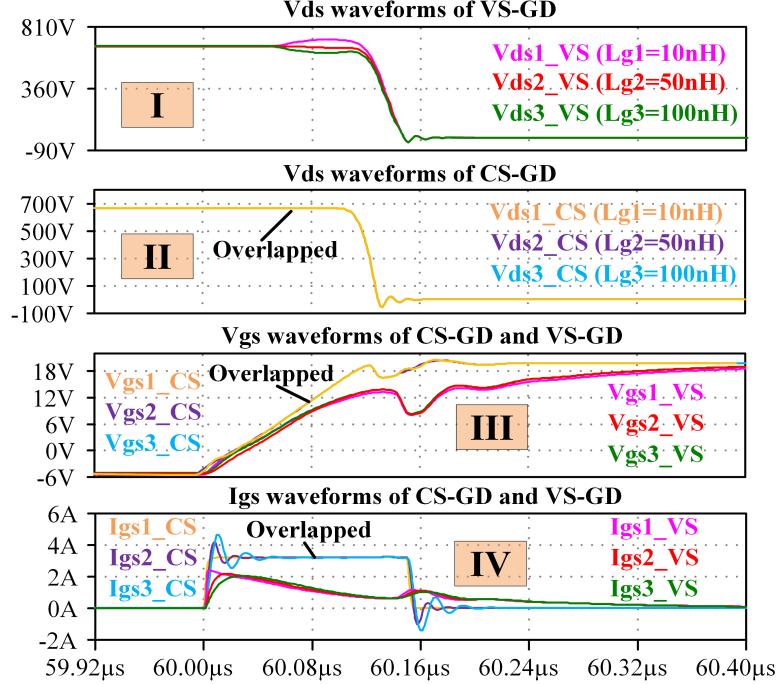
**Figure 4.9:** Turn-on Process of CS-GD and VS-GD With Different Gate Resistance.

Fig. 4.9 shows the turn-on process of CS-GD and VS-GD. Only the gate resistors of three channels are different, and the values are  $10/12/14\ \Omega$ , respectively. Each gate parasitic inductance is  $10\text{ nH}$ . The VS-GD and CS-GD have the same gate driver parameters.

For VS-GD, the 16% of the gate resistance difference results in 23%  $V_{ds}$  difference, and the  $V_{gs}$  has delay in the range of 20 ns. In contrast, the gate resistance variance does not have impact on the  $V_{gs}$  of CS-GD which can be verified by the overlapped  $V_{gs}$  in plot plane III of Fig. 4.9. Therefore, the  $V_{ds}$  of CS-GD are equally shared.

## b. Gate Parasitic Inductance Difference

Fig. 4.10 shows the turn-on process with different gate parasitic inductances. The values of inductance are 10/50/100 nH, respectively. Each gate resistance is  $12\ \Omega$ .



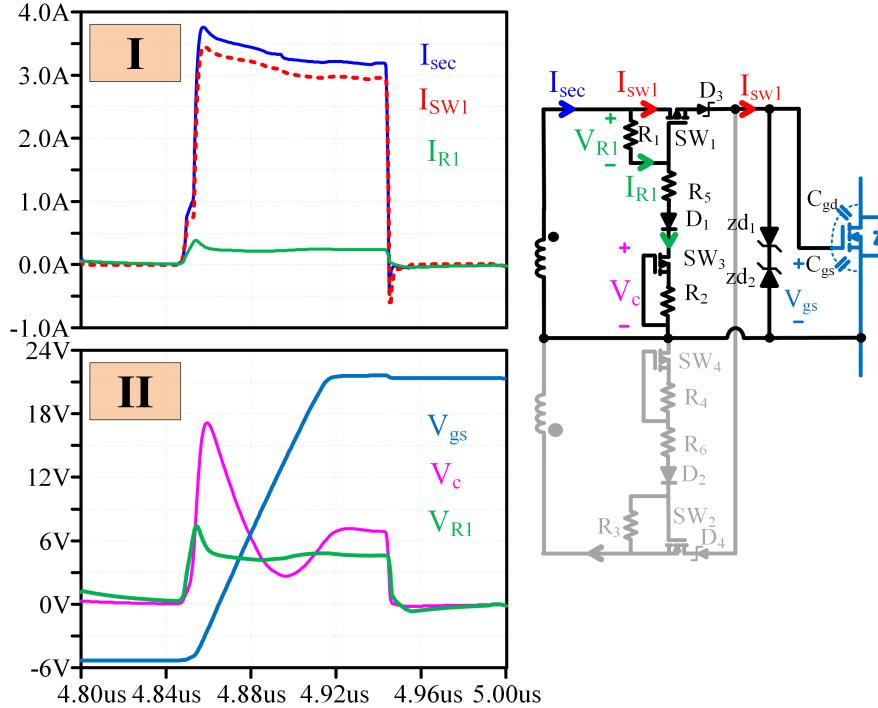
**Figure 4.10:** Turn-on Process of CS-GD and VS-GD With Different Gate Parasitic Inductance.

The inductor has impact on the current by delaying the current change. For VS-GD, the gate current ( $I_{gs1,2,3,vs}$  in plot plane IV) is always changing, and the inductor delays the gate current in the whole  $V_{gs}$  rising edge. Therefore, during the total turn-on transient, if the inductors of each channel are different, the  $V_{gs}$  ( $V_{gs1,2,3,vs}$  in plot plane III) rising edges will have different delays. For CS-GD, the gate current only changes at the rising/falling edges of the current pulse, and the gate current is constant during whole  $V_{gs}$  rising time. Hence, the path parasitic inductor only takes effect at the rising/falling edges which happens

within 10ns. Compared with the pulse time (150 ns), the rising/falling edge delay caused by the inductor almost does not affect the total gate current, as  $I_{gs1,2,3,CS}$  shown in plot plane IV. Due to the constant gate current, the difference of the parasitic inductance will not make the  $V_{gs}$  ( $V_{gs1,2,3,CS}$  in plot plane III) different. Thus, the  $V_{ds}$  of VS-GD shows 11% unequal share while the  $V_{ds}$  of CS-GD are equally shared. Because the parasitic inductance is in nH range, the influence of parasitic inductance difference is not as big as the gate resistor difference.

Based on the above analysis, the CS-GD is better than VS-GD in terms of  $V_{gs}$  synchronization under gate parameter variance.

## 2. CS-GD Operation Principle Validation



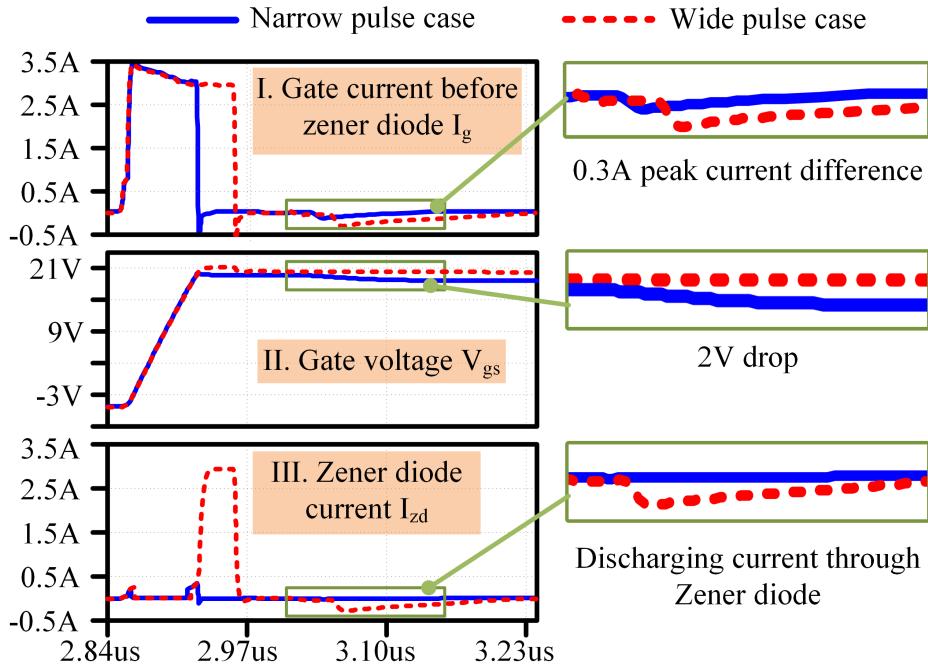
**Figure 4.11:** Current Distribution on Two Branches During Turn-on Process.

### 1) Self-driving Circuit

The process of positive current pulse is shown in Fig. 4.11. The positive current is transferred from CSI to the transformer secondary side, and the induced current will flow through the positive path of the secondary winding. This current is divided by two branches: the self-driving branch  $R_1 - R_5 - D_1 - SW_3 - R_2$  and SiC MOSFET gate path  $SW_1 - D_3$ . In Fig. 4.11, the self-driving branch current  $I_{r1}$  is 200 mA, and most of  $I_{sec}$  will flow through  $SW_1$  to the gate of SiC MOSFET, which is noted as  $I_{sw1}$  in the schematic. The 200 mA of  $I_{r1}$  is decided by the current limit unit  $SW_3 - R_2$ . Hence, the gate voltage of  $SW_1$  is safe (around 6 V in Fig. 4.11 II) and large enough to drive  $SW_1$ . Although the voltage across the current-limit unit ( $V_c$ ) is changing during the pulse period, the current  $I_{r1}$  is kept to a constant value 200 mA.

### 2) Zener Diode Transient

Two current pulses with different length are implemented to test the Zener diode transient effect. For the narrow current pulse, the pulse length is exactly equal to the  $V_{gs}$  rising time, which means the Zener diode will not go into the breakdown region. In this case, the Zener diode works like a capacitor in parallel with  $C_{gs}$ . The discharging magnetizing current will flow through both  $C_{gs}$  and Zener diode, making the  $V_{gs}$  drop, as shown in Fig. 4.12 II. For the wide current pulse, the current length is longer than  $V_{gs}$  rising time, the residue current makes the Zener diode in the breakdown region. In Fig. 4.12 III, the Zener diode is in breakdown region, providing a low resistance path to bypass the discharging current (red dash line). Therefore,  $V_{gs}$  maintains constant. But this Zener diode breakdown region will only maintain hundred nanosecond time after the pulse current, it is important to make the magnetizing current damp

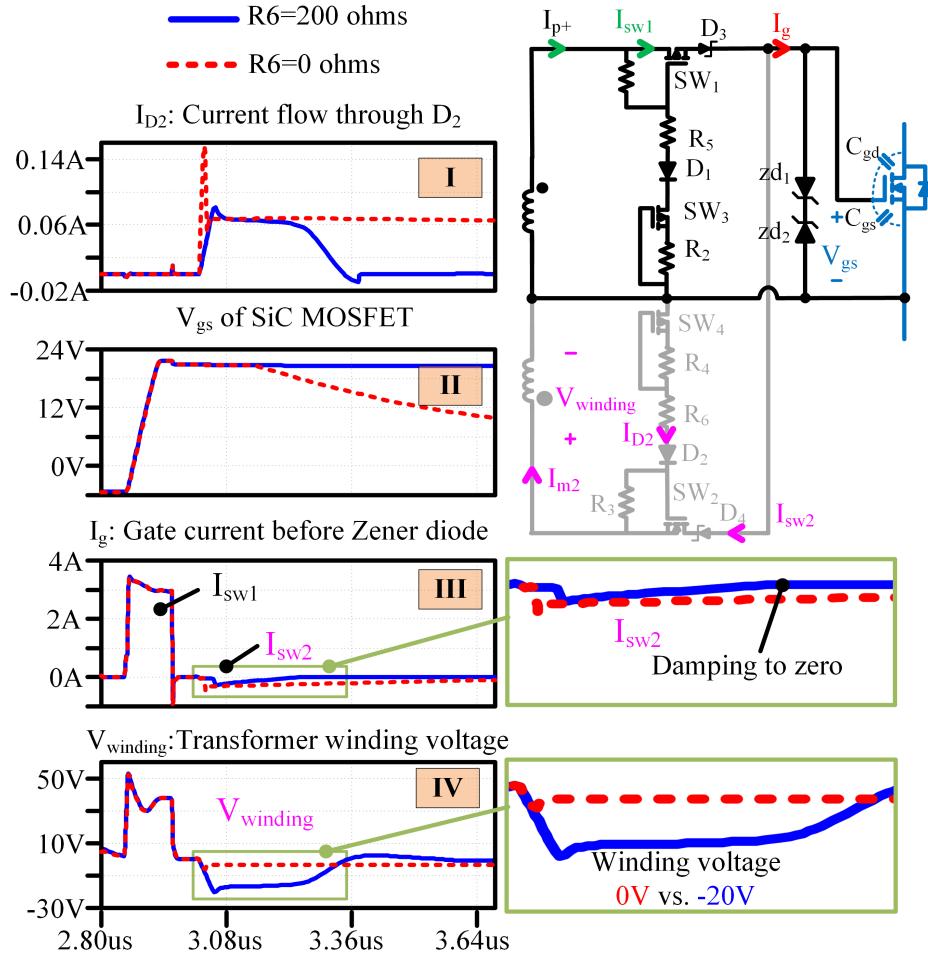


**Figure 4.12:** Zener Diode Transient Effect for Narrow Pulse and Wide Pulse Current Cases.

to zero within this time slot.

### 3) Magnetizing Current Damping (De-magnetization) Performance

The self-driving gate branch has damping function for the transformer magnetizing current because of additional resistors  $R_5$  and  $R_6$ . Taking the magnetizing current after positive pulse as an example, Fig. 4.13 shows the waveforms with and without  $R_6$ . The symbols are noted on the schematic. For the positive current operation, there are two phases, positive pulse current phase and magnetizing current damping phase. As shown in Fig. 4.13 III,  $I_g$  has two parts, positive pulse current  $I_{sw1}$  and magnetizing current  $I_{sw2}$ . Due to the current limit unit  $SW_4-R_4$ ,  $I_{D2}$  is limited to 70 mA (Fig. 4.13 I). Fig. 4.13 IV shows the transformer winding voltage in two cases. In the case where  $R_6$  equals to 200  $\Omega$ , the transformer winding voltage  $V_{winding}$  is -16 V due to the voltage



**Figure 4.13:** Transformer Magnetizing Current Damping Effect for Different  $R_6$ .

drop on  $R_6$ . In the case where  $R_6$  equals to  $0 \Omega$ , this voltage is slightly below 0 V. Thus, with this reverse winding voltage, the magnetizing current can be damped within 200ns (in Fig. 4.13 III). Without this reverse winding voltage, the magnetizing current decays slowly, and it will discharge  $V_{gs}$  after the Zener diode quits breakdown region, as shown in Fig. 4.13 II.

## E. Loss Analysis and Drain-Source Voltage Balancing Analysis of CS-GD

Part One: Loss Analysis

The loss analysis includes two parts: CS-GD gate driver loss and series-connected devices switching loss.

### A. Driving Loss Discussion

The CS-GD driving loss is mainly contributed by the CSI stage because there is continuous current during CSI zero state. Since the transformer is in pulse operation, its loss is neglected. The detailed calculation is as follows.

#### 1. CSI Loss

The CSI loss is composed of driving loss, conduction loss and switching loss of four Si MOSFETs. The CSI driving loss is small and can be neglected. The CSI loss is shared by all series-connected channels. In the calculation, the MOSFET is Infineon's IRFH5306, and the Schottky diode is TSPB10U45S from Taiwan Semiconductor.

##### 1a. CSI Conduction Loss

CSI conduction loss includes MOSFET conduction loss and Schottky diode conduction loss. The conduction loss can be calculated per 4.27, which is 4.1 W.

$$P_{\text{on}} = 2 \times I_{\text{dc}} \times (I_{\text{dc}} R_{\text{dson}} + V_F) \quad (4.27)$$

where  $I_{\text{dc}}$  is the dc-link current of CSI,  $R_{\text{dson}}$  is the on-state resistance of IRFH5306,  $V_F$  is the forward voltage of Schottky diode TSPB10U45S.

##### 1b. CSI Switching Loss

Fig. 4.3 shows the CSI complete phases and its corresponding output voltage and current. There are basically four phases: two current output phases and two zero state phases. Taking transition from phase IV to phase I as an example.

At phase IV, S3 and S4 are on, S1 and S2 are off. The switch S1 turns on first, entering the deadtime IV-I. In this deadtime, CSI output current is still zero, because both S3 and S4 are on to bypass the dc-link current. Thus, S1 is zero current turn-on (ZCS). After phase IV-I, S3 turns off, and CSI enters phase I. The current is hard commuted from S3 to S1, and CSI outputs positive current pulse. At this time (T1 in Fig. 4.3(c)), the voltage across S3 changes from zero to  $V_{in}$ , and the current through S3 is from  $I_p$  to zero. Therefore, the turn-off loss of S3 can be expressed as:

$$P_{\text{turn-off}}(S3) = \frac{1}{2} \times I_p \times V_{in}(T_1) \times T_{\text{off}} \times f_{\text{sw}} \quad (4.28)$$

where  $T_{\text{off}}$  is the turn-off transition time of S3,  $I_p$  is the dc-link current,  $V_{in}(T_1)$  is the input voltage of CSI at T1 time, which is  $(V_g + I_p + R_g)$  shown in Fig. 4.3(c). The calculation is based on the experimental results: Both turn-on and turn-off time are approximately 100ns; the equivalent reflected  $R_g$  of three gate loops is 0.67 Ω; the dc-link current  $I_p$  is 8.5A; the switching frequency is 200 kHz. The other switching loss of the switches can be calculated based on the calculation process of the above example. The total switching losses of CSI is 4.35 W.

## 2. Secondary Circuit Loss

Secondary circuit composes of auxiliary branch and gate current conduction branch. The current through auxiliary branch is small, and its loss is neglected. The gate current conduction path loss is 0.87 W per 4.29.

$$P_{\text{sec}} = \left(\frac{I_p}{3}\right)^2 \times R_{g,\text{equiv}} \times (T_{\text{pulse},\text{on}} + T_{\text{pulse},\text{off}}) \times f_{\text{sw}} \quad (4.29)$$

where  $P_{\text{sec}}$  is the secondary circuit loss of single channel,  $R_{g,\text{equiv}}$  is the equivalent resistance of single gate loop, which is 2 Ω,  $T_{\text{pulse},\text{on}}$  and  $T_{\text{pulse},\text{off}}$  are the positive

and negative current length, both of which are 300 ns. The total driving loss of CS-GD for each series-connected channel is 3.7 W, which is 6.45 times of VS-GD at the same condition [86]. However, the CS-GD loss can be reduced by implementing discontinuous operation mode [85]. In this way, nearly 37% of the driving loss is eliminated. Thus, the driving loss of CS-GD can be reduced to 4 times of VS-GD.

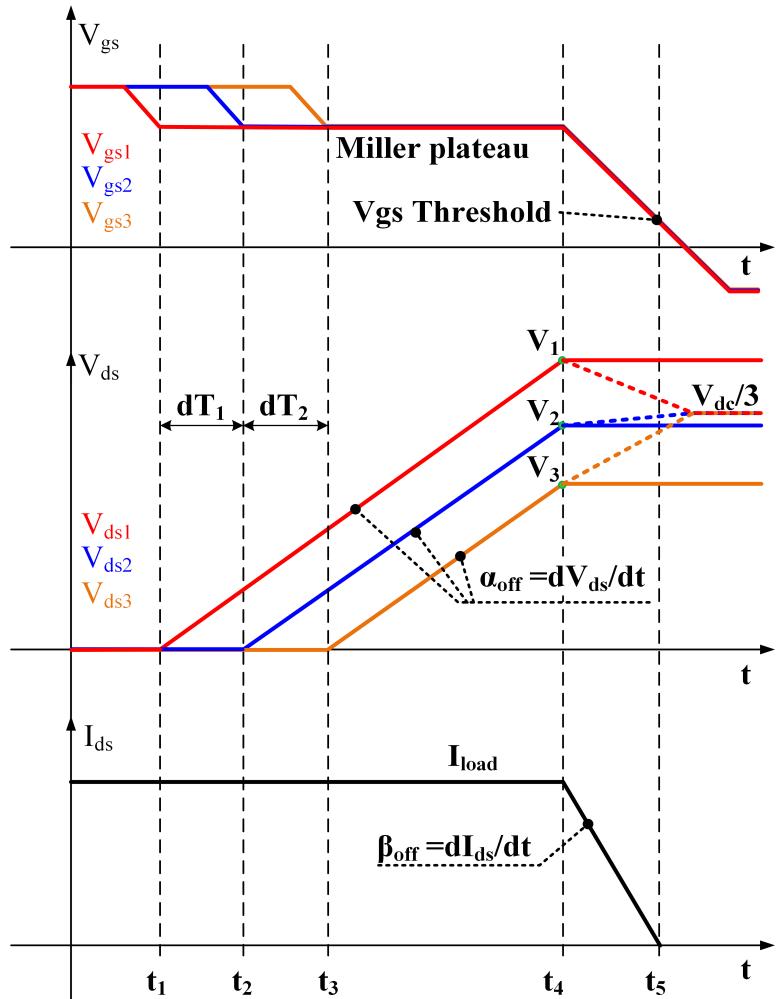
### B. Series-connected Devices Switching Loss Discussion

The proposed CS-GD has two main benefits over traditional VS-GD: 1. Higher switching speed [85]; 2. Better synchronization. The switching loss and reverse recovery loss of SiC MOSFET and its body diode can be compared between CS-GD and VS-GD based on these two benefits. All the  $V_{ds} dv/dt$  and  $I_{ds} di/dt$  of the series-connected devices during the transition are supposed to be equal for simplicity and better explanation.

#### 1. Turn-off transient

Suppose the delay times among S1-S3 are  $dT_1$  and  $dT_2$ . As shown in Fig. 4.14, the  $I_{ds}$  maintains load current level until the sum of three  $V_{ds}$  reaches dc-link voltage (at  $t_4$ ). It is because the freewheeling diodes of upper switches are reverse-biased and cannot conduct current. The turn-off loss can be calculated by integration of  $V_{ds}$  and  $I_{ds}$  during the transition time:

$$\begin{aligned}
 W_{\text{Loss,off}} &= W_{S1,\text{off}} + W_{S2,\text{off}} + W_{S3,\text{off}} \\
 \Rightarrow & \int_{t_1}^{t_5} I_{ds}(t) \times (V_{ds1}(t) + V_{ds2}(t) + V_{ds3}(t)) \cdot dt \\
 \Rightarrow & \int_{t_1}^{t_4} I_{load}(t) \times (V_{ds1}(t) + V_{ds2}(t) + V_{ds3}(t)) \cdot dt \\
 &+ \int_{t_4}^{t_5} I_{ds}(t) \times V_{dc} \cdot dt
 \end{aligned} \tag{4.30}$$



**Figure 4.14:** Typical Turn-off Waveforms of Three Series-connected SiC MOSFETs.

Based on the diagram, the following equations can be derived.

$$\left\{ \begin{array}{l} V_2 = V_1 - \alpha_{off} dT_1 \\ V_3 = V_1 - \alpha_{off} (dT_1 + dT_2) \\ V_1 + V_2 + V_3 = V_{dc} \\ t_5 - t_4 = I_{load} / \beta_{off} \end{array} \right. \quad (4.31)$$

where  $V_1, V_2, V_3$  are the  $V_{ds}$  voltages of three devices at  $t_4$ ,  $\alpha_{off}$  is the  $V_{ds} dv/dt$ ,  $\beta_{off}$  is the  $I_{ds} di/dt$ . From 4.30 4.31, the turn-off loss can be expressed by  $V_{dc}$ ,

$I_{\text{load}}$ ,  $\alpha_{\text{off}}$ ,  $\beta_{\text{off}}$  and  $dT_1$ ,  $dT_2$ .

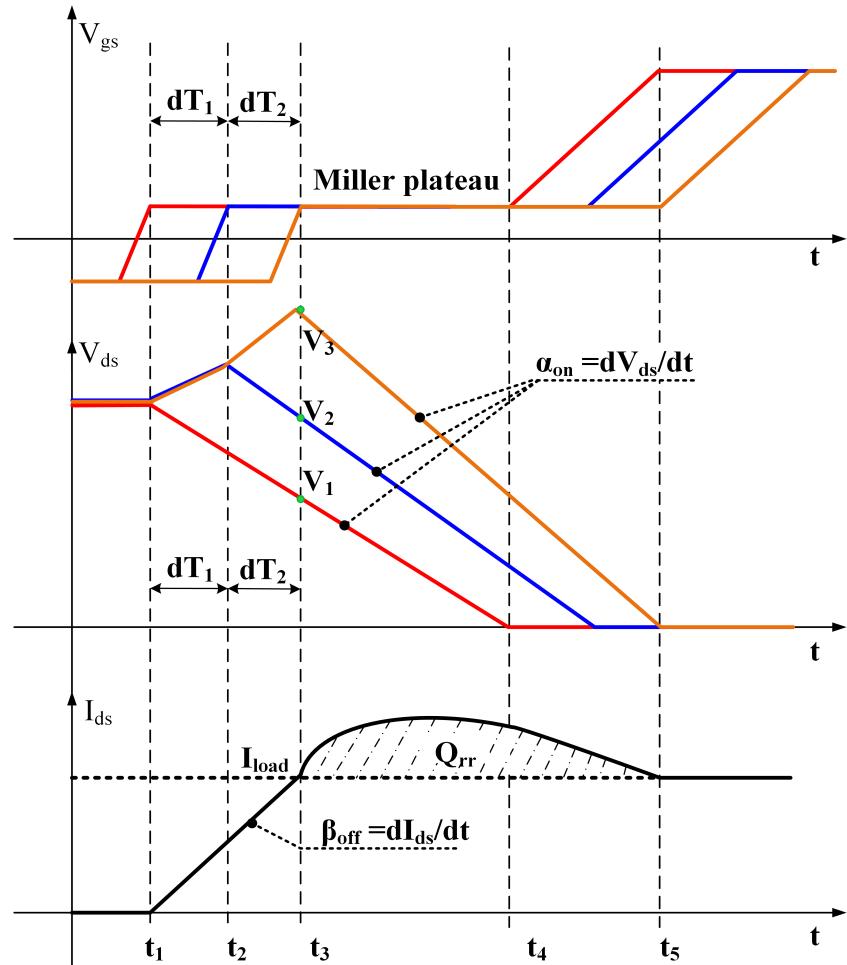
$$\begin{aligned}
 W_{\text{Loss,off}} &= \frac{1}{2} \left( \frac{V_1^2}{\alpha_{\text{off}}} + \frac{V_2^2}{\alpha_{\text{off}}} + \frac{V_3^2}{\alpha_{\text{off}}} \right) \times I_{\text{load}} + \frac{1}{2} V_{\text{dc}} \times \frac{I_{\text{load}}^2}{\beta_{\text{off}}} \\
 \Rightarrow & \frac{V_{\text{dc}}^2}{6\alpha_{\text{off}}} \times I_{\text{load}} + \frac{\alpha_{\text{off}}}{3} (dT_1^2 + dT_1 dT_2 + dT_2^2) \times I_{\text{load}} \\
 & + \frac{V_{\text{dc}}}{2} \times \frac{I_{\text{load}}^2}{\beta_{\text{off}}}
 \end{aligned} \tag{4.32}$$

There are three terms in 4.32, only the second term  $\alpha_{\text{off}}\alpha_{\text{off}}\alpha_{\text{off}}$  is related to the  $V_{\text{ds}}$  voltage synchronization level. The bigger the delay  $dT_1$  and  $dT_2$ , the bigger the loss will be. The other two terms are determined by the parameters  $\alpha_{\text{off}}$  and  $\beta_{\text{off}}$  representing the switching speed. The proposed CS-GD can achieve bigger  $\alpha_{\text{off}}$ ,  $\beta_{\text{off}}$  (higher switching speed) and smaller  $dT_1$ ,  $dT_2$  (better synchronization). Therefore, the total turn-off loss of CS-GD is smaller than VS-GD. It should be noted that the turn-off loss of three devices is not equal, first turn-off device has biggest loss per 4.33.

$$W_{S1,\text{off}} > W_{S2,\text{off}} > W_{S3,\text{off}} \tag{4.33}$$

where  $W_{S1,\text{off}}$ ,  $W_{S2,\text{off}}$ ,  $W_{S3,\text{off}}$  are turn-off loss of three devices.

2. Turn-on transient Suppose the delay time among series-connected devices is small, and the  $C_{\text{oss}}$  discharging current is still increasing before next switch turns on, thus,  $di/dt$  should be similar in each time interval, as shown in Fig. 4.15. Different from the single device turn-on transition, where  $V_{\text{ds}}$  and  $I_{\text{ds}}$  do not change at the same time because of the body diode clamping [32], the  $V_{\text{ds}}$  and  $I_{\text{ds}}$  of the device among series-connected string will change at the same time since only  $C_{\text{oss}}$  discharging process occurs before the last device turns on. Similarly, the turn-on loss can also be calculated by integration of  $V_{\text{ds}}$  and  $I_{\text{ds}}$



**Figure 4.15:** Typical Turn-on Waveforms of Three Series-connected SiC MOSFETs.

during the transition:

$$\begin{aligned}
 W_{\text{Loss},\text{on}} &= W_{S1,\text{on}} + W_{S2,\text{on}} + W_{S3,\text{on}} \\
 \Rightarrow &= \int_{t_1}^{t_5} I_{\text{ds}}(t) \times (V_{\text{ds}1}(t) + V_{\text{ds}2}(t) + V_{\text{ds}3}(t)) \cdot dt \\
 \Rightarrow &= \int_{t_1}^{t_4} I_{\text{ds}}(t) \times V_{\text{dc}} \cdot dt \\
 &+ \int_{t_4}^{t_5} I_{\text{load}}(t) \times (V_{\text{ds}1}(t) + V_{\text{ds}2}(t) + V_{\text{ds}3}(t)) \cdot dt \quad (4.34)
 \end{aligned}$$

Based on Fig. 4.15 and 4.34, the turn-on loss can be derived:

$$\begin{aligned}
W_{\text{Loss, on}} &= \frac{1}{2} \left( \frac{V_1^2}{\alpha_{on}} + \frac{V_2^2}{\alpha_{on}} + \frac{V_3^2}{\alpha_{on}} \right) \times (I_{\text{load}} + I_{\text{reverse}}) \\
&\quad + \frac{1}{2} V_{\text{dc}} \times \frac{I_{\text{load}}^2}{\beta_{on}} \\
\Rightarrow &= \frac{V_{\text{dc}}^2}{6\alpha_{on}} \times I_{\text{load}} + \frac{\alpha_{on}}{3} (dT_1^2 + dT_1 dT_2 + dT_2^2) \times I_{\text{load}} + \\
&\quad \frac{V_{\text{dc}}}{2} \times \frac{I_{\text{load}}^2}{\beta_{on}} + \frac{V_{\text{dc}}}{2} \times Q_{\text{rr}}
\end{aligned} \tag{4.35}$$

where  $V_1, V_2, V_3$  are the  $V_{\text{ds}}$  voltages of three devices at  $t_3$ ,  $\alpha_{on}$  is the  $V_{\text{ds}} dv/dt$ ,  $\beta_{on}$  is the  $I_{\text{ds}} di/dt$ ,  $Q_{\text{rr}}$  is the reverse recovery charge of the body diode.

It should be noted that the body diode reverse recovery current of the complementary switch will contribute to the turn-on loss, which is derived as 4th term of 4.35. Except for the reverse recovery induced loss, 4.35 has another three terms, in which only the second term is related to synchronization. It is obvious that, if the delay time  $dT_1$  and  $dT_2$  are small, this term will be small. The other two terms are related to the switching speed ( $\alpha_{on}$  and  $\beta_{on}$ ), if the switching speed is higher, the loss will be smaller.

### 3. Reverse Recovery Loss of Body Diodes

The utilization of body diodes typically introduces two major loss mechanisms: first, the actual reverse recovery losses in the intrinsic PN body diode, and second, the peak reverse recovery current reflects into the complementary switch and can induce additional turn-on losses [169]. The higher the switching speed, the higher the reverse recovery loss will be [169]. Since CS-GD can achieve higher switching speed, the reverse recovery loss driving by CS-GD should be bigger than that by VS-GD. As for a single device in the series string, the body diode reverse recovery loss of each device is not affected by the gate voltage synchronization level. It is because the body diode is uncontrollable by the

gate driver.

As for the reverse recovery induced additional turn-on loss of the complementary switches. The total additional turn-on loss is not affected by the voltage synchronization level, which can be seen from 4th term of 4.35. However, for a single device in the series string, the first turn-on device has the smallest additional turn-on loss.

From Fig. 4.15, first turn-on device has smallest Drain-Source current and voltage overlap area, which represents smallest turn-on loss. The comparison of turn-on loss is expressed in 4.36:

$$W_{S1,on} < W_{S2,on} < W_{S3,on} \quad (4.36)$$

where  $W_{S1,on}$ ,  $W_{S2,on}$ ,  $W_{S3,on}$  are turn-on loss of three devices. From 4.334.36, the unequal shared  $V_{ds}$  voltages will cause unequal switching loss among devices in the series string. However, the turn-off loss and turn-on loss has opposite trend. The earliest switched device has highest turn-off loss but smallest turn-on loss. Therefore, the switching loss difference may not be big, depending on which transition loss (turn-on or turn-off) is dominant. The additional loss induced by the  $V_{ds}$  difference is:

$$W_{add,loss} = \frac{\alpha_{on} + \alpha_{off}}{3} (dT_1^2 + dT_1dT_2 + dT_2^2) \times I_{load} \quad (4.37)$$

In summary, compared with traditional VS-GD, the driving loss of the proposed current source gate driver is big. But the current source gate driver can achieve higher switching speed because of the constant current at miller plateau voltage, this helps to reduce the device switching loss, which is much bigger than the driving loss. Thus, the overall loss using CS-GD can be smaller than that using

traditional VS-GD. Moreover, the proposed CS-GD loss is mainly contributed by CSI stage. The CSI loss can be reduced in a large scale by implementing discontinuous current mode.

### Part Two: $V_{ds}$ Balancing Analysis of CS-GD

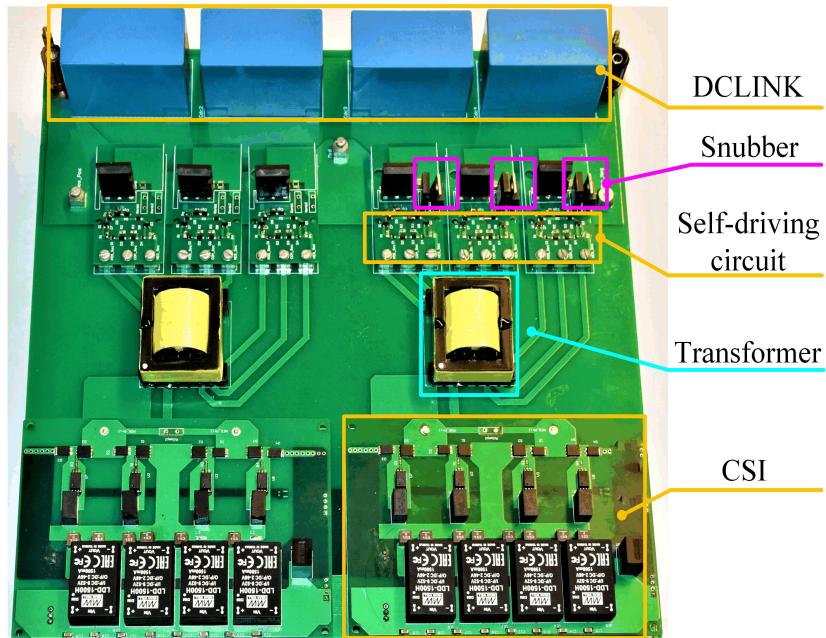
In general case of the series-connected SiC MOSFETs, the voltage unequal sharing is mainly because of unsynchronized gate voltages [70]. Taking turn-off as an example in Fig. 4.14, the following equations can be derived.

$$\begin{cases} V_1 - V_2 = \alpha_{off}dT_1 \\ V_2 - V_3 = \alpha_{off}dT_2 \\ V_1 + V_2 + V_3 = V_{dc} \end{cases} \Rightarrow \begin{cases} V_1 = \frac{1}{3}V_{dc} + \frac{\alpha_{off}}{3}(2dT_1 + dT_2) \\ V_2 = \frac{1}{3}V_{dc} + \frac{\alpha_{off}}{3}(-dT_1 + dT_2) \\ V_3 = \frac{1}{3}V_{dc} + \frac{\alpha_{off}}{3}(-dT_1 - 2dT_2) \end{cases} \quad (4.38)$$

It can be seen from 4.38 that under the same delay  $dT_1$  and  $dT_2$ , the difference of  $V_{ds}$  will increase with the increase of switching speed ( $\alpha_{off}$ ). Under the same switching speed ( $\alpha_{off}$ ), the difference of  $V_{ds}$  voltages will increase with the increase of delay time  $dT_1$  and  $dT_2$ . It should be noted that if the delay time  $dT_1$  and  $dT_2$  are small, the switching speed impact on the voltage balancing is negligible. It is because the delay time and switching speed are product relations. The main benefit of proposed CS-GD is to achieve tiny delay time. However, the  $V_{ds} dv/dt$  is supposed to be same for the above analysis. The voltage unbalance can also be caused by different  $V_{ds} dv/dt$ . The reasons causing different  $V_{ds} dv/dt$  are different junction temperature and parasitic capacitors induced common mode current, etc.. With the junction temperature increasing, the gate threshold voltage will decrease, which leads to more turn-off delay time [170, 171]. The data from literature [171] also shows that the higher junction temperature makes the turn-off  $V_{ds} dv/dt$  slightly lower. Paper [172] comprehensively investigated the parasitic capacitors' impact on the voltage balancing of series-connected SiC MOSFETs. The parasitic capacitors that are connected

to different terminals are gate-to-ground parasitic capacitors and drain/source parasitic capacitors [172]. These two kind of capacitors both affect the voltage sharing performance by influencing the gate current (gate-to-ground capacitors) and junction capacitor charging current (drain/source parasitic capacitors) at turn-off transition. In a word, both of these two factors influences voltage sharing performance by affecting  $V_{ds} dv/dt$  and delay time even when the gate driving signals are highly synchronized by the CS-GD. Therefore, closed-loop control methods or snubber circuits are necessary to compensate these factors.

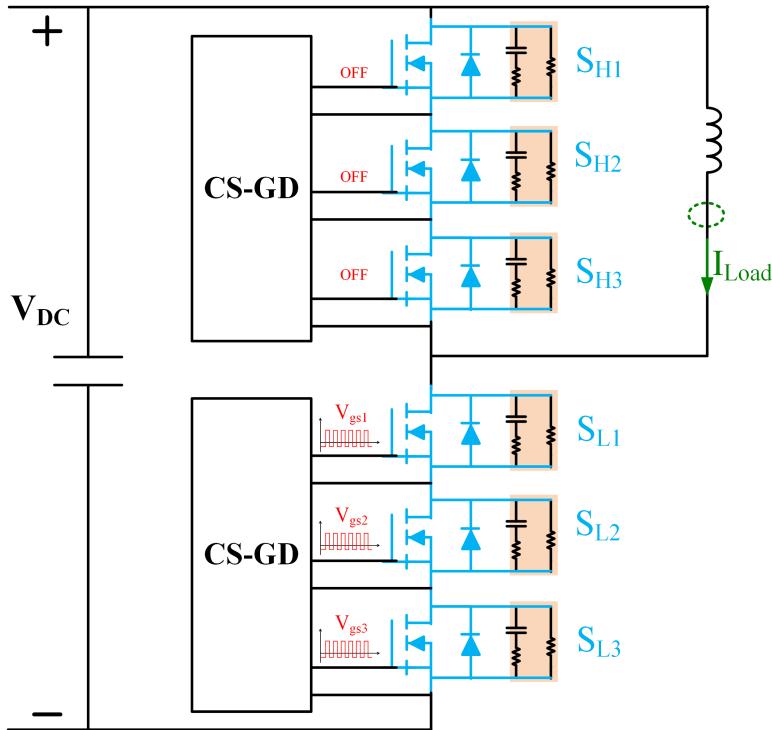
## F. Experimental Verification



**Figure 4.16:** Prototype of Series-connected SiC MOSFETs Half-bridge.

To validate the proposed CS-GD, a half-bridge prototype is designed using two blocks of series-connected SiC MOSFETs, as shown in Fig. 4.16. The multi-pulse test is conducted on this prototype. Fig. 4.17 shows the schematic of the test setup.

There are three 1.2 kV/60 A SiC MOSFETs in series in each block, and two blocks form a half-bridge. In the multi-pulse test, the low-side block is the ‘device’ under test (DUT), which will turn on and off multiple times. Each time DUT turns on, the load current will increase. Therefore, the performance of the proposed block can be evaluated at different current level. In this test, the number of pulses is set to make the load current change from 0 A to 60 A (the current rating of DUT). Thus, the full current range is covered. The test specifications are listed in Table 4.2.



**Figure 4.17:** Schematic of Multi-pulse Test.

### 1. CS-GD Experimental Validation

The CS-GD evaluation consists of operation principle verification,  $V_{gs}$  synchronization performance and de-magnetizing performance. The components used in this CS-GD are provided in Table 4.1. The multi-winding transformer is designed following the transformer design guideline in section III, and the key parameters are listed

**Table 4.2:** Multi-pulse Test Specifications.

Specifications	Values
Pulse switching frequency	200 kHz
Dc-link voltage	2 kV
Load current	0-60 A
SiC MOSFETs	C2M0040120D
Number of device in series	3
Block equivalent ratings	3.6 kV/60 A
Snubber parallel resistor $R_d$	100 $k\Omega$
Snubber parallel resistor $R_s$	10 $\Omega$
Snubber series capacitor $C_s$	2200 pF

in Table 4.3.

To verify the operation principle of CS-GD, Fig. 4.18 shows its typical signal waveforms. The input voltage  $V_{dc}$  (dark blue) is fixed at 9 V to make the inductor volt-sec balance. The CSI input current (light blue) is 8.9 A DC current. The amplitude of the output pulse current at transformer primary side is 8.9 A and the pulse length is 300 ns. The  $V_{gs}$  of the SiC MOSFET shows that there is not transient fluctuation at the start of the pulse operation. Therefore, the input voltage control strategy of the CSI is verified. The pulse operation frequency is 200 kHz which is high enough for the medium voltage hard-switching converter applications.

To evaluate the  $V_{gs}$  synchronization performance of the proposed CS-GD, the inductor and resistor with different values are inserted in the gate loop. Fig. 4.19 shows three channels'  $V_{gs}$  waveforms with different gate parasitic inductances. The intentionally inserted gate inductances are 5 nH/20 nH/50 nH by implementing different coils in the gate loop. For CS-GD, it can be seen that the gate voltages are high-

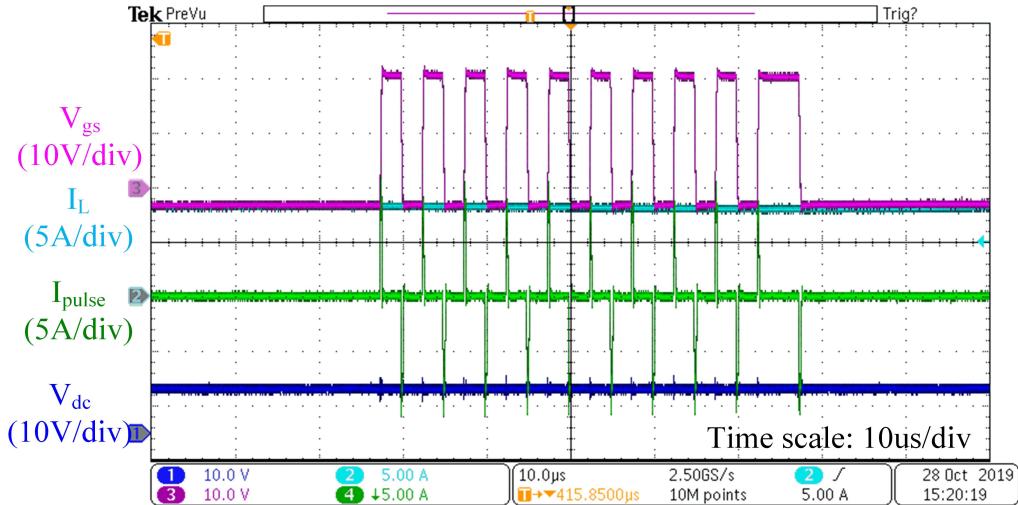
**Table 4.3:** Transformer Key Parameters in This Study.

Key parameters	Values
Maximum operating frequency	500 kHz
Insulation voltage level	5 kV
# of secondary windings N	3
# of turns	4(pri) 4(sec)
Core Material	Ferroxcube 3F36
Core dimension	E41/17/12
Core cross-section area	154.4 mm <sup>2</sup>
Maximum flux density <sup>1</sup>	8.3 mT
Primary leakage inductance $L_{lk1}$	128 nH
Secondary leakage inductance $L_{lk2}$	102/117/109 nH
Magnetizing inductance $L_m$	58 $\mu$ H
Total stray capacitance refer to primary side <sup>2</sup>	19.8 pF
Litz wire <sup>3</sup>	20 strands, 44 AWG

<sup>1</sup>The maximum flux density is small because the core dimension is selected based on the insulation distance.

<sup>2</sup>The parameter is measured using methods in [173].

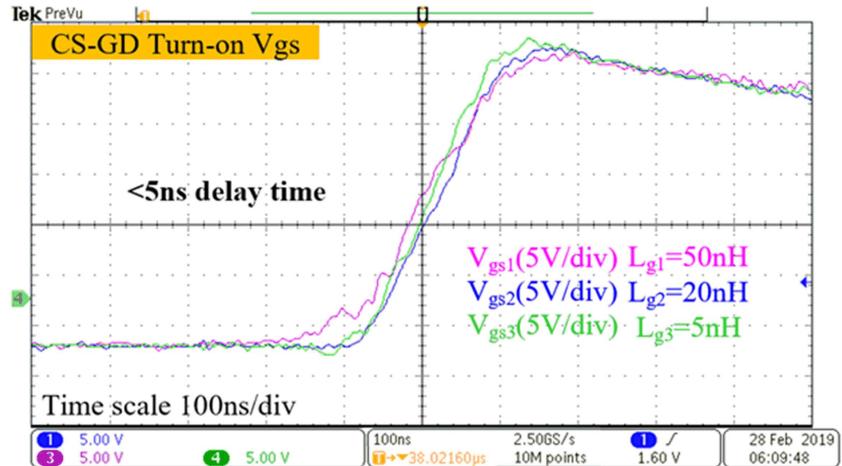
<sup>3</sup>The size of the single strand is 44AWG and the number of strands is 20. The equivalent nearest AWG of the Litz wire is 31.



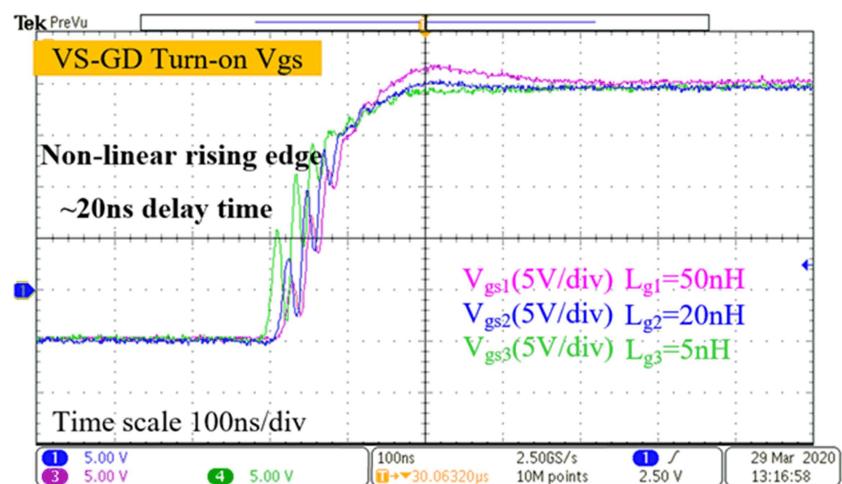
**Figure 4.18:** Typical Signals of CS-GD.

ly synchronized both at transient state (rising/falling edge) and steady state. The channel-to-channel delay time is within 5 ns. Compared with CS-GD,  $V_{gs}$  of the device driven by VS-GD has obvious high-frequency resonance, and the channel-to-channel delay time is 20 ns. This delay time is 4 times of the CS-GD counterpart. Fig. 4.20 shows the  $V_{gs}$  waveforms with different gate resistances. The intentionally inserted gate resistances are  $4 \Omega$ / $6 \Omega$ / $8 \Omega$ . For CS-GD, the rising edge is linear, and the channel-to-channel delay time of  $V_{gs}$  is within 5 ns. However, in the case of VS-GD, the  $V_{gs}$  rising edge is nonlinear, and the channel-to-channel delay time is 40 ns. The delay time of VS-GD is at least 7 times higher than that of CS-GD. Therefore, compared with VS-GD, the designed CS-GD is robust to gate loop parasitic inductance difference and gate loop resistance variance.

To verify the de-magnetizing performance of the secondary auxiliary circuit, the resistors  $R_5$  and  $R_6$  (noted in Fig. 4.5) for damping of the transformer magnetizing current are served as the experimental variables. Two control experiments are conducted. One experiment is done with  $0 \Omega$   $R_5$  and  $R_6$ . Another experiment is with

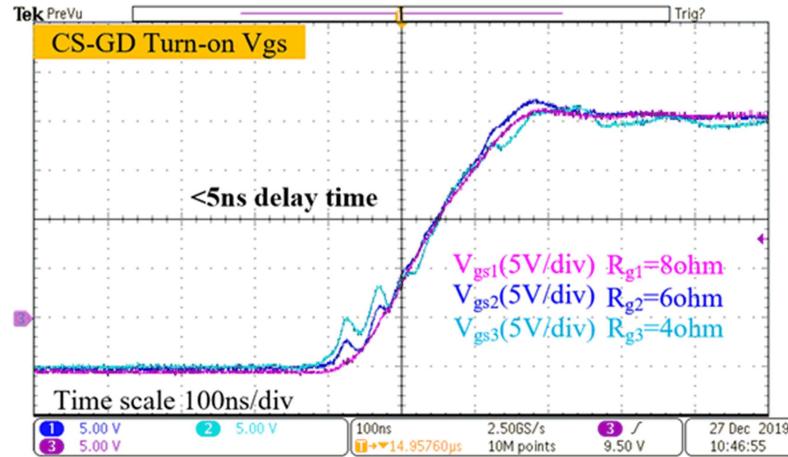


(a) CS-GD three channels'  $V_{gs}$  waveforms with different gate parasitic inductance

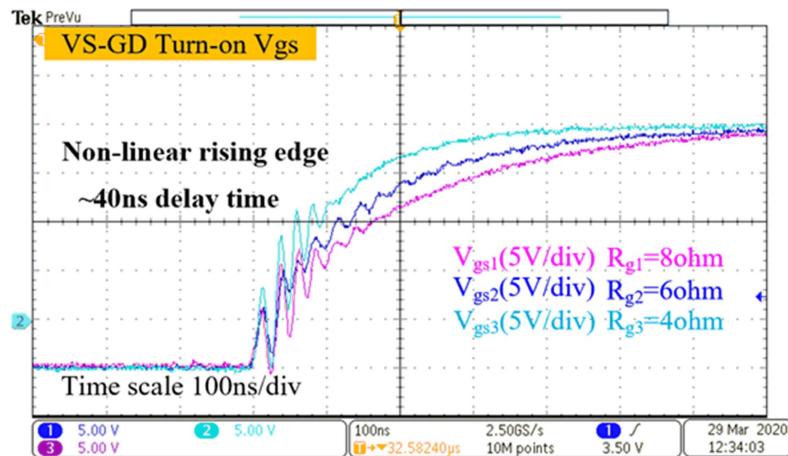


(b) VS-GD three channels'  $V_{gs}$  waveforms with different gate parasitic inductance

**Figure 4.19:** CS-GD and VS-GD  $V_{gs}$  Waveforms Under Different Gate Loop Parasitic Inductances.

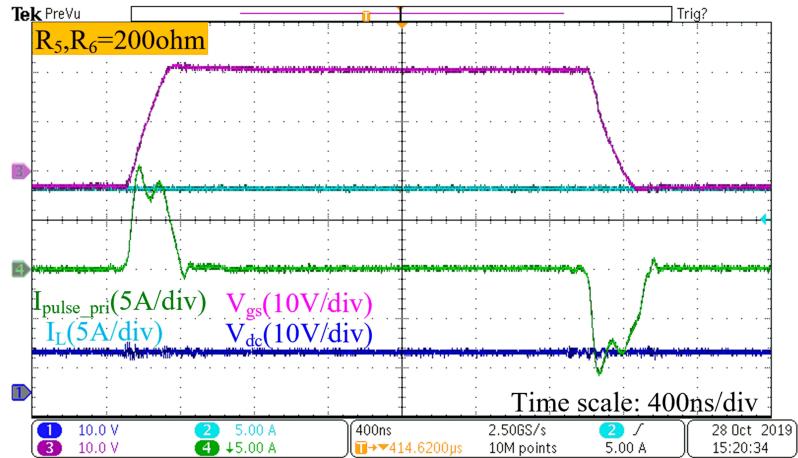


(a) CS-GD three channels'  $V_{gs}$  waveforms with different gate resistance

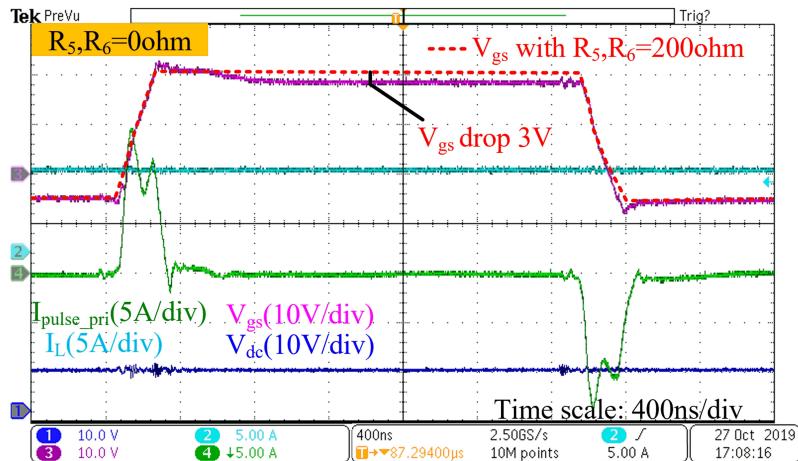


(b) VS-GD three channels'  $V_{gs}$  waveforms with different gate resistance

**Figure 4.20:** CS-GD and VS-GD  $V_{gs}$  Waveforms Under Different Gate Loop Resistances.

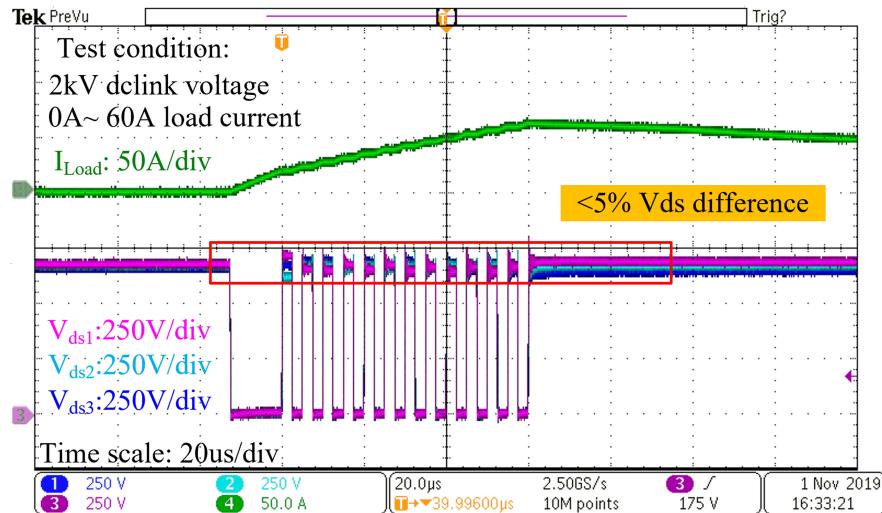


(a) Typical waveforms of CS-GD with 200ohm  $R_5$  and  $R_6$



(b) Typical waveforms of CS-GD with 0ohm  $R_5$  and  $R_6$   
(red dash line is the  $V_{gs}$  waveform with 200ohm  $R_5$  and  $R_6$ )

**Figure 4.21:** De-magnetizing Performance of the Proposed CS-GD Auxiliary Circuit:  $V_{gs}$  Waveforms With (a) 200  $\Omega$  Damping Resistor and (b) 0  $\Omega$  Damping Resistor.

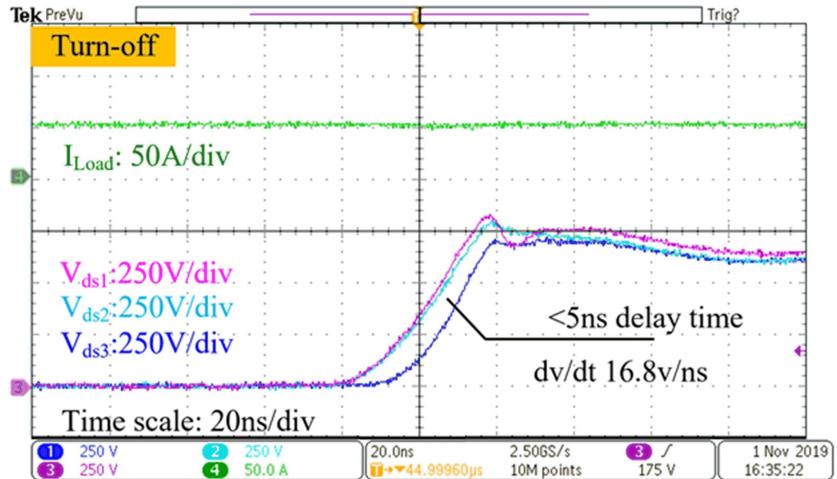


**Figure 4.22:** Multi-pulse Test Power Loop Signals:  $V_{ds}$  of Three SiC MOSFETs and Load Current Waveforms.

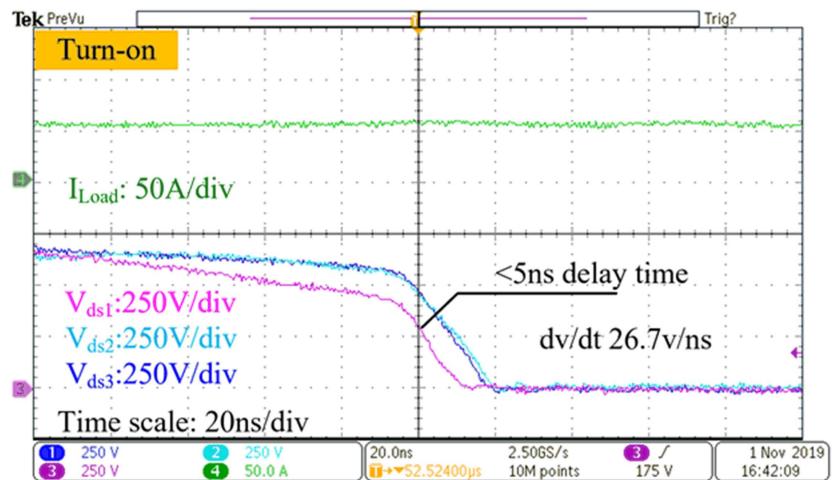
200  $\Omega$   $R_5$  and  $R_6$ . The magnetizing current based on 4.14 is 86.2 mA. With  $R_6$  of 200  $\Omega$ , the time of magnetizing current damping to zero can be calculated as 140 ns per 4.15. Fig. 4.21 shows the experiment results. The waveform in purple color is the  $V_{gs}$  of SiC MOSFET. The waveform in green color is the total gate current. With  $R_5$  and  $R_6$  of 0  $\Omega$ ,  $V_{gs}$  drops 3V after the positive current pulse, as shown in Fig. 4.21(b). It is because the transformer magnetizing current cannot be damped quickly within the time when Zener diode is still at low impedance. With  $R_5$  and  $R_6$  of 200  $\Omega$ , the gate voltage can maintain steady 20 V after the current pulse. It is verified that the resistors on the auxiliary gate driving circuit can increase the transformer winding voltage and damp the magnetizing current in a short time. In this way, the drop of the  $V_{gs}$  after the current pulse is avoided.

## 2. $V_{ds}$ Voltage Balancing Performance

The CS-GD generates three synchronous  $V_{gs}$  voltages within 5 ns time delay. Under this gate driving condition, the multi-pulse test is conducted, and the full-scale waveform is shown in Fig. 4.22. Fig. 4.23 shows the zoom-in waveforms of

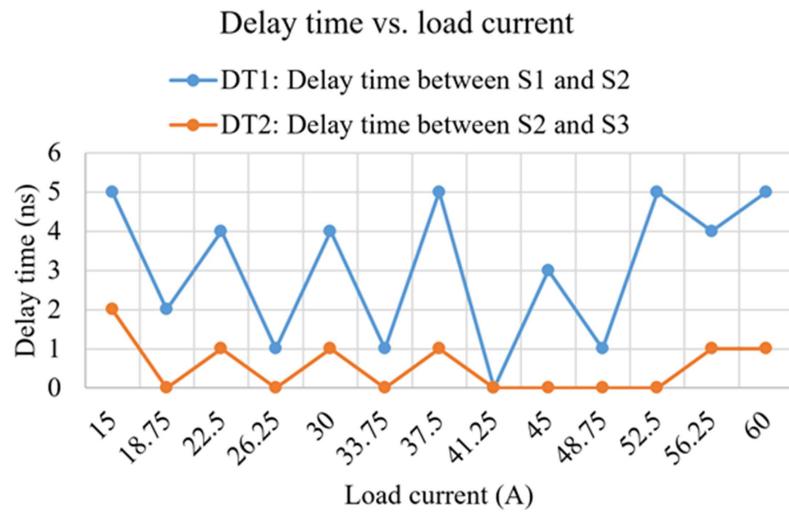


(a) Three channel  $V_{ds}$  signals zoom-in view of Figure 21  
turn-off at 56A load current

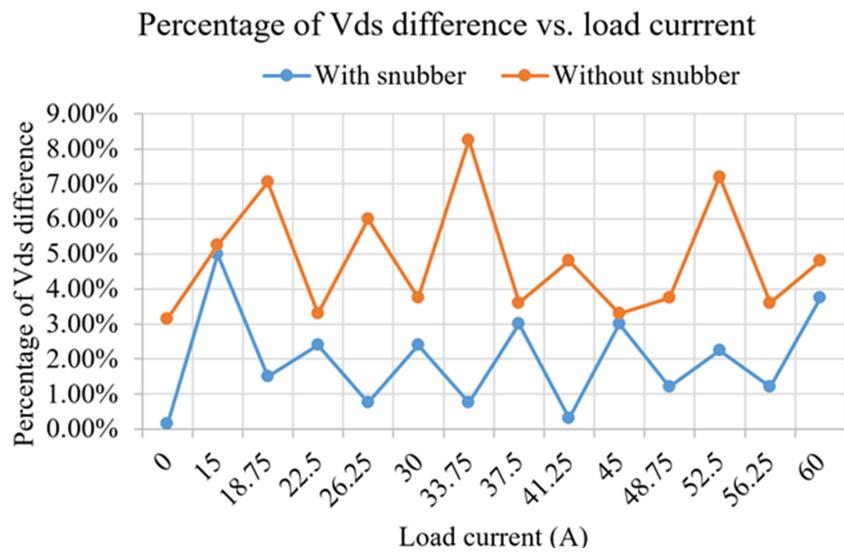


(b) Three channel  $V_{ds}$  signals zoom-in view of Figure 21  
turn-on at 56A load current

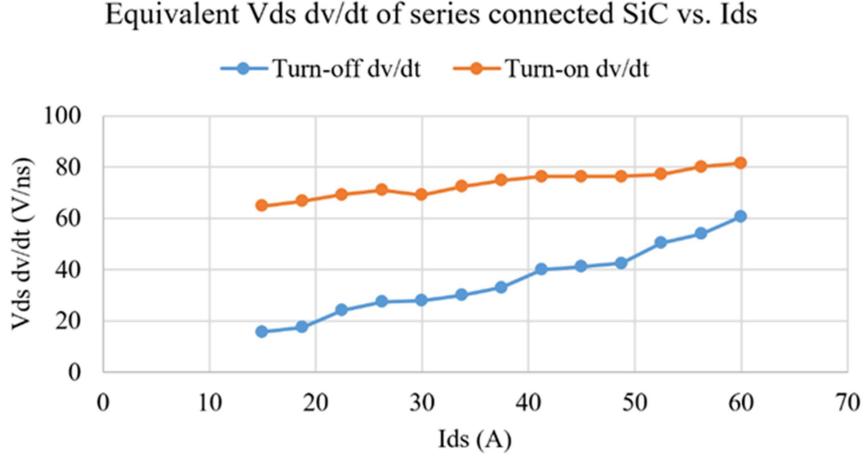
**Figure 4.23:**  $V_{ds}$  of Three SiC MOSFETs and Load Current Waveforms.



**Figure 4.24:**  $V_{ds}$  Channel-to-channel Delay Time  $dT_1$  and  $dT_2$  at Different Drain-source Current.



**Figure 4.25:**  $V_{ds}$  Voltage Difference With and Without Snubber Circuit at Different Load Current.



**Figure 4.26:** Equivalent  $V_{ds}$   $dv/dt$  of the Block at Different Drain-source Current.

turn-on and turn-off transient at 56 A load current. For the  $V_{ds}$  rising edge and falling edge, the channel-to-channel delay time is smaller than 5 ns. The  $V_{ds}$  channel-to-channel delay time  $dT_1$  and  $dT_2$  at different drain-source current is shown in Fig. 4.24. The data is the average value based on ten times of the same test. The  $V_{ds}$  voltage difference at different load current is shown in Fig. 4.25. At 2 kV dc-link voltage, the absolute  $V_{ds}$  difference is from 0V to +33 V which is within 5% of the average  $V_{ds}$ . Fig. 4.26 shows the equivalent  $V_{ds}$   $dv/dt$  of the series-connected SiC MOSFETs block at different load current. For example, the equivalent  $dv/dt$  of the series-connected SiC MOSFETs block is 80.1 V/ns for turn-on and 50.4 V/ns for turn-off at 56 A load current. The parasitic capacitors induced common mode current issue is not obvious in the experiment. There are three reasons:

- I. The CS-GD gate current is large and constant (2.8 A). According to the analysis in [172], a larger gate current causes a smaller voltage unbalance. It is because a larger gate current leads to a smaller miller plateau voltage. Therefore, all devices mainly transfer the turn-off current to charge the junction capacitor,

causing smaller difference in  $V_{ds} dv/dt$ . In other words, when the gate current is high, the  $I_{ds}$  turn-off current mainly charges the device junction capacitor, dominating the  $V_{ds} dv/dt$ . Even though the gate currents are different because of different gate common mode currents, the  $V_{ds} dv/dt$  of each series-connected device is similar. The detailed analysis about this effect can be found in [172].

- II. The gate-to-ground capacitance is small. Because discrete devices have negligible gate-to-baseplate capacitance, and the CS-GD has only one isolation barrier, avoiding parasitic capacitors introduced by the isolated power supplies. The gate-to-ground capacitance is mainly the transformer inter-winding capacitance for CS-GD. This capacitance is 12.7 pF/16.1 pF/13.2 pF of three series-connected channels using the measurement method in [173] and can be designed to be smaller if necessary. For the conventional voltage source gate driver, the parasitic capacitance of the state-of-the-art isolated gate driver and power supply is around 5-20 pF [14], which is comparable to CS-GD case.
- III. The drain/source terminal parasitic capacitance is negligible because discrete devices are used. For the PCB layout of discrete device package TO-247, the parasitic capacitance of drain/source-to-ground is around 10 pF, while the junction capacitance of device is 150 pF. Thus, the parasitic capacitance effect is not obvious.

### 3. Snubber Circuit Performance Discussion

Based on the snubber design guideline in section III, the measured  $V_{ds}$  delay times  $dT_1$  and  $dT_2$  are 5 ns and 2 ns, respectively. And the maximum allowed voltage difference  $k$  in 4.25 is set to be 20%. Therefore, per the proposed snubber circuit example calculation, the snubber parameters in this test are 2200 pF and 10  $\Omega$ . The  $C_s$  is not 6 nF as the value in the calculation example because the  $dT_2$  is 5ns in the

example and the measured  $dT_2$  in Fig. 4.24 is 2 ns.

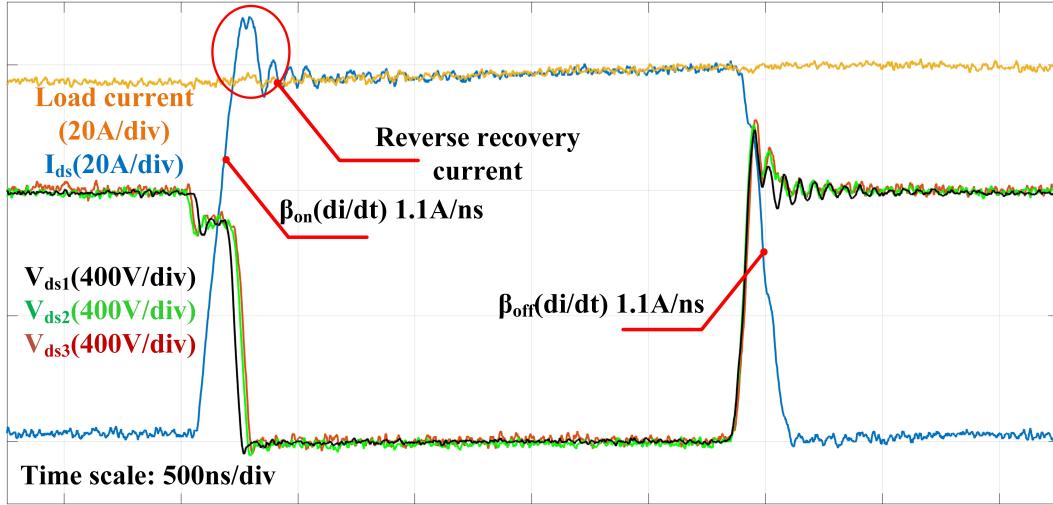
In Fig. 4.25, the  $V_{ds}$  voltage difference with and without the snubber circuit is compared in full load range. Without the snubber circuit, the maximum percentage of the voltage difference is 8%. With the snubber circuit, this number reduces to 5%. This means that the gate loop difference is the main cause of unequal voltage sharing. The power loop and device part-to-part difference is not big, and the block of series-connected SiC MOSFETs can also work properly without the snubber circuit. With the snubber circuit, the  $V_{ds}$  voltage sharing performance can be improved, and under the synchronous  $V_{gs}$ , the snubber circuit can be designed only for the power loop and device part-part difference. Therefore, the snubber circuit is also proposed in this chapter to provide an optional choice for the power loop difference and device difference compensation. In other words, the main difference is caused by gate-loop difference which has been overcome by the proposed CS-GD. For the power-loop difference and device part-to-part difference, snubber can be a solution. The proposed CS-GD together with the snubber circuit provides a comprehensive solution to this unequal  $V_{ds}$  sharing problem.

In conclusion, if the snubber circuit is used to compensate both gate loop difference and power loop difference, the snubber will be big and lossy. Besides, the big snubber will slow down the device switching speed. If the gate loop difference is compensated by the proposed CS-GD, the snubber only has to solve the issue of power-loop difference and device tolerance. The snubber loss can be reduced, and the switching speed will not be largely slowed down.

It should be noted that the  $V_{ds}$  voltage sharing performance is better than the pre-set 20% voltage difference, because under the worst-case assumptions mentioned in the snubber design guideline, the snubber is over-designed to some extent.

To evaluate the snubber loss and size, the snubber circuit based on the VS-GD [69]

is compared. It shows 9.7% voltage difference with the large and lossy snubber (33 nF and  $4.7\ \Omega$ ). Per 4.26, the power loss of snubber in this test (using CS-GD) is only 6.7% of that using VS-GD. Because the snubber power loss is mainly dissipated by the snubber resistor  $R_s$ , the  $R_s$  with smaller power rating can be selected. Therefore, the snubber size can be reduced.



**Figure 4.27:**  $V_{ds}$  and  $I_{ds}$  Waveforms at 56 A Load Current for Loss Calculation.

As shown in Fig. 4.22,  $dT_1$  is 5ns and  $dT_2$  is 2 ns at 56 A/2 kV operation condition. Per 4.37, the additional loss induced by unequal  $V_{ds}$  is  $31.67\ \mu J$ , where  $\alpha_{on}$  is 26.7 V/ns,  $\alpha_{off}$  is 16.8 V/ns. Fig. 4.27 shows that the  $di/dt$  ( $\beta_{on}, \beta_{off}$ ) is 1.1 A/ns. Therefore, the total switching loss is 12.89 mJ per ???. The additional loss only accounts for 0.25% of total switching loss. The reverse recovery charge is  $1.05\ \mu C$ , and reverse recovery loss is 2.1 mJ.

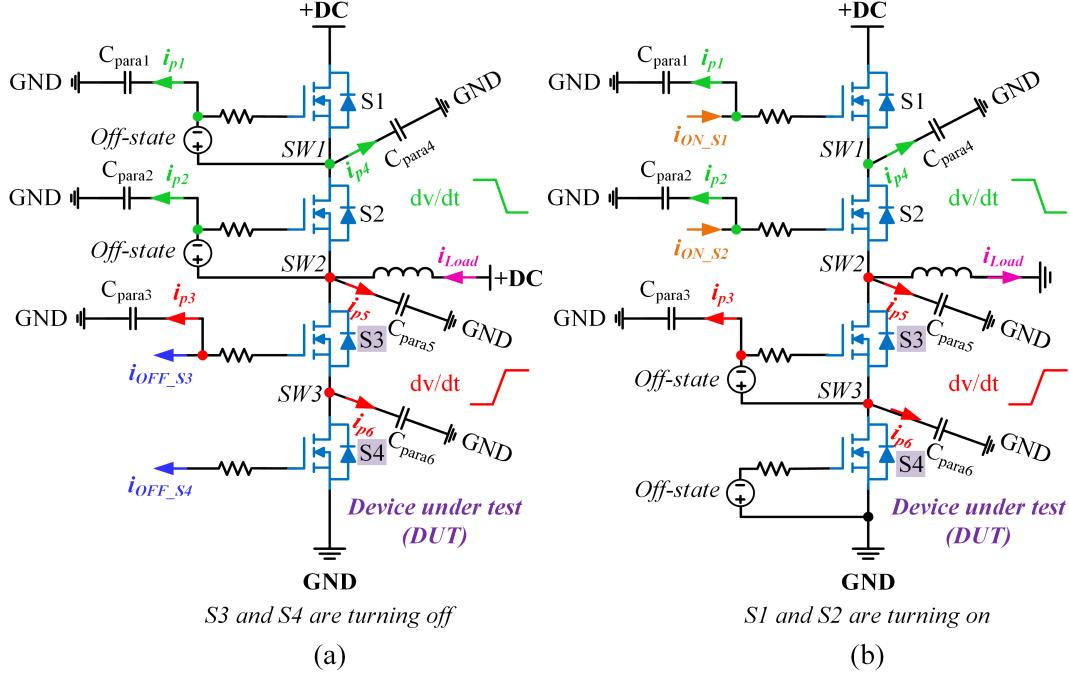
#### **4.1.2 Voltage Balancing Strategy 2: An Active Current Mirror Based Current Source Gate Driver with High Resolution Voltage Balancing Control**

The dynamic voltage imbalance can be caused by: 1) the discrepancies in the gate driving loops; 2) the device parameter tolerance; and 3) the device-to-ground displacement currents. For the discrepancies in the gate driving loops, it can be alleviated by using symmetrical connections and circuit layouts for different channels in the stack. Besides, the current source gate driver can suppress this gate loop difference, which has been verified in the open loop current source gate driver. For the device parameter tolerance, it can be overcome by adding small external gate-to-source/drain-to-source capacitors. However, for the device-to-ground displacement currents, it is hard to be passively compensated because the device-to-ground parasitic capacitance is typically unknown. Therefore, the active compensation mechanism should be employed. Basically, the major focus of this study is to actively compensate for the voltage imbalance brought by the device-to-ground displacement currents. The effects of the device-to-ground displacement currents on the dynamic voltage sharing for the series-connected devices have already been discussed in the previous studies [70, 172, 174–179]. A short review of those effects in different switching scenarios is conducted as follows.

##### **A. Root Cause of Voltage Unbalance at Different Switching Scenarios**

###### **I. Soft Turn-off Scenario**

As is shown in Fig. 4.28(a), two SiC MOSFETs are connected in series for both upper arm and lower arm in a phase-leg. The load inductor is paralleled with the upper arm. The upper arm switches (S1 and S2) are in the gate-off



**Figure 4.28:** (a) Device-to-ground Displacement Currents During the Lower Arm Switches (DUT) Soft Turn-off Transient. (b) Device-to-ground Displacement Currents During the Lower Arm Switches (DUT) Hard Turn-off Transient.

state, and the lower arm switches (S3 and S4) are actively turning off. The lower arm switches are regarded as the device under test (DUT). Since the load current will assist the charging/discharging of the device junction capacitances during this transient, the lower arm switches are experiencing a soft turn-off process. For the ‘soft’ turn-off scenario, the device drain-to-source  $dv/dt$  can be restricted by either the device gate current ( $i_g$ ) or the device drain current ( $i_d$ ) [175], as illustrated in the following equation:

$$\begin{cases} i_g \geq C_{gd}dV_{ds}/dt \\ i_d \geq (C_{gd} + C_{ds})dV_{ds}/dt \end{cases} \quad (4.39)$$

where  $C_{gd}$  is the device gate-to-drain capacitance (Miller capacitance) and  $C_{ds}$  is the device drain-to-source capacitance.

For the devices with large input capacitance, such as Si devices and high-current SiC power modules, drain-to-source  $dv/dt$  is typically restricted by the gate current during the soft turn-off transient. Most of the gate driver supplied current is utilized to charge the Miller capacitance during the rising  $dv/dt$  transient. However, for the devices with small input capacitance, such as discrete WBG devices (SiC and GaN) or even Si super-junction MOSFETs, the device drain-to-source  $dv/dt$  is typically determined by the drain/load current during the soft turn-off transient. With the excessive gate driver supplied current, the device gate-to-source capacitance ( $C_{gs}$ ) will be quickly discharged below its threshold. Therefore, the device channel can be already cut off before its drain-to-source voltage starts to rise. Then the device becomes an equivalent junction capacitor, and the charging speed of the junction capacitor is determined by the drain/load current amplitude [175]. This fast turn-off property is beneficial for reducing the device turn-off energy because the overlapping between the device drain-to-source voltage and current is minimized. The extremely fast turn-off process of the discrete WBG devices is also called the nearly ‘lossless’ turn-off in [172].

However, due to the device-to-ground parasitic capacitances, the actual gate current and drain current of the series-connected switches are different even with well-matched gate drivers and device parameters. The device gate-to-ground parasitic capacitances are labeled as  $C_{para1}$ ,  $C_{para2}$ , and  $C_{para3}$  in Fig. 4.28. Since there is almost no  $dv/dt$  between the gate of  $S_4$  and the power ground, minimal displacement current will be produced. The parasitic capacitance between the gate and ground for  $S_4$  is not shown in the figure. In the real system, the gate-to-ground parasitic capacitances consist of the isolation capacitance for the isolated DC/DC power supplies, the isolation capacitance for the isolated

gate drivers, and the device gate to heat sink parasitic capacitance (if the heat sink is grounded). The device drain/source-to-ground parasitic capacitances are labeled as  $C_{\text{para}4}$ ,  $C_{\text{para}5}$  and  $C_{\text{para}6}$  in Fig. 4.28. Similarly, since there is no  $dv/dt$  between the drain of  $S_1$  and the power ground, no displacement current will be generated. The parasitic capacitance between the drain and ground for  $S_1$  is not shown in the figure as well. In the real system, the major drain-to-ground parasitic capacitance comes from the PCB interlayer capacitance for the discrete devices. For the fast-switching SiC-based power converters, the flux-cancellation PCB layout techniques are usually employed to reduce the power loop parasitic inductance. To achieve the flux-cancellation between the switching nodes and the power ground, they are normally placed in two adjacent layers of a PCB and overlapped pretty well. Suppose the overlapping area between the switching node and the power ground is only  $10 \text{ mm} \times 10 \text{ mm}$ . In that case, the interlayer stray capacitance will be around  $30 \text{ pF}$ , which is already significant compared with the junction capacitance of the discrete SiC devices.

Based on Fig. 4.28(a), the gate currents of  $S_3$  and  $S_4$  can be written as:

$$\begin{aligned} i_{\text{gate}(S3)} &= i_{\text{OFF}(S3)} + i_{p3} \\ i_{\text{gate}(S4)} &= i_{\text{OFF}(S4)} \end{aligned} \quad (4.40)$$

where  $i_{\text{OFF}(S3)}$  and  $i_{\text{OFF}(S4)}$  are the gate driver supplied turn-off currents for  $S_3$  and  $S_4$ , respectively;  $i_{p3}$  is the gate-to-ground displacement current for  $S_3$ .

Meanwhile, due to the existence of the drain/source-to-ground displacement currents, the relation between the drain currents of  $S_3$  and  $S_4$  can be expressed as:

$$i_{\text{drain}(S3)} = i_{\text{drain}(S4)} + i_{p6} \quad (4.41)$$

where  $i_{p6}$  is the drain-to-ground displacement current for  $S_4$ .

It is clear that  $S_3$  has both higher gate current and higher drain current than  $S_4$ . As discussed earlier, the drain-to-source  $dv/dt$  is typically determined by the drain current for the discrete SiC devices. If no compensation mechanism is implemented, the top-sitting switch  $S_3$  will have higher  $dv/dt$  than the bottom-sitting switch  $S_4$  due to the bigger drain current, which can eventually cause the over-voltage breakdown.

## II. Hard Turn-off Scenario

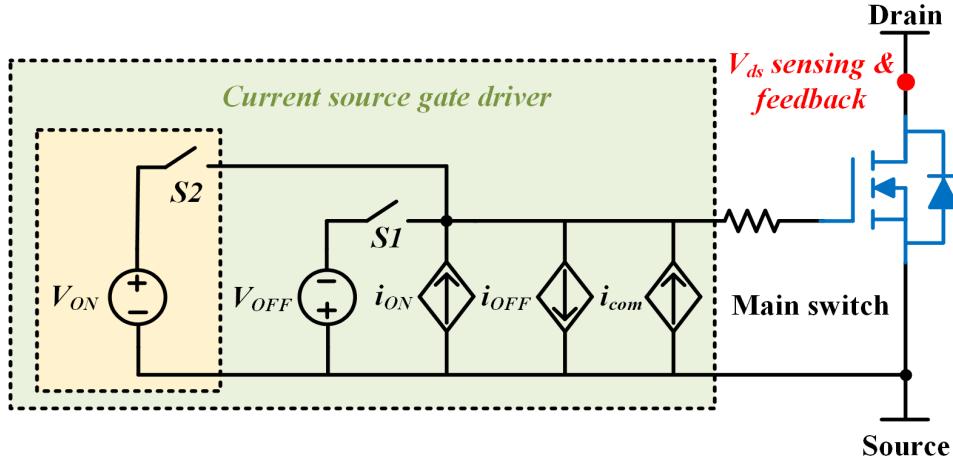
As is shown in Fig. 4.28(b), the upper arm switches ( $S_1$  and  $S_2$ ) are actively turning on, and the lower arm switches ( $S_3$  and  $S_4$ ) are in the gate-off state. The load inductor is paralleled with the lower arm for this scenario. Since the load current will not assist charging/discharging of the device junction capacitances during this transient, the upper arm switches are experiencing ‘hard’ turn-on. Meanwhile, the drain-to-source voltage of the lower arm switches will be passively pulled up. Therefore, the lower arm switches can be regarded as experiencing ‘hard’ turn-off.

Since the lower arm switches are already in the gate-off state during this transient, the  $dv/dt$  will be determined by the drain current from the dc-link. Based on (4.41), the top-sitting switch  $S_3$  has a higher drain current than the bottom-sitting switch  $S_4$  due to the existence of the drain-to-ground displacement current. Therefore, the top-sitting switch  $S_3$  will have higher  $dv/dt$  than the bottom-sitting switch  $S_4$ , which can eventually cause the over-voltage breakdown. As mentioned earlier, this phenomenon is also called the voltage imbalance of series-connected body-diodes in [172]. The voltage imbalance for this scenario is hard to compensate from the gate side with the conventional voltage source gate driver because the gates are already in the off state for the switches

with rising drain-to-source voltages.

It should be mentioned that the device-to-ground displacement currents also affect the slew rate of falling  $dv/dt$  for the turn-on switches. As long as the turn-on timing is very synchronized for all the switches in the stack, the over-voltage breakdown is unlikely to occur during the turn-on transient. However, if there is several nanosecond turn-on timing difference among the series-connected switches, the over-voltage can still occur [72]. The drain-to-source voltage of the delayed turn-on switch will start to rise at first and then starts to fall when its gate-to-source voltage reaches the turn-on threshold. Therefore, it is still very critical to guarantee the consistency of the gate driving circuits for different channels in the stack [175].

## B. Proposed Voltage Balancing Schemes in Different Switching Scenarios



**Figure 4.29:** Simplified Schematic of Proposed Current Source Gate Driver.

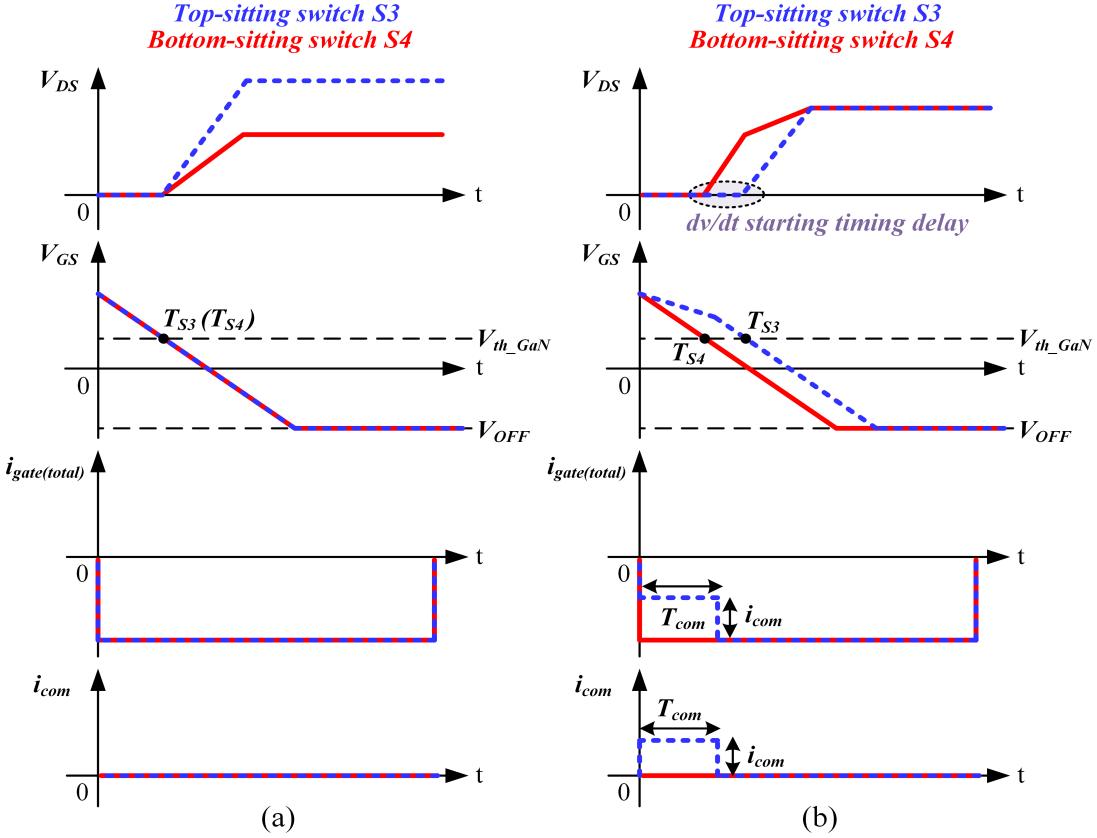
To address the voltage imbalance issue, the current source gate driver strategy is adopted. The basic idea is to utilize additional compensation gate current to counteract the effects from the device-to-ground displacement currents. The simplified

schematic of the proposed current source gate driver is shown in Fig. 4.29. The critical operating principles are highlighted as follows.

- 1) The main switch turn-on and turn-off gate currents are provided by the controlled current sources  $i_{ON}$  and  $i_{OFF}$ , respectively. Additional compensation current is generated from another controlled current source  $i_{com}$ , and the compensation current direction is opposite to the turn-off gate current.
- 2) The negative voltage source ( $V_{OFF}$ ) is still required to sustain the steady-state turn-off voltage. However, the voltage source is only for clamping the steady-state gate-to-source voltage rather than providing the transient turn-off gate current. The auxiliary switch  $S_1$  determines when the active negative voltage clamping is kicked in the circuit.
- 3) For the voltage-driven type SiC devices, another positive voltage source ( $V_{ON}$ ) is needed for clamping the steady-state turn-on gate-to-source voltage, which is controlled by the auxiliary switch  $S_2$ .
- 4) Though the current direction of  $i_{ON}$ ,  $i_{com}$  and  $i_{on-state}$  is the same, separate controlled current sources are desired instead of using a single one. The turn-on gate current is typically in the range of hundreds of mA or even higher, but the compensation gate current and the on-state gate current are in the range of tens of mA. If a single controlled current source is utilized, the current regulation range is huge, which is hard to meet the high-resolution and fast-transient requirement for the gate driver of WBG devices. This is the same reason for employing the additional small current source  $i_{com}$  to precisely tune the overall gate current rather than directly regulating the output current of  $i_{OFF}$ .

The following part presents the voltage balancing schemes with the proposed current source gate driver for both soft and hard-switching scenarios.

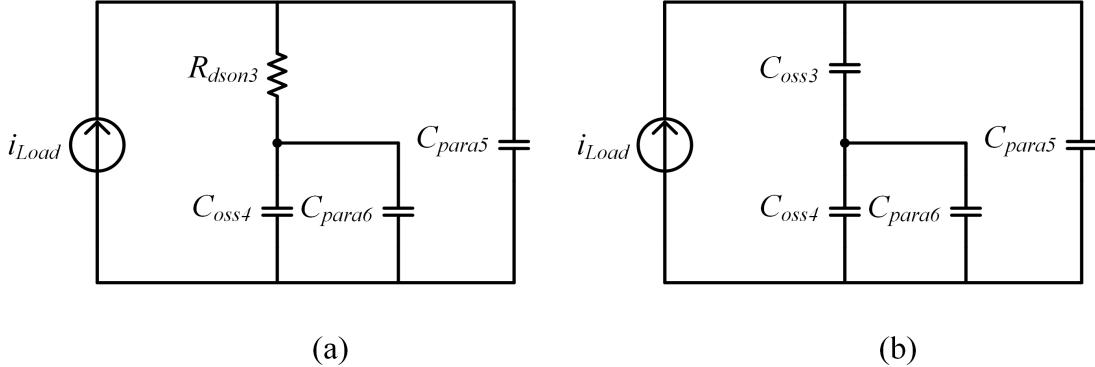
## I. Voltage Balancing Scheme in Soft Turn-off Scenario



**Figure 4.30:** Voltage Balancing Scheme in Soft Turn-off Scenario With Current Source Gate Driver. (a) Without Active Gate Current Control. (b) With Active Gate Current Control.

Due to the small input capacitance, the gate of SiC MOSFET can be quickly discharged below the threshold before its drain-to-source voltage starts to rise. Therefore, the rising  $dv/dt$  can not be directly regulated by tuning the supplied gate current amplitude. However, the starting timing of the rising  $dv/dt$  can be adjusted, which may compensate for the voltage imbalance brought by the slew rate difference. Actually, this voltage balancing strategy is the so-called active gate delay control in [72, 174]. The drawbacks of the active gate delay control with the voltage source gate driver have already been discussed earlier in the introduction part. The implementation of active gate delay control by

employing the current source gate driver is shown in Fig. 4.30. The circuit diagram for the soft turn-off scenario is referred to Fig. 4.28(a).



**Figure 4.31:** Equivalent Circuit of Lower Arm at Soft Turn-off Scenario When (a) S3 On, S4 Off. (b) S3, S4 Off.

As is shown in Fig. 4.30(a), without the active gate current control, the top-sitting switch  $S_3$  exhibits higher  $dv/dt$  compared with the bottom-sitting switch  $S_4$ , due to the higher drain current. By regulating the pulse width ( $T_{\text{com}}$ ) or amplitude ( $i_{\text{com}}$ ) of the compensation gate current, the  $dv/dt$  starting timing ( $T_{S3}$ ) of the top-sitting switch  $S_3$  is delayed by certain duration. The equivalent circuits during the soft turn-off transient are shown in Fig. 4.31. The parameters are consistent with the parameters defined in Fig. 4.28. When  $S_4$  is turned off and  $S_3$  is still on,  $S_3$  is a small on-state resistor ( $R_{\text{dson}}$ ), as shown in Fig. 4.31(a). Hence, the drain-to-source voltage of  $S_3$  remains very low during this interval. Once  $S_3$  is turned off, it is equivalent to a junction capacitor ( $C_{\text{oss}}$ ), as shown in Fig. 4.31(b). Then the drain-to-source voltage of  $S_3$  will rise with a larger slew rate compared to  $S_4$ , due to the higher drain current. As a result, both switches can have equalized off-state drain-to-source voltages, though the  $dv/dt$  of the two switches are not same, as shown in Fig. 4.30(b).

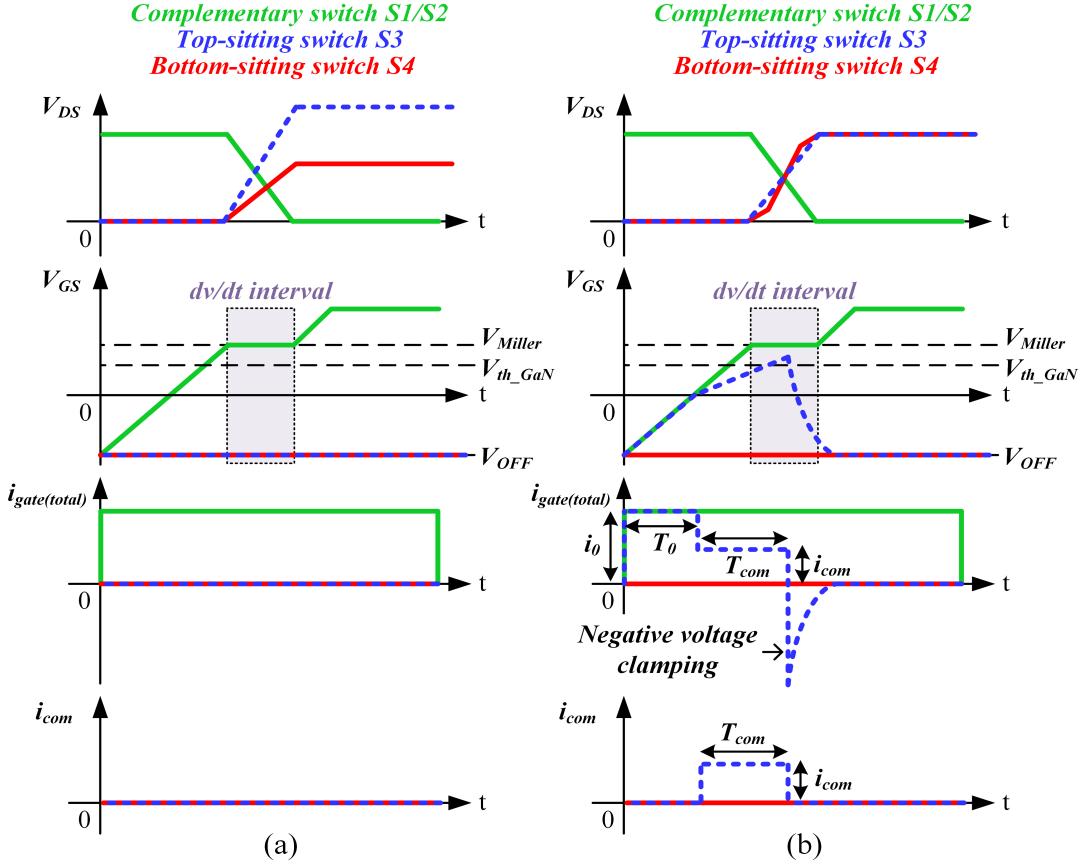
The product of  $T_{\text{com}}$  and  $i_{\text{com}}$  is actually the compensation gate charge ( $Q_{\text{com}}$ ).

The two control variables  $T_{\text{com}}$  and  $i_{\text{com}}$  can be tuned to achieve the desired voltage sharing. The resolution of  $T_{\text{com}}$  is restricted by the controller minimum clock cycle. As mentioned earlier, the sub-nanosecond unit time step is required for the controller if the signal timing is the only control variable, which is the case for the voltage source gate driver [72, 174]. The compensation current amplitude can be set at a relatively small value for the proposed current source gate driver. High-resolution tuning can still be achieved even with a larger unit time step for the compensation pulse width. Hence, the voltage balancing control will be more reliable for the proposed approach.

## II. Voltage Balancing Scheme in Hard Turn-off Scenario

As discussed earlier, the voltage imbalance in the hard turn-off scenario is caused by the drain-to-ground displacement currents. Since the switches with the rising drain-to-source voltage are already in the gate-off state during the  $dv/dt$  transient, the voltage imbalance can not be suppressed by adjusting the turn-off timing of the switches. One of the strategies is to trigger the gate of the switch that has higher  $dv/dt$  during the rising  $dv/dt$  transient to reduce the device impedance, so the average  $dv/dt$  during the switching transient is reduced. Then the well-balanced voltage sharing among the switches can be achieved [175]. The implementation of this strategy by employing the current source gate driver is shown in Fig. 4.32. The circuit diagram for the ‘hard’ turn-off scenario is referred to Fig. 4.28(b).

As is shown in Fig. 4.32(a), without the active gate current control, the top-sitting switch  $S_3$  exhibits higher  $dv/dt$  compared with the bottom-sitting switch  $S_4$ , due to the higher drain current. In the hard-switching scenario, the  $dv/dt$  starts when the gate-to-source voltage of the complementary switches ( $S_1/S_2$ )



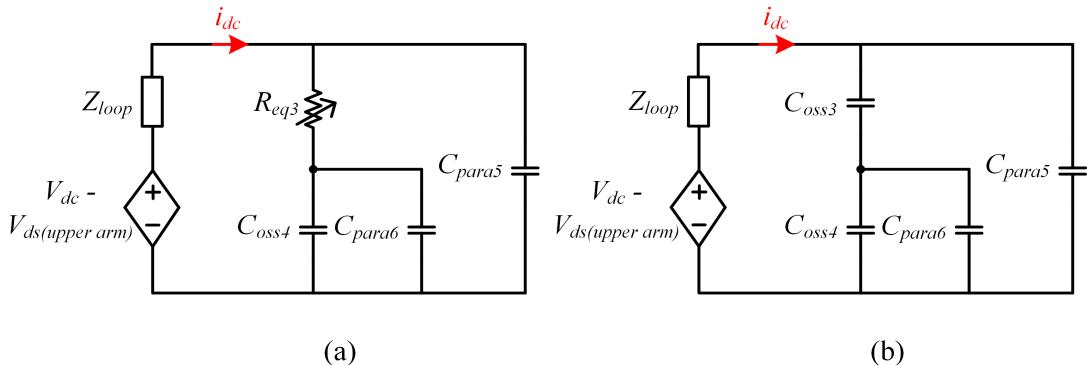
**Figure 4.32:** Voltage Balancing Scheme in Hard Turn-off Scenario. (a) Without Proposed Voltage Balancing Scheme. (b) With Proposed Voltage Balancing Scheme.

reaches the turn-on Miller plateau. During this interval, both  $S_3$  and  $S_4$  are in the gate-off state without active gate current control. To suppress the voltage imbalance, the gate of  $S_3$  is actively triggered, as shown in Fig. 4.32(b). The proposed active current control in the ‘hard’ turn-off scenario has the following three steps.

- 1) At the beginning, the large gate current  $i_0$  is actively injected into the gate with the duration of  $T_0$ . This current can be considered as the ‘pre-charge’ current, and it can be generated by the turn-on current source ( $i_{ON}$  in Fig. 4.29). Hence, the gate-to-source voltage of  $S_3$  rises simultaneously with the gate-to-

source voltage of the complementary switches ( $S_1/S_2$ ) during this interval. It should be mentioned that the large ‘pre-charge’ current  $i_0$  is used to reduce the rise time of the gate-to-source voltage for  $S_3$ . If the small compensation current is applied during the entire interval, the starting timing of the compensation current needs to be advanced a lot, which will extend the required dead-time between the turn-off and turn-on switches. The fixed duration  $T_0$  can be selected as the time needed for the gate-to-source voltage of  $S_3$  rising from the negative turn-off voltage to zero.

- 2) At  $T_0$ , the injection of  $i_0$  is stopped, and the small compensation current  $i_{\text{com}}$  is added into the gate to continue elevating the gate-to-source voltage of  $S_3$ . The pulse width of the compensation gate current is  $T_{\text{com}}$ . The small amplitude of  $i_{\text{com}}$  achieves the ‘fine-tuning’ of the gate-to-source voltage of  $S_3$ .
- 3) At  $T_0 + T_{\text{com}}$ , the injection of  $i_{\text{com}}$  is stopped, and the active negative voltage clamping is kicked in the circuit to turn off the gate of  $S_3$ . Eventually,  $S_3$  is completely in the gate-off state again.



**Figure 4.33:** Equivalent Circuit of Lower Arm at Hard Turn-off Scenario When (a)  $V_{gs}$  of  $S_3$  Is Around the Threshold. (b)  $V_{gs}$  of  $S_3$  Below the Threshold.

During the  $dv/dt$  interval, when the gate-to-source voltage ( $V_{gs}$ ) of  $S_3$  exceeds the threshold, its impedance will be reduced significantly. Since  $V_{gs}$  of  $S_3$  is

just above the threshold, it should be regarded as a large equivalent resistor ( $R_{\text{eq}}$ ) rather than the small on-state resistor ( $R_{\text{dson}}$ ). The equivalent circuit for this situation is shown in Fig. 4.33(a). The parameters are consistent with the parameters defined in Fig. 4.28. When the gate-to-source voltage of  $S_3$  is below the threshold, it goes back to the high-impedance junction capacitor ( $C_{\text{oss}}$ ), as shown in Fig. 4.33(b). Therefore, with the proposed strategy, the average  $dv/dt$  of  $S_3$  can be reduced, and the equalized voltage sharing among the series-connected switches can be obtained, as shown in Fig. 4.32(b). It should be noted that though  $V_{\text{gs}}$  of  $S_3$  is elevated during the  $dv/dt$  interval, the gate of  $S_4$  is always completely off during the entire interval. Hence, the dc-link shoot-through will not occur for the proposed voltage balancing strategy.

Similar to the ‘soft’ turn-off scenario,  $T_{\text{com}}$  and  $i_{\text{com}}$  are the two free control variables. By appropriately regulating  $T_{\text{com}}$  and  $i_{\text{com}}$ , the well-balanced voltage sharing can be obtained for the series-connected switches in the stack. The detailed control algorithm of  $T_{\text{com}}$  and  $i_{\text{com}}$  will be introduced later.

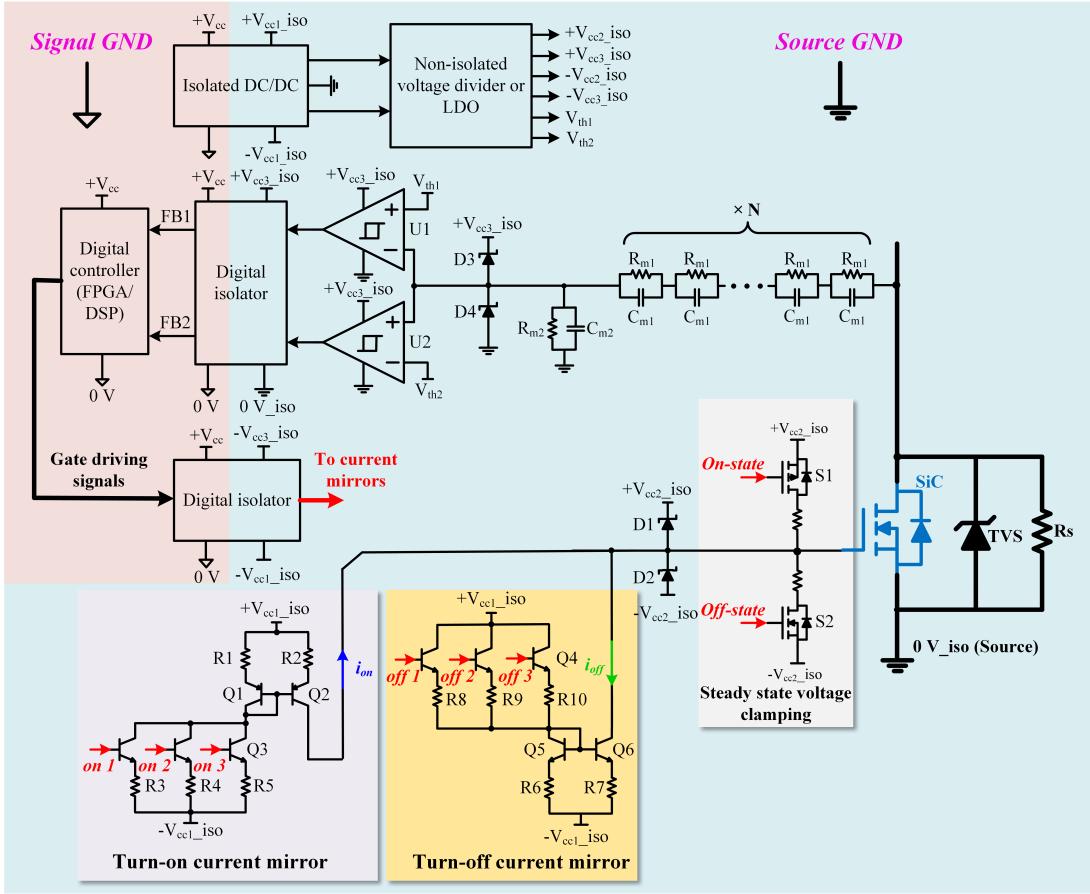
## C. Operating Principles of the Proposed Closed-loop Current Source Gate Driver

### I. Hardware Architecture

The complete schematic of the proposed current source gate driver is shown in Fig. 4.34. The detailed operating principles of each part are introduced as follows.

#### 1. Current Mirror Circuits

The current mirror circuits are utilized as the fast-responded, discontinuous current sources. The current source can be obtained by employing the current



**Figure 4.34:** Complete Schematic of the Proposed Current Source Gate Driver.

source inverter (CSI) as well [180]. However, there will be continuous flowing current in the switches for CSI, which will lead to the additional gate driving loss. The current mirror circuits are the voltage-controlled current sources. When the control voltage for the current mirrors is in the low state, there will be no ‘idle’ loss. Therefore, the gate driving loss for the current mirror-based current source gate driver is comparable to the conventional voltage source gate driver [175].

Two sets of current mirror circuit with total six amplitude control units are included in the proposed current source gate driver: the turn-on current mirror circuit (providing  $i_{ON}$ ); the turn-off current mirror circuit (providing  $i_{OFF}$ );

the compensation current mirror circuit (providing  $i_{\text{com}1}$  and  $i_{\text{com}2}$  for both turn-on and turn-off transients). Besides, the turn-on/turn-off speed as well as the magnitude of the compensation gate current can be regulated by enabling different level amplitude control units.

It is clear that the current mirror output current amplitude is determined by the driving voltage amplitude and the resistance value. To regulate the current amplitude, one solution is to change the driving voltage amplitude. Then the continuous varying output current can be realized. However, this solution needs to involve either the digital-to-analog converter (DAC) or the analog controller on the secondary side, which makes the structure of the gate driver more complicated. Another solution is to adjust the number of active current mirror's driving circuit. Since several current mirror's driving units are paralleled, the discrete varying output current can be obtained by enabling different level of current mirror driving units. The latter solution is employed to simplify the gate driver structure for the proposed current source gate driver.

For the practical design of the current mirror circuits, the following rules should be followed. First, the switching speed of the current mirror transistors should be fast enough to ensure the gate current for the main switch reach the desired value most of the time within its switching transients [175]. The commercial state-of-the-art small-signal transistors have minimal input and output capacitances. For example, for Diodes Incorporated 40 V/200 mA transistor pair (DMMT3904 W), the input capacitance and output capacitance is only 8 pF and 4 pF, respectively. Based on the characteristics of the small-signal transistors, they are able to provide a very high slew rate pulse current. Second, since the slew rate of the pulse current is also limited by the gate loop stray induc-

tance, the flux-cancellation technique should be employed for the gate driving loop PCB layout.

## 2. Voltage Clamping Circuits

One of the concerns for the current source gate driver is about the gate voltage clamping during the steady off-state or on-state due to the lack of the voltage source. The breakdown voltage of the Zener diode can be used to sustain the desired off-state or on-state gate-to-source voltage. However, it is found that the Zener diode clamping can not guarantee the stable off-state or on-state gate-to-source voltage in [175]. For the proposed current source gate driver, the isolated power supply is still needed to power the secondary side current mirror circuits, so the power supply can be directly used to clamp the gate voltage. As is shown in Fig. 4.34, during the off-state, the low-voltage MOSFET  $S_1$  will be turned on to clamp the gate-to-source voltage to the desired off-state voltage ( $-V_{cc2\_iso}$ ). The resistor  $R_9$  is used to limit the peak transient current amplitude flowing through  $S_1$ . The pulse current rating of  $S_1$  should exceed the peak transient current amplitude when  $S_1$  is just turned on. It should be noted that the off-state/on-state active voltage clamping is only kicked in during the steady off-state/on-state. The current mirror circuits still supply the device gate current during the switching transients, so the gate driver is still based on the controllable current sources. Moreover, the Schottky diodes  $D_1$  and  $D_2$  are utilized to suppress the gate-to-source voltage overshoot and undershoot during the switching transients.

## 3. Sensing Circuit and Window Comparator

The voltage divider circuit is employed to sense the device drain-to-source voltage during the steady off-state. The pure resistive voltage divider is found to

have a slow transient response, so the capacitive voltage divider is also employed [70, 74]. Based on the voltage divider operating principle, the sensed device drain-to-source voltage can be written as:

$$V_{\text{sense}} = \frac{R_{m2}}{N \cdot R_{m1} + R_{m2}} \cdot V_{ds} = \frac{\frac{C_{m1}}{N}}{\frac{C_{m1}}{N} + C_{m2}} \cdot V_{ds} \quad (4.42)$$

where  $V_{\text{sense}}$  is the sensed off-state drain-to-source voltage and  $N$  is the number of  $R_{m1}$  and  $C_{m1}$  parallel branches.

Larger capacitors ( $C_{m1}$  and  $C_{m2}$ ) will help to improve the sensing circuit transient response. However, the series-connected sensing capacitors are directly placed between the drain and source of the main switch, so they are equivalent to the snubber capacitors. If  $C_{m1}$  and  $C_{m2}$  are set to be too large, the sensing circuit will slow down the main switch switching speed and produce an additional loss. Therefore, the total value of the sensing capacitors should be significantly lower than the device junction capacitance value.

As is shown in Fig. 4.34, the sensed drain-to-source voltage is the input for the window comparator. The window comparator has two thresholds ( $V_{th1}$  and  $V_{th2}$ ), which indicate the desired off-state drain-to-source voltage range. The upper threshold  $V_{th1}$  represents the upper limit of the desired voltage range, while the lower threshold  $V_{th2}$  reflects the lower limit of the desired voltage range. If the desired voltage sharing is  $\pm 10\%$  of the average voltage, the two thresholds can be expressed as:

$$\begin{aligned} V_{th1} &= \frac{R_{m2}}{N \cdot R_{m1} + R_{m2}} \cdot \frac{V_{dc}}{M} \cdot 110\% \\ V_{th2} &= \frac{R_{m2}}{N \cdot R_{m1} + R_{m2}} \cdot \frac{V_{dc}}{M} \cdot 90\% \end{aligned} \quad (4.43)$$

where  $V_{dc}$  is the dc-link voltage and  $M$  is the number of the series-connected main switches.

Employing the window comparator brings two key benefits compared with the single threshold comparator. First, the over-voltage and the under-voltage of the main switch can be detected. When the under-voltage occurs, the over-voltage must occur for the other switches in the stack. Second, once the detected voltage is within the desired range, the digital tuning process is stopped, improving the closed-loop control's stability. The detailed adaptive digital tuning process in different switching scenarios will be explained later.

Meanwhile, it is obvious that the measured drain-to-source voltage is directly compared to the average value, so the voltage balancing strategy is independent for each switch. If the sensed voltages are compared with each other among the switches in the stack, the sequencing algorithm needs to be involved in the controller, which makes the control logic more complicated.

Moreover, when  $M$  switches are connected in series, the voltage balancing strategy can be implemented for  $M - 1$  switches. When the sensed drain-to-source voltages of the  $M - 1$  switches are all within the desired range, the last switch will achieve the desired drain-to-source voltage automatically. Hence, if two switches are connected in series, the proposed voltage balancing strategy can be employed for just one switch.

The output states of the window comparator are summarized in Table 4.4. The digital isolator is employed to transfer the outputs of the window comparator to the digital controller on the primary side. Based on the two feedback signals (FB1 and FB2), the controller will implement the appropriate tuning algorithm for the compensation current mirrors in the next control cycle. The detailed

**Table 4.4:** Output States of the Window Comparator.

Input	$FB_1$	$FB_2$	Voltage sharing
$V_{\text{sense}} < V_{\text{th2}}$	'1'	'0'	Under-voltage
$V_{\text{th2}} < V_{\text{sense}} < V_{\text{th1}}$	'1'	'1'	Desired voltage range
$V_{\text{sense}} > V_{\text{th1}}$	'0'	'1'	Over-voltage

tuning algorithms in different switching scenarios will be discussed later. It should be mentioned that the hysteresis comparators are recommended to prevent the state toggles caused by the ringings in the sensed voltage. Moreover, the Schottky diodes  $D_4$  and  $D_5$  are utilized to protect the input of the window comparator.

#### 4. Power Supplies

As is shown in Fig. 4.34, the isolated DC/DC power supply is needed for powering the current mirror circuits, digital isolators, current buffers, and comparators on the secondary side. A single isolated power supply with the non-isolated voltage dividers or low-dropout regulators (LDOs) can satisfy all the desired driving and signal conditioning voltage levels for the proposed current source gate driver.

First, the isolated DC/DC power supplies should have bidirectional outputs ( $+V_{\text{cc1,iso}}$  and  $-V_{\text{cc1,iso}}$ ) because the negative turn-off gate voltage is usually desired for the low-threshold GaN devices to prevent the mis-triggering during the switching transients [86]. The main switch source should be set as the ground for the secondary side of the isolated DC/DC power supply. Meanwhile, the current mirror power supply voltage should be wider than the GaN device gate-to-source voltage range to guarantee the BJTs operate in the forward active

region [175]. The desired gate-to-source voltage range for the main switch is from  $-V_{cc2\_iso}$  to  $+V_{cc2\_iso}$ .

Second, the driving voltage of the current mirrors should be referred to their negative supplied voltage (the current mirror ground), so it can be negative ( $-V_{cc3\_iso}$ ) referred to the main switch source ground.

Finally, since the window comparator refers to the main switch source ground, another positive supply voltage ( $+V_{cc3\_iso}$ ) should be generated for powering the comparator and the following digital isolator. It should be mentioned again that only the widest bidirectional voltages ( $+V_{cc1\_iso}$  and  $-V_{cc1\_iso}$ ) are directly obtained from the isolated DC/DC power supply. All the other voltage levels are generated from the secondary side non-isolated voltage dividers or LDOs. Since all the components sit on the main switch source ground, no additional isolation is needed for the secondary side of the proposed gate driver.

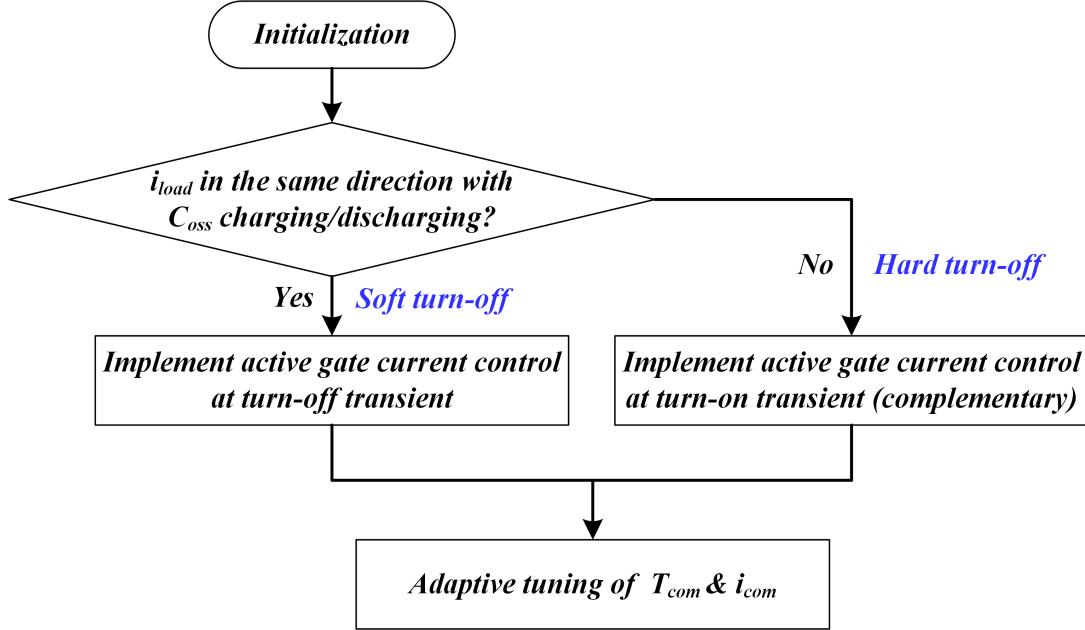
## 5. Static Voltage Sharing Resistors and Transient Voltage Suppressor Diodes

The static voltage sharing resistor ( $R_{10}$ ) is utilized for equalizing the steady-state voltage sharing. Its value should be in the range of hundreds of  $\text{k}\Omega$ , so the additional loss generated in the resistor is negligible. Since its value is so large, it will not help the device dynamic voltage balancing at all.

The transient voltage suppressor (TVS) diode should be employed to prevent the over-voltage breakdown of the main switch for the initial few switching cycles because the closed-loop control is one-control-cycle delayed. Since the TVS diode only dissipates the energy of voltage spike for very few switching cycles, the size of the TVS diodes can be very compact. Meanwhile, for the state-of-the-art TVS diode, the junction capacitance is only around 10 pF, which has minimal impact on the main switch switching speed. If higher blocking voltage

device is implemented, the TVS diodes can be series-connected to achieve the required breakdown voltage level.

## II. Control Algorithm



**Figure 4.35:** The Proposed Top-level Control Algorithm.

Based on the previous analysis, two control variables ( $T_{com}$  and  $i_{com}$ ) are available for balancing the voltage sharing of the series-connected switches, which is equivalent to regulate  $Q_{com}$ . For the proposed current source gate driver, the regulation range and resolution of  $i_{com}$  are restricted by the number of paralleled current mirrors. However, for  $T_{com}$ , it can be regulated in a large range with the controller minimum time step size. Therefore,  $T_{com}$  is selected as the major control variable.

In this way, the change of the compensation gate charge for each unit step is:

$$Q_0 = \Delta t \cdot i_{com} \quad (4.44)$$

where  $\Delta t$  is the unit time step in the controller.

It is clear that if  $i_{\text{com}}$  is fixed,  $Q_0$  will be consistent for all operating conditions, which may be not ideal regarding the transient response and steady-state errors. In particular, in the ‘soft’ turn-off scenario, the  $dv/dt$  is determined by the load current amplitude. In light load conditions, the  $dv/dt$  is low, so the desired turn-off timing difference between the series-connected switches is relatively large [175]. Larger  $Q_0$  is preferred in this situation to obtain a faster transient response. However, in heavy load conditions, the  $dv/dt$  is high, so the desired turn-off timing difference between the series-connected switches becomes smaller. Then smaller  $Q_0$  is preferred in this situation to do the ‘fine-tuning’; otherwise, large steady-state errors may occur.

The proposed current source gate driver provides different levels of  $Q_0$  by tuning  $i_{\text{com}}$  discretely, so the adaptivity to different operating conditions is excellent. In the ‘soft’ turn-off scenario, higher levels of current mirrors are enabled to generate larger  $Q_0$  for lighter load conditions, and lower levels of current mirrors are enabled to generate smaller  $Q_0$  for heavier load conditions. In the ‘hard’ turn-off scenario, the  $dv/dt$  is determined by the gate current amplitude of the complementary turn-on switch rather than the load current amplitude [181]. Hence, lower levels of current mirrors (‘fine-tuning’) should be enabled for a more enormous turn-on gate current situation. The unit time step can be kept at the minimum interval  $\Delta t$  for the best tuning resolution.

Another possible solution for varying  $Q_0$  is to keep  $i_{\text{com}}$  fixed but adjust the unit time step  $\Delta t$  for different operating conditions. However, this solution has the same drawback as the voltage source gate driver, where the signal timing is the only control variable. To achieve the ‘fine-tuning’ for higher  $dv/dt$  scenarios, the minimum  $\Delta t$  needs to be set very small (below 1 ns), so the accuracy is easy

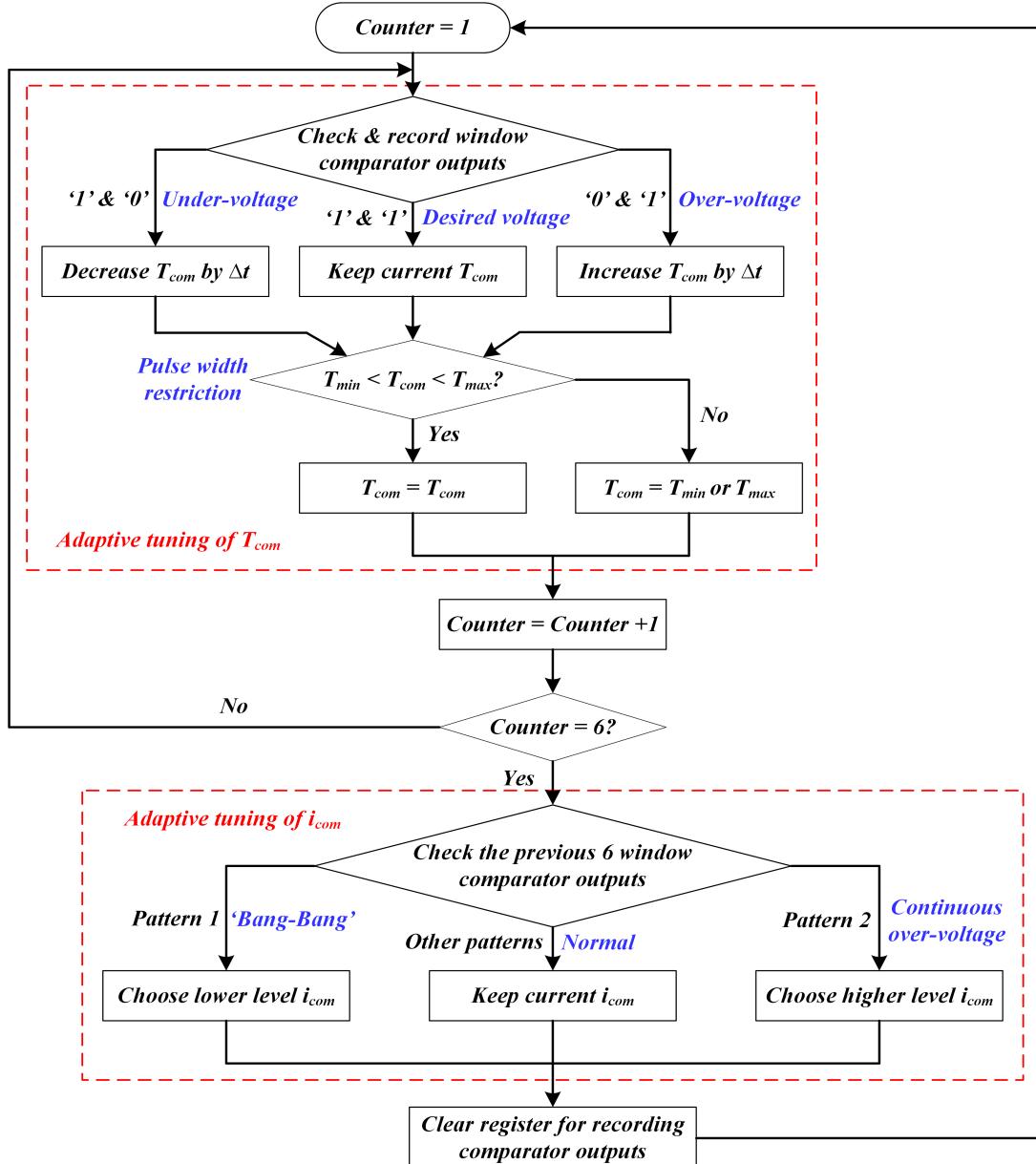
to be affected by signal jitters [72]. In this study, the controller minimum time step is selected to be 5 ns, which has much better immunity to signal jitters.

To sum, for the proposed current source gate driver, the compensation gate current pulse width ( $T_{\text{com}}$ ) is selected as the major control variable, while the compensation gate current amplitude ( $i_{\text{com}}$ ) is utilized to provide variable tuning resolutions for adapting to different operating conditions. The detailed control algorithm of  $T_{\text{com}}$  and  $i_{\text{com}}$  is introduced as follows.

The proposed top-level control algorithm is shown in Fig. 4.35. After the initialization, the load current direction needs to be known to determine the device turn-off scenario, which can be obtained from the load current sensor. If the load current direction is the same as the device junction capacitance charging/discharging direction, the device will experience ‘soft’ turn-off [shown in Fig. 4.28(a)]. Then the active gate current control is implemented at device turn-off transient, as shown in Fig. 4.30. If the load current direction is the opposite to the device junction capacitance charging/discharging direction, the device will experience ‘hard’ turn-off [shown in Fig. 4.28(b)]. Then the active gate current control is implemented at complementary device turn-on transient, as shown in Fig. 4.32. Once the switching scenario of the device is determined, the adaptive tuning of  $T_{\text{com}}$  and  $i_{\text{com}}$  should be executed next.

The proposed control algorithm for  $T_{\text{com}}$  and  $i_{\text{com}}$  is shown in Fig. 4.36. A counter is utilized to trigger the adaptive tuning of  $i_{\text{com}}$  after six control cycles for  $T_{\text{com}}$ . Within each control cycle of  $T_{\text{com}}$ , the window comparator outputs will be detected and recorded at first. The two outputs of the window comparator reflect the voltage sharing of the device during the steady off-state.

1) If the two outputs are ‘1’ & ‘0’, the device  $V_{\text{ds}}$  is below the desired range,



**Figure 4.36:** The Proposed Adaptive Control Algorithm for  $T_{com}$  and  $i_{com}$ .

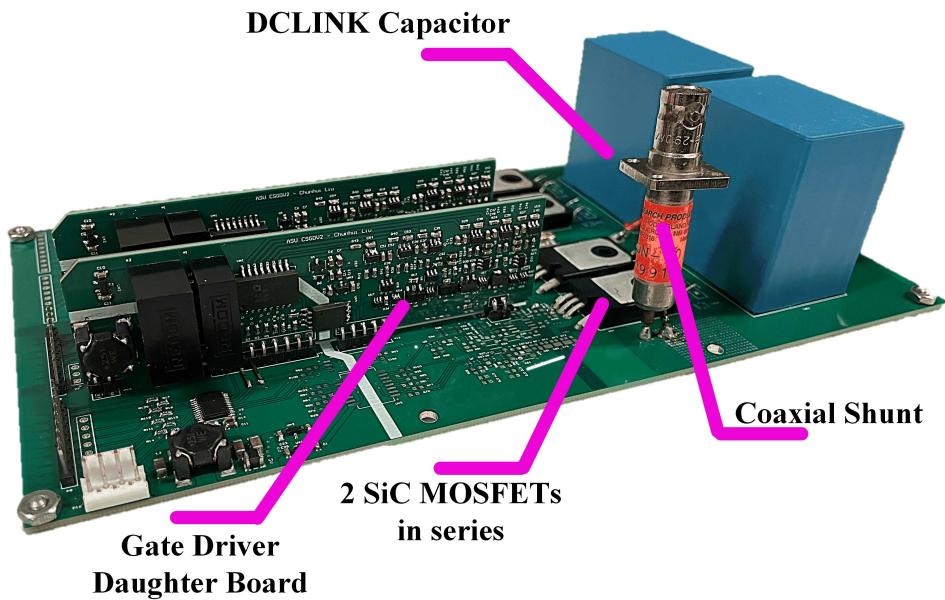
which indicates over-compensation. In the next control cycle,  $T_{\text{com}}$  should be decreased by a unit time step  $\Delta t$ .

2) If the two outputs are ‘0’ & ‘1’, the device  $V_{\text{ds}}$  is beyond the desired range, which indicates under-compensation. In the next control cycle,  $T_{\text{com}}$  should be increased by a unit time step  $\Delta t$ .

3) If the two outputs are ‘1’ & ‘1’, the device  $V_{\text{ds}}$  is within the desired range.

In the next control cycle,  $T_{\text{com}}$  should remain the current value.

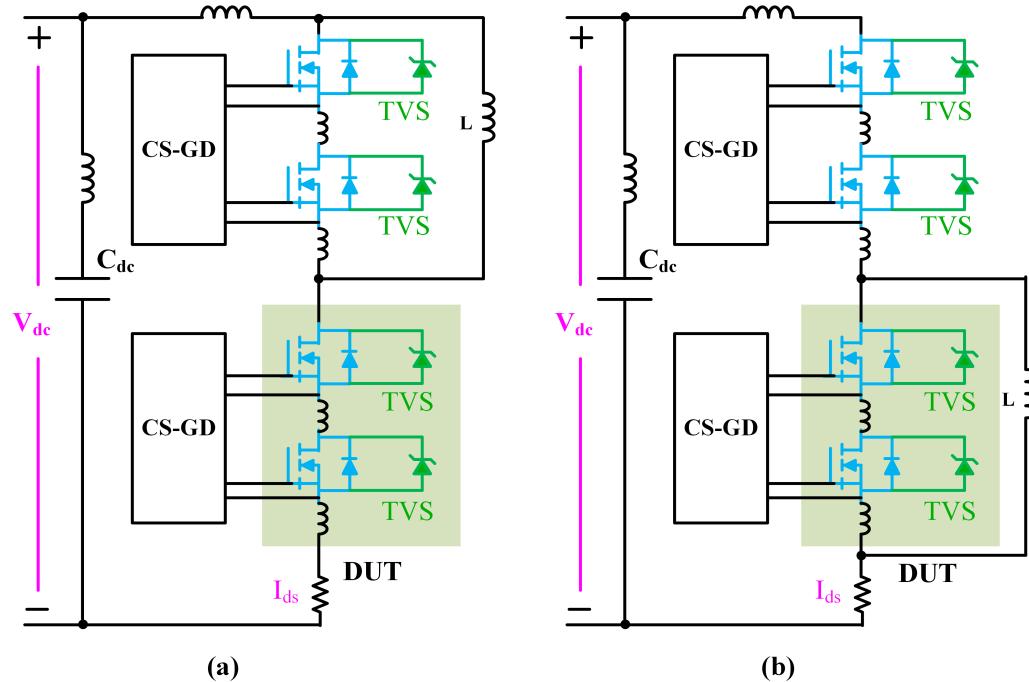
#### D. Experimental Verification



**Figure 4.37:** Prototype of the Series-connected SiC-based Multiple Pulse tester.

A series-connected SiC-based multiple pulse tester (MPT) prototype with the proposed closed-loop current source gate driver is designed and fabricated as shown in Fig. 4.37. The MPT is a half-bridge converter. Two series-connected SiC MOSFETs are employed for both the upper arm and the lower arm of the MPT. The schematic of the MPT is the same as the circuit shown in Fig. 4.28. The two upper arm

switches are labeled as S1 (top-sitting switch) and S2 (bottom-sitting switch), while the two lower arm switches are labeled as S3 (top-sitting switch) and S4 (bottom-sitting switch). Meanwhile, the lower arm switches are regarded as the device under test (DUT), and the lower arm device current is measured by T&M Research SDN-414 current shunt. When the soft turnoff scenario is investigated, an air-core inductor needs to be paralleled with the upper arm switches, as shown in Fig. 4.38(a), when the hard turn-off scenario is investigated, an air core inductor needs to be paralleled with the lower arm switches, as shown in Fig. 4.38(b). Although only two switches are connected in series for the prototype, the proposed gate driver and the adaptive voltage balancing scheme can be extended for more switches in series.



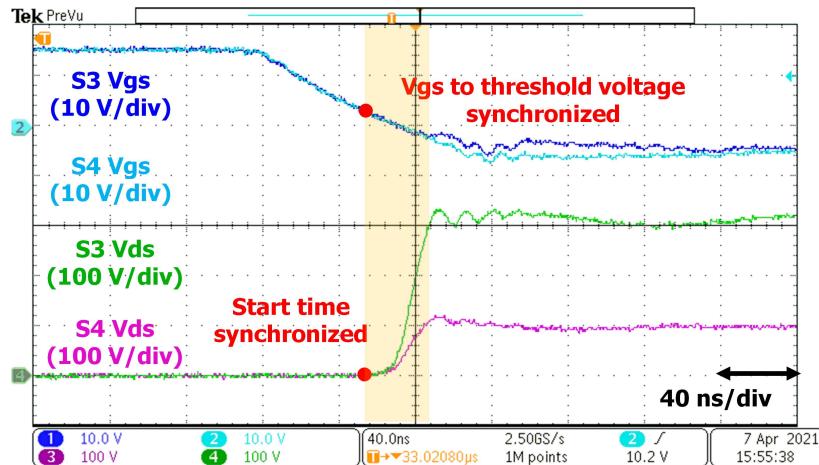
**Figure 4.38:** Test Setup for (a) Soft Turn-off Scenario (b) Hard Turn-off Scenario.

#### A. Voltage Balancing Scheme Verification in Soft Turn-off Scenario

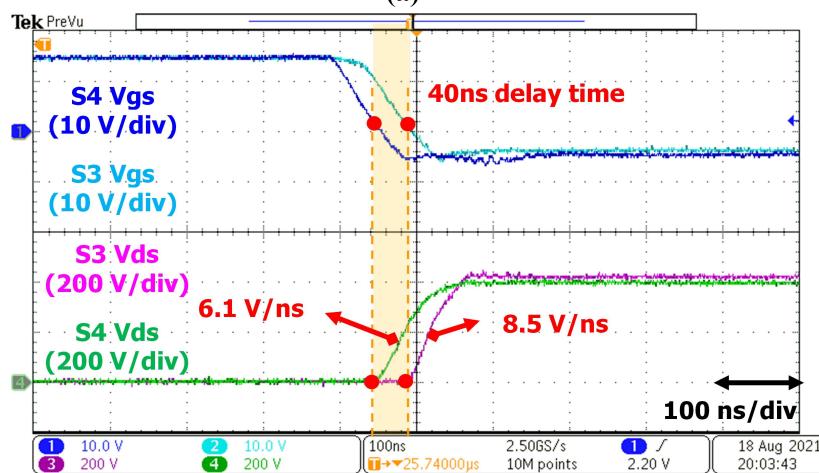
The waveforms for the lower arm switches (S3, S4) soft turn-off transient in 1 kV  $V_{dc}$  and 28 A load current condition are captured. As shown in Fig. 4.39(a), without

the active gate current control, S3 exhibits higher  $dv/dt$  than S4, which results in 50% over-voltage for S3 compared with the desired average value (400 V). It is clear that during most of the time in the  $dv/dt$  transient the gate-to-source voltages of the two switches already drop below the threshold. Therefore, the voltage sharing difference is caused by the variance in the drain current because of the contribution from the drain-to-ground displacement current (labeled as  $i_{p6}$  in Fig. 4.28). With the implementation of the active gate current control, the total turn-off gate current for S3 is reduced due to the compensation current, so the  $dv/dt$  starting timing of the S3 is delayed appropriately. Though the  $dv/dt$  of S3 is still higher than S4, the two switches can reach the steady state value at the same time because of the starting timing difference. As a result, the over-voltage for S3 is cut down to 2.7% compared with the desired average value, as shown in Fig. 4.39(b). The experimental result successfully validates the theoretical analysis in Fig. 4.30.

The experimental results for the soft turn-off scenario without and with the proposed closed-loop control are shown in Fig. 4.40. Meanwhile, the nominal breakdown voltage for the selected TVS diode is 600 V, which is used for the transient over-voltage protection of the main switch. When the closed-loop control is not implemented, as shown in Fig. 4.40(a), severe voltage imbalance occurs, and the drain-to-source voltage of the top-sitting switch (S3) is clamped by the TVS diode for every pulse. Due to the accumulated thermal stress, the leakage current of the TVS diode becomes larger with the emergence of more ‘over-voltage’ pulses. Therefore, the loss generated in the TVS diode will be considerable. If no active voltage balancing strategy is implemented, the TVS diode can be burned eventually. When the proposed closed-loop active gate current control is implemented, as shown in Fig. 4.40(b), the well-balanced voltage sharing is achieved, and the off-state drain-to-source voltage is very flat for all the pulses, which indicates that the TVS diode is not in the breakdown region (except



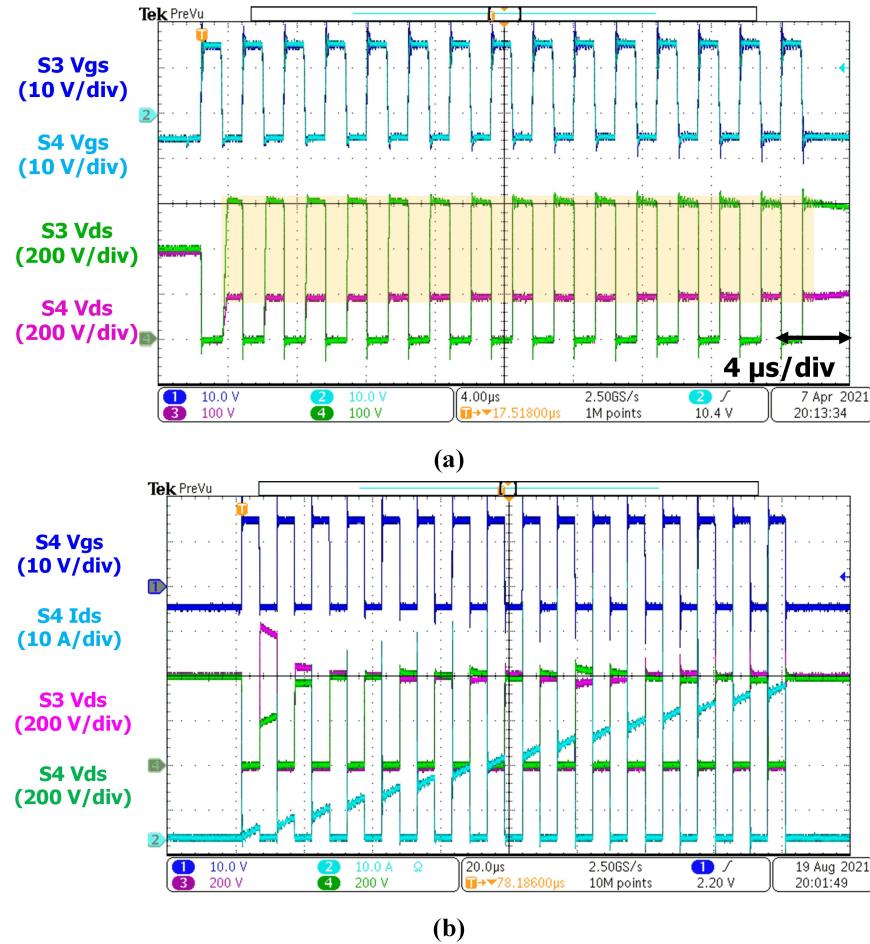
(a)



(b)

**Figure 4.39:** Waveforms for Lower Arm Switches Soft Turn-off (a) Without Compensation (b) With Compensation.

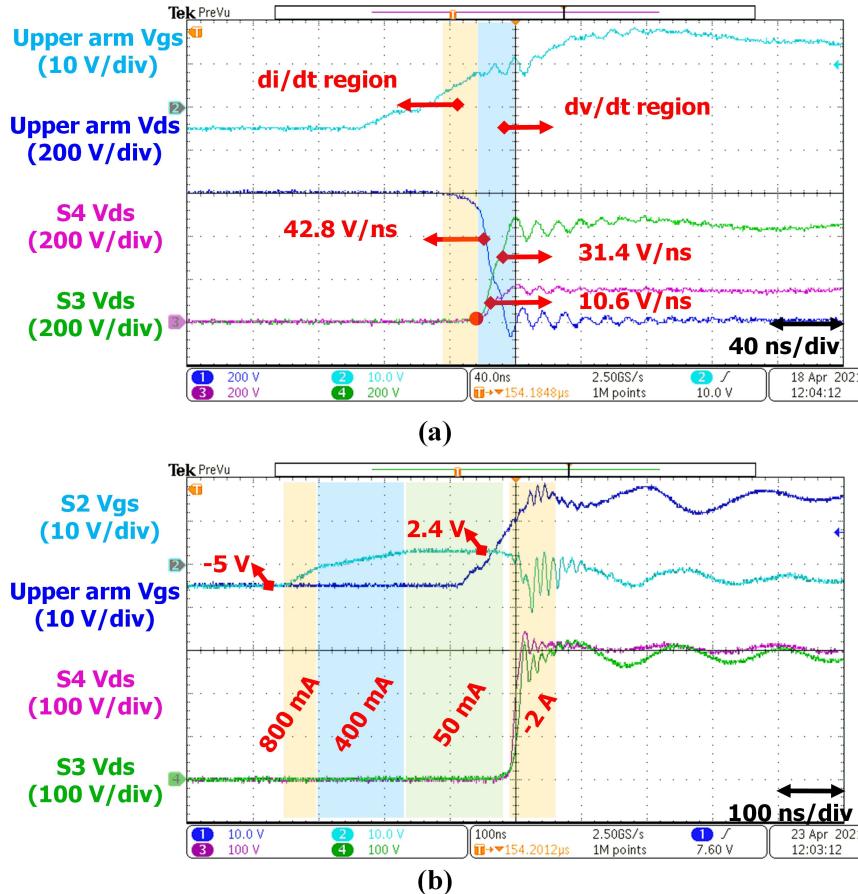
for the first pulse). Therefore, the leakage current in the TVS diode is minimal, and the loss generated in the TVS diode is insignificant.



**Figure 4.40:** Waveforms for Lower Arm Switches Soft Turn-off (a) Without Closed-loop Control (b) With Proposed Closed-loop Control.

### B. Voltage Balancing Scheme Verification in Hard Turn-off Scenario

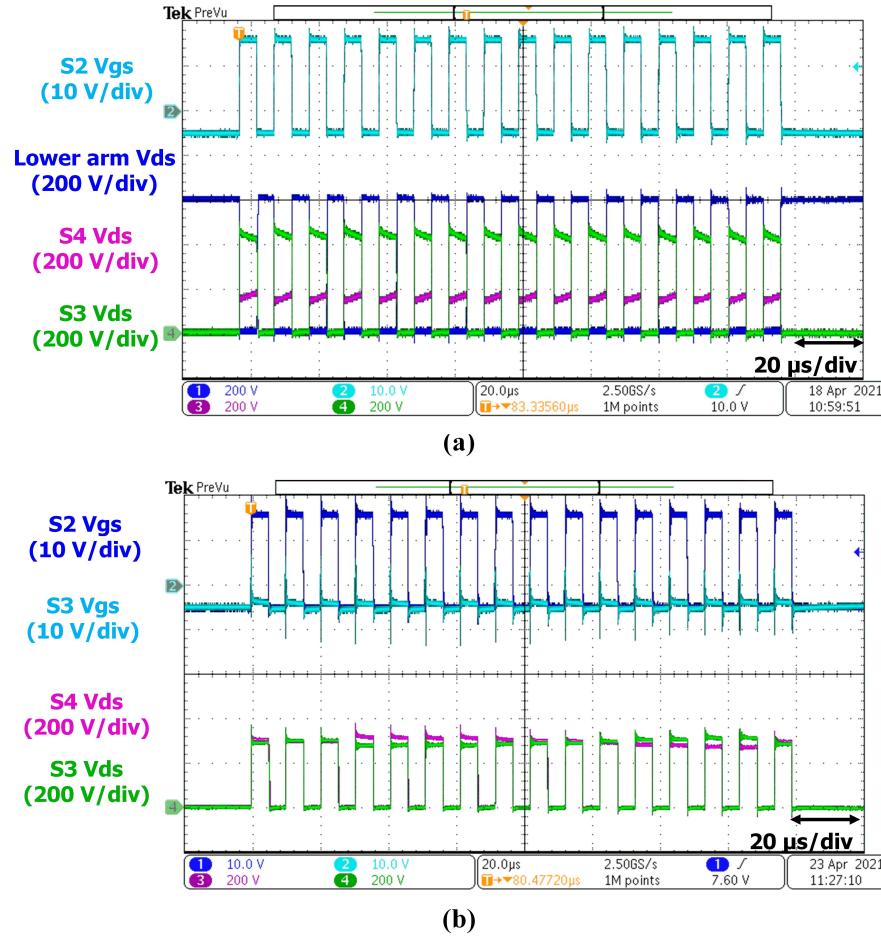
The testing circuit for the lower arm switches hard turn-off is the same as Fig. 4.38(b). When the upper arm switches ( $S_1, S_2$ ) are hard turned on, the drain-to-source voltages of the lower arm switches ( $S_3, S_4$ ) are forced to be pulled up and the voltage imbalance occurs, as shown in Fig. 4.41(a). It is clear that the gate-to-source voltage of  $S_3$  is far below the threshold when the  $dv/dt$  occurs, so the impedance of  $S_3$



**Figure 4.41:** Waveforms for Lower Arm Switches Hard Turn-off (a) Without Compensation (b) With Compensation.

is very high during this transient. The existence of the drain-to-ground displacement current will lead to the variance in the device drain currents, which results in voltage imbalance. In the operating condition of  $600\text{ V}_{dc}$  and  $21\text{ A}$  load current, the top-sitting switch S3 exhibits higher  $dv/dt$  than the bottom-sitting switch S4 does, which results in 48% over-voltage for S3 compared with the desired average value ( $300\text{ V}$ ). With the implementation of the active gate current control, the compensation current is actively injected into the gate of S3 to elevate its gate-to-source voltage closer to the threshold voltage when the  $dv/dt$  occurs. The large pre-charge gate current  $i_0$  is used to reduce the rise time for the gate-to-source voltage of S3, and the small

compensation gate current  $i_{\text{com}}$  is employed to achieve the fine-tuning. Right after the end of the compensation current pulse, the active negative voltage clamping is kicked in to safely turn off the gate of S3. In this way, the average  $dv/dt$  of S3 is decreased due to its reduced impedance. The over-voltage of S3 is cut down to 2.7% compared with the desired average value, as shown in Fig. 4.41(b). The experimental result successfully validates the theoretical analysis in Fig. 4.32.



**Figure 4.42:** Waveforms for Lower Arm Switches Soft Turn-off (a) Without Closed-loop Control (b) With Proposed Closed-loop Control.

To verify the proposed closed-loop control strategy in the hard turn-off scenario, the multiple pulse test is conducted under the 600 V dc-link condition. The frequency

of the continuous pulses is 200 kHz. The captured waveform for the open-loop case is shown in Fig. 4.42(a). When S1 is hard turned on, the lower arm switches (S3 and S4) are experiencing the hard turn-off. When the first switching event occurs, a severe voltage imbalance is observed. The top-sitting switch (S3) has higher drain-to-source voltage than the bottom-sitting switch (S4) does. The captured waveform for the closed-loop (with both  $T_{\text{com}}$  and  $i_{\text{com}}$  control) case is shown in Fig. 4.42(b). The adaptive tuning of the compensation gate current pulse width ( $T_{\text{com}}$ ) and amplitude ( $i_{\text{com}}$ ) are both implemented. Since the  $dv/dt$  is not determined by the load current in the hard turn-off scenario, the desired  $Q_{\text{com}}$  will not change rapidly with the load current. The control cycle of  $i_{\text{com}}$  is set to be six times the switching cycle in the hard turn-off scenario. The well-balanced voltage sharing is achieved for the entire load range (except for the first few pulses), which validates the proposed closed-loop control strategy in the hard turn-off scenario. To sum, the proposed closed-loop control strategy works well for both ‘soft’ turn-off and hard turn-off scenarios. Meanwhile, the TVS diode is only used to clamp the voltage for the first pulse, so the generated loss in the TVS diode is highly insignificant. The size and power rating of the TVS diode can be minimal as well.

#### 4.1.3 Conclusions

Firstly, an open-loop current source gate driver has been proposed to achieve highly synchronized gate voltage for series-connected SiC MOSFETs. This current source gate driver has better channel-to-channel gate voltage synchronization capability because of the constant gate current and novel gate driver structure. The constant gate current can provide several benefits in the aspect of  $V_{\text{gs}}$  synchronization: the immunity to gate loop difference, miller current compensation and  $V_{\text{gs}}$  linearity. The proposed CS-GD uses multi-winding transformer to equally split the pulse current,

and self-driving secondary circuit is invented to avoid any digital control signals from controller side. Thus, the control signals are all at grounded side. No signals' isolation barriers and isolated power supplies are needed which avoids propagation delay difference induced by signal transmission and different isolation level. Even though the gate driver signals are synchronous, the snubber circuits are still necessary because the  $V_{ds}$   $dv/dt$  may be different caused by different junction temperatures or parasitic capacitors. Due to the highly synchronized gate voltages, the snubber circuit can be designed smaller and only for power loop difference, system displacement current and device tolerance. The loss of proposed CS-GD is compared to the traditional VS-GD. Although the gate driving loss is bigger than that of VS-GD, the switching loss of series-connected string can be largely reduced by CS-GD high speed driving capability. The delay time among each device in the series-connected string will induce additional switching loss. The proposed concepts have been verified thoroughly by LTSPICE simulations and multi-pulse test experiment. A universal series-connected SiC MOSFETs block has been developed, and the switching characteristics of the block are evaluated. The  $V_{ds}$  voltage sharing challenge has been addressed using highly synchronized gate voltages with small snubber circuit.

However, in the WBG based applications, the closed-loop control should be achieved so that the snubber circuit can be eliminated. Therefore, a novel closed-loop current source gate driver is proposed for addressing the voltage imbalance issue in the series-connected SiC MOSFETs. The low-loss, low-cost, and fast-responded current mirror circuits are utilized to drive the SiC MOSFETs, which can actively counteract the voltage imbalance brought by the device-to-ground displacement currents. Meanwhile, the digital adaptive voltage balancing scheme is proposed and verified in both soft-switching and hard-switching scenarios. The multilevel current source gate driver provides different tuning resolutions, which improves the adaptivity to various

operating conditions. Moreover, without employing the snubber circuit and the extra Miller capacitor, the high-switching-speed and low-switching-energy benefits of using WBG devices are well reserved. A series-connected multiple pulse tester is built to validate the proposed closed-loop current source gate driver and the adaptive voltage balancing scheme. The experimental results coincide with the theoretical analysis pretty well for both soft-switching and hard-switching scenarios. With the implementation of the proposed approach, the over-voltage for the switch in the stack is cut down below 10% compared with the ideal average voltage under different load and different switching speed ( $dv/dt$ ) conditions.

In the course of further research, the proposed block will be further optimized in terms of efficiency improvement and size minimization. The comprehensive protection functions will also be developed for this current source gate driver.

## 4.2 A Comprehensive Short-Circuit Protection Scheme for Series-Connected SiC MOSFETs

For series-connected SiC MOSFETs, the protection functions can be directly borrowed except for the short circuit (SC) protection. Besides the SC protection for the entire string, there is a unique short circuit scenario, which is the SC of a single device among the series-connected string. Take the phase-leg configuration as an example, for the single device application, the short circuit of one device usually results in shoot-through of the phase leg when the complimentary switch turns on. This will cause severe overcurrent. Different from single device short circuit, the short circuit of one device among the series-connected string will not cause shoot-through of the phase leg. It is because the other devices in the series-connected string are still off to block the voltage. In this case, the drain-source voltage ( $V_{ds}$ ) of the short circuit device is zero, and the voltage across the other devices will increase, which may cause overvoltage failure of these devices. The transient voltage suppressor (TVS) is commonly implemented in parallel with each series-connected SiC MOSFETs to avoid overvoltage failure. Therefore, for the SC protection of series-connected SiC MOSFETs, it is necessary to monitor each device in the series-connected string. Not only the short circuit of the whole series-connected string but also the short circuit of a single device in the series-connected string should be considered.

In this chapter, a SC protection method for the series-connected SiC MOSFETs is proposed. In section 4.2.1, the shoot-through behavior is analyzed. Based on the phenomena, the evaluation metrics for SC protection is proposed. In section 4.2.2, a comprehensive SC analysis method is proposed to cover all the possible SC scenarios. By following the proposed method, the complete SC scenarios of series-connected SiC MOSFETs are analyzed. Section 4.2.3 presents the SC protection scheme to cover

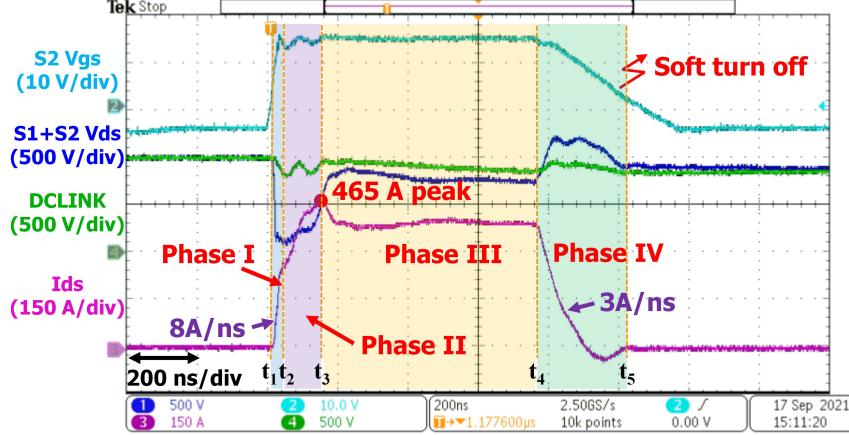
all the SC scenarios. In section 4.2.4, the design guideline of the protection circuit is demonstrated. The performance of the proposed SC protection method for each SC scenario will be evaluated in Section 4.2.5. Finally, Section 4.2.6 concludes the short-circuit protection of series-connected SiC MOSFETs.

#### 4.2.1 Shoot-through Behavior and Short-circuit Evaluation Metrics

If the whole series-connected string is regarded as a switch unit, the traditional short circuit tester of single device can be used [89, 94]. To understand the SC behavior of series-connected SiC MOSFETs, an unprotected nondestructive worst-case SC test (shoot-through) is conducted. The test results can provide more insights into the behavior of serial devices during a SC event and can aid in defining evaluation metrics of the short-circuit performance.

For simplicity, the discussions on SC behavior will focus on the device under test (DUT), which is S1-Sn connected in series. To focus the behavior analysis on DUT, the top switch unit UHigh is bypassed by a short copper-bar with low parasitic inductance. This configuration gives a total power-loop parasitic inductance around  $L_{\text{loop}} = 100nH$ . The SC gate-pulse duration on DUT is limited to  $1 \mu\text{s}$  to ensure its survival. The dc-link voltage is set to 1000 V and the junction temperature  $T_j$  is 25 °C.

Fig. 4.43 shows the typical waveforms of a shoot-through event. Similar to the short circuit of single device [89], there are four phases. Phase I ( $t_1-t_2$ ): the SiC MOSFET transits from the cut off region to the ohmic region when DUT is turned on, and stays at ohmic region. The  $I_{\text{ds}}$ , and thus  $dV_{\text{ds}}/dt$ , is determined by the parasitic inductance  $L_{\text{loop}}$ , transconductance of the SiC MOSFET, gate voltage ( $V_{\text{gs}}$ ), and dc-link voltage ( $V_{\text{dc}}$ ). Once  $V_{\text{gs}}$  reaches the device threshold voltage, the  $I_{\text{ds}}$  starts to rise rapidly due to the small power-loop inductance  $L_{\text{loop}}$ . The  $V_{\text{ds}}$  abruptly reduces



**Figure 4.43:** Typical Experimental Waveforms of Nondestructive Shoot-through Short-circuit Test.

to a lower value. Rough quantitative relation between  $V_{ds}$ , dc-link voltage  $V_{dc}$ , drain current  $I_{ds}$ , and power-loop inductance  $L_{loop}$ , is determined by 4.45.

$$V_{ds} = V_{dc} - L_{loop} + dI_{ds}/dt \quad (4.45)$$

Power loop is formed by  $C_{dc}$ , upper and lower switch units and dc bus bar. Power-loop inductance  $L_{loop}$  is determined by

$$L_{loop} = L_{dc,cap} + L_{dc,bus} + 2n \cdot L_{stray} \quad (4.46)$$

where  $L_{dc,cap}$ ,  $L_{dc,bus}$ , and  $L_{stray}$  are equivalent serial inductance (ESL) of the dc-link capacitor, parasitic inductance of the laminated dc bus bar, and device stray inductance, respectively, as denoted in Fig. 4.44. According to Fig. 4.43, the  $dI_{ds}/dt$  is around 8 A/ns.

Phase II ( $t_2-t_3$ ): At  $t_2$ , the SiC MOSFET starts to transit from the ohmic region to the saturation region, where the  $V_{ds}/I_{ds}$  ratio ( $R_{dson}$ ) is ramping up. Under saturation region (large  $V_{ds}$  and  $I_{ds}$ ), the velocity saturation of surface mobile carriers results in

relatively small high-field mobility, limiting the total carrier mobility. Thereby, the current in the saturation region is limited and the  $dI_{ds}/dt$  decreases [182, 183]. At  $t_3$ ,  $dI_{ds}/dt$  becomes zero and  $I_{ds}$  reaches its peak at 465 A, nearly 15.5 times of the rated current.

Phase III ( $t_3-t_4$ ): The device stays in the saturation region as  $V_{ds}$  is close to the dc-link voltage and  $I_{ds}$  remains high. The tremendous energy accumulated on the DUT has built a high junction temperature. High junction temperature significantly increases the scattering of phonon, reducing the low-field and high-field carrier mobility [182, 183]. Therefore, the  $R_{ds(on)}$  increases, which results in the  $I_{ds}$  drop from its peak. Following that current drop, the device is still exposed to high current, voltage, and junction temperature. As the junction temperature continues rising, the leakage current induced by thermally-assisted impact ionization becomes bigger [92]. At the late stage of Phase III, the decreasing rate of carrier mobility is comparable with the rising rate of leakage current. Thus, the  $I_{ds}$  keeps nearly constant. The device will probably fail under this condition, since the excessive SC energy  $E_{sc}$  will keep rising rapidly with time and cannot be dissipated in such a short time. As such, the turn-off action must kick in before the end of this phase to cut off the drain current. Therefore, a fault detection  $T_{det}$  and reaction time  $T_{reac}$  are pursued to be as short as possible to minimize the SC energy, and defined as one of the crucial parameters in SC protections.

Phase IV ( $t_4-t_5$ ): at  $t_4$ , the soft turn-off (STO) action is activated. According to (2), the negative  $dI_{ds}/dt \sim 3$  A/ns produces a 1.3 kV voltage spike of  $V_{ds}$ . The main concern during phase D should be safe SC protection, avoiding extreme transient oscillation and voltage overshoot. To enable the safe SC protection of the DUT at the nominal dc-link voltage, reducing  $L_{loop}$ , or slowing down the turn-off speed upon the faults, are possible solutions. Since  $L_{loop}$  always has a lower limit, a STO technique,

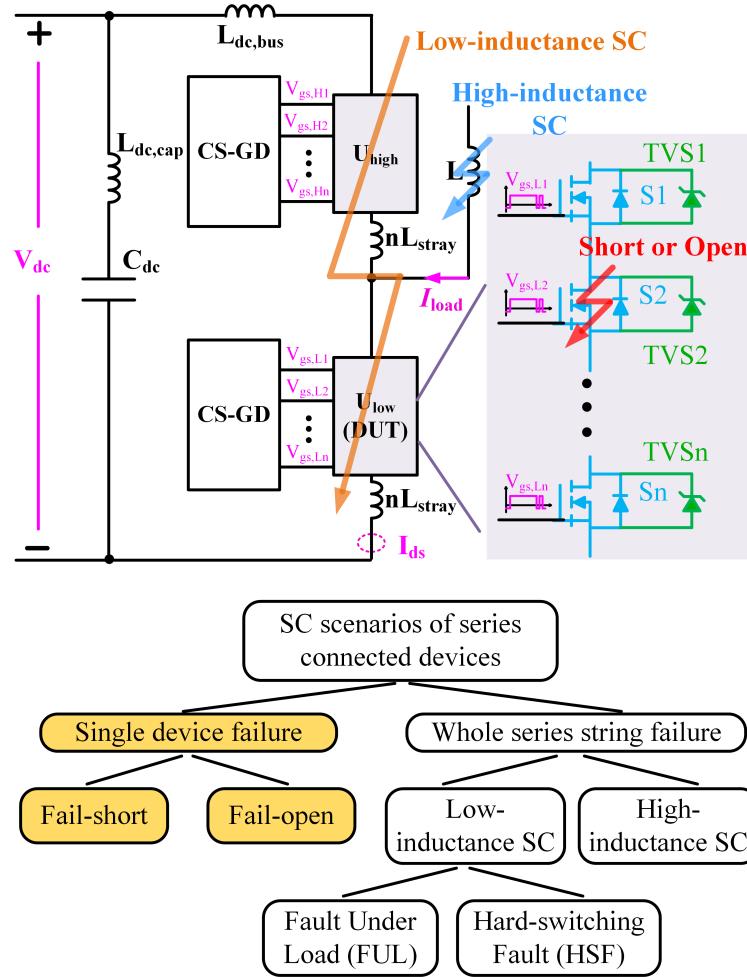
with reduced turn-off gate current, has been widely applied to gently cut off the SC current [95]. Particular attention should be devoted to the STO design because of the 15 times SC current. If the normal turn-off gate current is implemented, the  $dI_{ds}/dt$  will be very high and thus induces a large  $V_{ds}$  spike, threatening to destroy the device through an avalanche breakdown [184]. The apple-to-apple experiment comparison with and without soft turn-off will be demonstrated in the experiment section. Soft turn-off is employed only for SC current turn-off, not affecting the performance of the system under normal operating conditions.

According to the discussion on the SC behavior of series-connected SiC MOSFETs, the shoot-through leads to overcurrent, and its current peak is determined by the voltage applied to the dc loop parasitic inductance and the on-state impedance of the device. The critical evaluation metrics are summarized in Table 4.5.

**Table 4.5:** Short-circuit Protection Evaluation Metrics.

Evaluation Metrics	Description
<b>Time spent in SC</b> $T_{sc}$ [ns]	Time from start of SC to termination of SC current
<b>Detection time</b> $T_{det}$ [ns]	Time from start of SC trigger point to detection signal by FPGA
<b>Reaction time</b> $T_{reac}$ [ns]	Time from detection signal to soft turn-off starting point
<b>Dissipated Energy</b> $E_{sc}$ [mJ]	Total energy of SC. $E_{sc} = \int_0^{T_{sc}} V_{ds} \cdot I_{ds} dt$
<b>SC current peak</b> $I_{sc,pk}$ [A]	Maximum device current of SC
<b>SC voltage peak</b> $T_{reac}$ [ns]	Maximum device voltage of SC

#### 4.2.2 Short-circuit Scenarios of Series-connected SiC MOSFETs



**Figure 4.44:** Short-circuit Scenarios of Series-connected Devices In Half-bridge Configuration.

The failure of a SiC MOSFET can be short-circuit (fail-short) and open-circuit (fail-open)[90–92]. For applications where a single device serves as a switch unit, SC faults is widely investigated [89, 93, 94]. But the open-circuit of a switch unit is not widely discussed in previous literature. It is because the blocking voltage of a switch unit is higher than the maximum dc-link voltage. Thus, open-circuit failure of a switch unit can still block the dc-link voltage and will not induce any severe issues.

However, for the series-connected devices, the blocking voltage of a single device is smaller than the total dc-link voltage. Thus, the open-circuit of a single device in the serial string may cause overvoltage breakdown. Besides, the single device short-circuit will reduce the blocking voltage capability of the serial string, which may also cause overvoltage. Due to the much smaller overvoltage withstand time of the device, the overvoltage fault is hard to be protected. Therefore, the TVS diode is commonly implemented in parallel with each serial device to abruptly reduce the equivalent impedance of the device when overvoltage happens. Thus, the overvoltage is transferred to ‘short-circuit’ of the device. To sum, for applications where the series-connected devices are used as a switch unit, additional SC scenarios are the failures (fail-short and fail-open) of a single device among the serial string. Fail-open of a single device among the serial string can also cause short-circuit due to the parallel TVS diode.

As shown in Fig. 4.44, the stacking devices ( $n$  in series) serve as a switch unit, and two switch units ( $U_{\text{high}}$  and  $U_{\text{low}}$ ) form a half-bridge tester. Each serial device is protected from overvoltage by a parallel TVS diode. When the series-connected string is regarded as a switch unit, the traditional SC scenarios still exist and can be categorized into two types, namely, low-inductance SC (shoot-through) and high-inductance SC (load short) [89, 94]. Besides, fail-open and fail-short of a single device among the serial string may also cause overvoltage or overcurrent failure. In the following paragraphs, the SC of whole series-connected string and its SC characteristics are investigated firstly, then the unique single device failure scenarios are analyzed. The detailed analysis is as follows.

## A. Short Circuit of Whole Series-connected String

### 1. Low-inductance Short Circuit

A low-inductance SC event is induced when the conduction of both high-side and low-side switch units is overlapped in a phase-leg configuration. These fault types can be caused by failure of switches, incorrect control logic, driving-signal propagation errors, or other noise-related malfunctions [185]. The energy stored in the dc-link capacitor  $C_{dc}$  floods into the power devices by producing an inrush SC current through the dc-loop. Low  $L_{loop}$ , typically less than 100 nH, results in the abrupt rise of the SC current in a short time, usually within hundred nanoseconds. Upon low-inductance SC, a tremendous amount of accumulated energy on the power devices can escalate into a catastrophic failure if protective reactions fail to respond timely.

Depending on the failure timing, two possible scenarios of the low-inductance fault exist. Referring to the DUT in Fig. 4.44, when high-side switch  $U_{high}$  fails short at on-state, no abnormal phenomena occur at this state. But at next switching transient, the DUT  $U_{low}$  turns on and  $U_{high}$  cannot effectively turn off. Then, the shoot-through happens. This is so called ‘hard-switching fault’ (HSF) for  $U_{low}$ . When  $U_{high}$  fails short at off-state, the shoot-through occurs immediately because the DUT  $U_{low}$  is at on-state. This is so called ‘fault under load’ (FUL) for  $U_{low}$ .

## 2. High-inductance Short Circuit

A high-inductance SC event can be produced by incidents such as magnetic saturation of inductors or transformers, dielectric breakdown of motor windings, cable damage in construction accidents and different ground faults [185]. The SC inductance plays a significant role in determining the rising slope of the SC current. It varies from hundreds of nH to tens of mH depending on the severity and location of the faults. Even though this type of fault is less stressful to

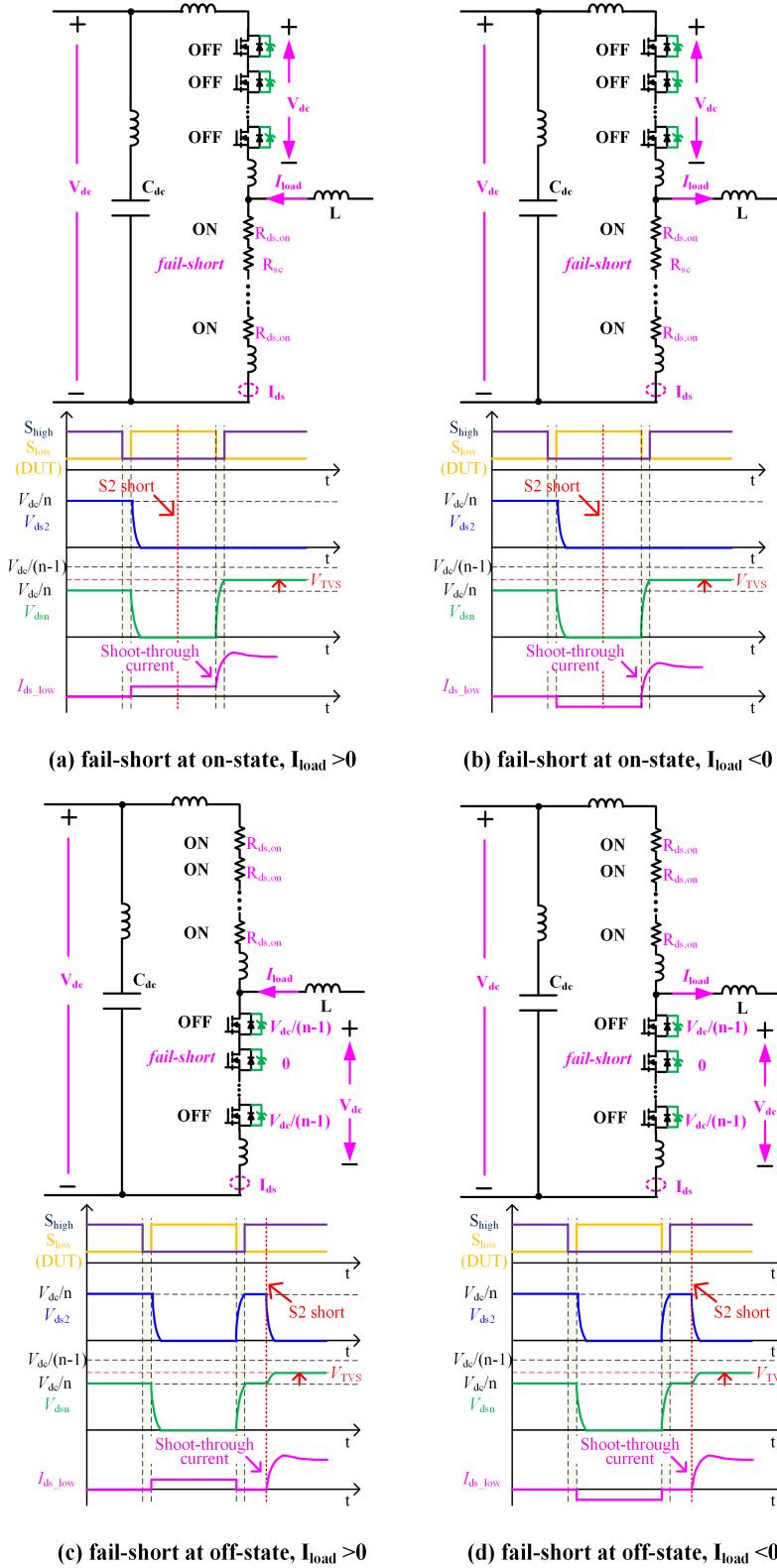
devices than the low-inductance SC, proper protection is still necessary to stop excessive currents and heat accumulation. This fault event is also referred to as overcurrent.

## B. Failure of A Single Device Among Series-connected String

The failure mode of SiC MOSFETs can be fail-short or fail-open [90–92], both of which may cause short-circuit of the phase-leg. Therefore, both cases should be discussed. The fail-open of a single device in the serial devices may also cause short-circuit because the TVS diode will work at the breakdown region with low impedance to protect the device from overvoltage. In the SC analysis, it is important to cover all the SC scenarios. In order not to neglect any SC scenario, a systematic analysis method is introduced in this section. The SC analysis method is derived from the device's state. There are three variables for a failure device: failure mode (fail-open or fail-short), failure timing (fail at on- or off-state) and device current direction. By following this analysis method, every possible scenario will be covered. And the protection method can be proposed based on the common phenomena of all the scenarios. Eight scenarios can be derived based on these three variables. The detailed analysis is as follows.

### 1. Single Device Fail-short:

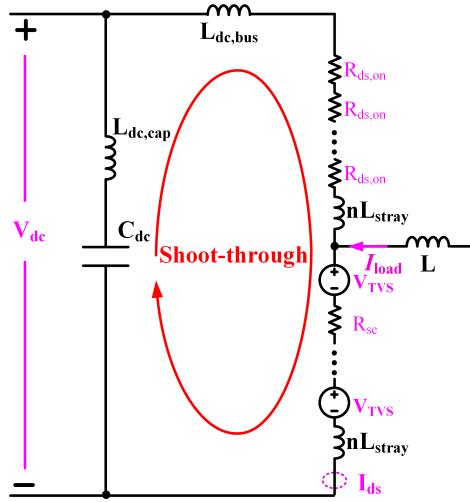
When a single device fails short, the  $V_{ds}$  of other serial devices increases from  $V_{dc}/n$  to  $V_{dc}/(n - 1)$ . If  $V_{dc}/(n - 1)$  is lower than the clamping voltage of the TVS diode  $V_{TVs}$ , the serial string can still block the dc-link voltage. Under this condition, the converter can still work correctly. But the reliability of the serial string is compromised since the  $V_{ds}$  of each device increases. Therefore, the SC protection scheme should detect this condition. If  $V_{dc}/(n - 1)$  is higher than



**Figure 4.45:** Typical Scenarios of Single Device Fail-short When  $V_{dc} > (n - 1)V_{TVS}$ .

the clamping voltage  $V_{\text{TVS}}$ , the analysis can be divided into four cases based on the failure timing and device current direction, as shown in Fig. 4.45.

### 1.1 Fail-short at on-state, $I_{\text{load}} > 0$



**Figure 4.46:** Equivalent Circuit of Single Device Fail-short Among Series-connected String When  $V_{\text{dc}} > (n - 1)V_{\text{TVS}}$ .

In Fig. 4.45(a), if SC of S2 happens during the on-state of the S1-S<sub>n</sub> serial string, there is not any difference from the normal device since short-circuit behaves the same as the device on-state. However, at next turn-off transition, the  $V_{\text{ds}}$  of other serial devices increases from  $V_{\text{dc}}/n$  to  $V_{\text{dc}}/(n - 1)$ . If  $V_{\text{dc}}/(n - 1)$  is higher than the clamping voltage, the TVS diode will clamp the  $V_{\text{ds}}$  of other serial devices at  $V_{\text{TVS}}$ , protecting them from overvoltage breakdown. The equivalent circuit and the typical waveforms are shown in Fig. 4.46. Under this condition, the  $I_{\text{ds}}$  increases since the difference of the dc-link voltage ( $V_{\text{dc}}$ ) and total TVS clamping voltage ( $(n - 1)V_{\text{TVS}}$ ) is applied to the dc-loop parasitic inductance. This current rising speed is much smaller than the traditional shoot-through, because the shoot-through voltage is much smaller than  $V_{\text{dc}}$ . From Fig. 4.46, the equivalent shoot-through voltage source is  $[V_{\text{dc}} - (n - 1)V_{\text{TVS}}]$ .

### 1.2 Fail-short at on-state, $I_{\text{load}} < 0$

If the load current changes direction, the phenomena are similar to case 1.1. The typical circuit and corresponding waveforms are shown in Fig. 4.45(b). Because the failure is shoot-through of phase-leg with a smaller voltage source, the direction of the load current has little impact.

### 1.3 Fail-short at off-state, $I_{\text{load}} > 0$

If the SC of S2 happens during the off-state of the serial string and the load current flows into the switch-node, the above mentioned abnormal phenomena will occur immediately, as shown in Fig. 4.45(c).

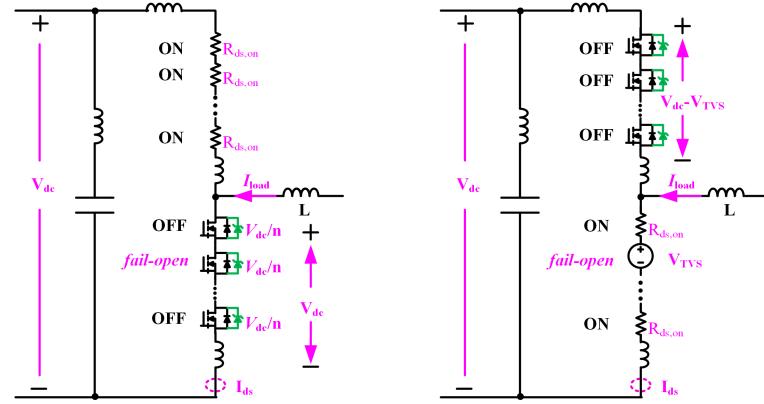
### 1.4 Fail-short at off-state, $I_{\text{load}} < 0$

If the SC of S2 happens during the off-state of the serial string and the load current flows out of the switch-node, the above mentioned abnormal phenomena will occur immediately, as shown in Fig. 4.45(d).

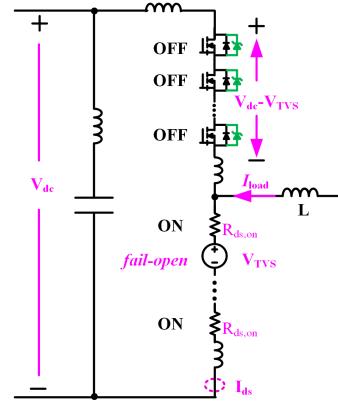
To sum, for the fail-short of a single device in the serial string, the maximum blocking voltage capability of the whole string is reduced from  $nV_{\text{TVS}}$  to  $(n - 1)V_{\text{TVS}}$ . If  $V_{\text{dc}} < (n - 1)V_{\text{TVS}}$ , the converter can still work properly. However, the reliability of the other normal devices is compromised, because the operating voltage of each device increases. If  $V_{\text{dc}} > (n - 1)V_{\text{TVS}}$ , the shoot-through overcurrent will occur with a smaller voltage source  $[V_{\text{dc}} - (n - 1)V_{\text{TVS}}]$ . The load current direction does not influence the fail-short phenomena because the shoot-through fault is at dc-loop.

## 2. Single Device Fail-open:

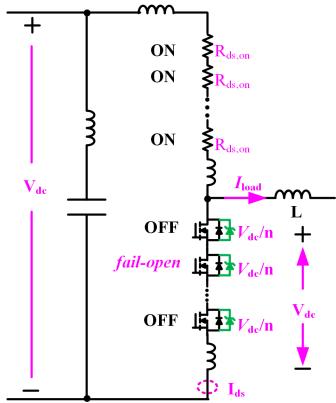
The open-circuit in single device applications will not cause any issue since the blocking voltage of a single device is bigger than the dc-link voltage. However,



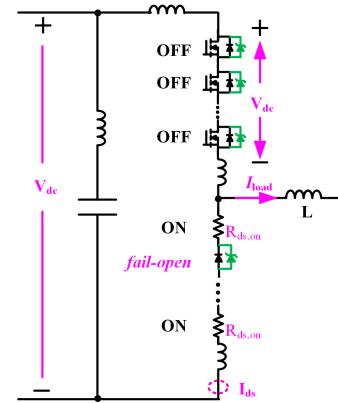
(a) fail-open at off-state,  $I_{load} > 0$



(b) fail-open at on-state,  $I_{load} > 0$



(c) fail-open at off-state,  $I_{load} < 0$



(d) fail-open at on-state,  $I_{load} < 0$

**Figure 4.47:** Typical Scenarios of Single Device Fail-open Among Series-connected String.

the blocking voltage of a single device in serial devices' application is smaller than dc-link voltage. Therefore, the fail-open of a single device in the serial devices' application can cause severe issues. As mentioned previously, the load current direction and the failure timing (failure at on-state or off-state) are two variables, which can form four cases. Each case is analyzed as follows.

### 2.1 Fail-open at off-state, $I_{\text{load}} > 0$

In Fig. 4.47(a), the load current is conducted by the on-state switch unit  $U_{\text{high}}$  before failure. If the open-circuit of S2 occurs during the off-state of the low-side string, no abnormal phenomena will be observed since the device in the off-state behaves the same as the open-circuit. However, at the next turn-on transition of the low-side string, the S2 is open-circuit while the other switches are on. At this time, although the complimentary switch unit ( $U_{\text{high}}$ ) is already turned off, the load current can be conducted by its body diode. Therefore, the S2 will be charged toward dc-link voltage when the low-side switch unit turns on. The TVS diode TVS2 clamps the  $V_{\text{ds}}$  of S2 at  $V_{\text{TVS}}$ , protecting S2 from overvoltage breakdown. The TVS2 and the other on-state devices form a low impedance path, making the load current commutate from the body diode of  $U_{\text{high}}$  to the low-side switch unit (TVS2-n $R_{\text{dson}}$ ). After that, the body diodes of  $U_{\text{high}}$  are reverse biased by ( $V_{\text{dc}} - V_{\text{TVS}}$ ). Under this condition, the overcurrent does not occur since  $U_{\text{high}}$  blocks the dc-link voltage. The equivalent circuit and the typical waveforms are shown in Fig. 4.47(a). The TVS diode conducts the load current with high clamping voltage during this fault event. Significant power loss is generated in the TVS diode, and thereby the protection circuit should detect this situation timely to avoid the subsequent failures of the converter.

### 2.2 Fail-open at on-state, $I_{\text{load}} > 0$

In Fig. 4.47(b), the load current is conducted by low-side string before failure. When S2 fails open-circuit at on-state, the load current charges the TVS diode of S2 to  $V_{\text{TVS}}$ . After that, the TVS diode becomes a voltage source with very low impedance. This TVS diode conducts the load current with high clamping voltage. No overcurrent phenomena occur during this fault event, because the high-side switch unit is always reverse-biased. The typical waveforms are shown in Fig. 4.47(b). Significant power loss is generated in the TVS diode, and thereby the protection circuit should detect this situation timely to avoid the subsequent failures of the converter.

### 2.3 Fail-open at off-state, $I_{\text{load}} < 0$

If the load current changes direction, which flows out of the switch-node, the phenomena will be different. Fig. 4.47(c) shows the typical waveforms. When the open-circuit of S2 occurs during the off-state of the low-side string, no abnormal phenomena will be observed since the device in the off-state behaves the same as the open-circuit. At the next turn-on transition of the low-side string, the complimentary switch unit  $U_{\text{high}}$  turns off first. After that, the load current is commutated by the body diode of  $U_{\text{low}}$ . Even though S2 fails open-circuit, its body diode and TVS diode conduct load current at the forward region. Therefore, the converter can still work properly.

### 2.4 Fail-open at on-state, $I_{\text{load}} > 0$

If the load current changes direction, which flows out of the switch-node, the phenomena will be similar to case 2.3. It is because the body diode or the TVS diode of S2 can continuously conduct the load current even though S2 fails open-circuit. In this case, the converter can still work properly. The typical waveforms are shown in Fig. 4.47(d).

In summary, for the single device fail-open fault, the load current direction determines the phenomena. When the load current flows from source to drain of DUT (synchronous rectification mode), the DUT can still work properly because the body diode or TVS diode can conduct load current. When the load current flows from drain to source of DUT, the fail-open device will be charged to TVS clamping voltage during on-state. The abnormal phenomena occur at on-state of the fail-open device regardless of the failure timing. The TVS diode conducts the load current with high clamping voltage, thus, the protection circuit should detect this situation timely to avoid subsequent failures.

In this section, all the possible short-circuit scenarios in serial devices' applications are discussed. Besides the traditional SC scenarios, the single device failure can also cause severe issues. Although the single device failure may not cause overcurrent, the reliability of the serial string can still be comprised. Specifically, for single device fail-short, the abnormal phenomena happen at gate-off state regardless of load current direction. For single device fail-open, the abnormal phenomena occur at gate-on state only when the load current flows from drain to source. When the load current from source to drain (synchronous rectification mode), the converter can still work properly. A SC protection scheme is proposed in the next section to cover the above-mentioned SC scenarios.

#### 4.2.3 Short-circuit Protection Scheme of Series-connected SiC MOSFETs

As mentioned in the introduction section, five SC fault indicators (temperature, dc-link voltage dip, drain-source current, gate charge, and  $V_{ds}$ ) can be compared in terms of sensitivity and response time. Because single device failure may not induce overcurrent, the drain-source current cannot be used as a fault indicator in

the applications of serial devices. As for the temperature, the response time is long because the fault can only be detected after the over-temperature already occurs. Moreover, the single device fail-short may not cause over-temperature if the blocking voltage of the serial string is still bigger than the dc-link voltage. The dc-link voltage dip is caused by the excessive current, thus, it cannot cover single device failure scenarios in the serial devices' application. Besides, the dc-link voltage dip is very sensitive to parasitics. The gate charge method is only effective when shoot-through failure happens. Thus, the only effective method is based on the gate voltage and  $V_{ds}$  voltage. Because the  $V_{ds}$  voltage is compared between dc-link voltage and the on-state voltage drop, the voltage difference from the normal operation is big. Moreover, the response time is short because the detection is based on the voltage signal. The existing DeSat protection scheme can safely terminate the overcurrent based short-circuit of the whole series-connected string. Basically, the DeSat circuit detects the  $V_{ds}$  at on-state and reports the fault once the  $V_{ds}$  is higher than the threshold. At off-state, the DeSat circuit is disabled. As for the failure of a single device in the serial string, the  $V_{ds}$  monitoring circuit should be active at both on-state and off-state to cover the unique fault scenarios of serial devices. Therefore, the proposed protection scheme combines the gate on/off logic and the  $V_{ds}$  feedback signal. In this way, all the SC scenarios can be detected. Unlike the traditional DeSat protection for single device applications, where the STO signal can be generated locally at the secondary side, the SC fault signal for the series-connected devices should be feeded back to the primary side (controller). It is because each device in the serial string should take synchronous action. Otherwise, severe voltage unbalance would occur, putting the device in danger of overvoltage breakdown. Therefore, for applications of series-connected devices, the  $V_{ds}$  signal of each device should be transmitted to the controller side. Once the controller receives the fault signal of any device, the soft turn-off signal

should be sent to all the series-connected devices. Therefore, synchronization can be guaranteed even at SC conditions. The detection circuit will be explained first in the following paragraphs, and the protection scheme based on this detection circuit will be elaborated for each SC scenario.

**Table 4.6:** Short-circuit Scenarios and Corresponding Protection Signals.

Operation condition		Gate signal	SC detection signal $S_d$
<b>Normal operation</b>	on	1	0
	off	0	1
	on to off transient	0	0
	off to on transient	1	1
<b>Single device failure</b>	fail-short	0	0
	fail-open	1	1
<b>SC of whole serial string</b>	low-inductance SC	FUL	1
		HSF	1
	high-inductance SC	-	1

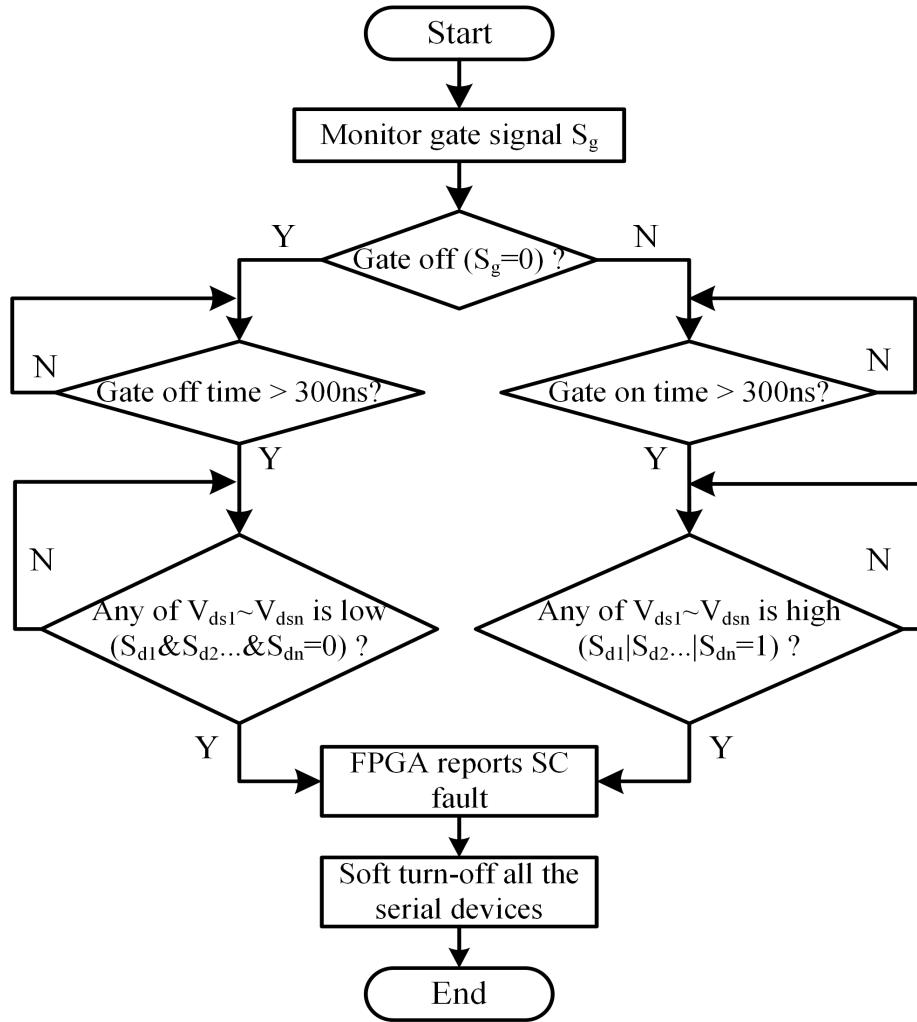
### A. Protection Schemes for Every Scenario

All the SC scenarios of series-connected devices have been summarized in Table 4.6, and the protection scheme should differentiate between the SC event and the normal operations. From Table 4.6, it is easy to conclude that the gate signal and detection circuit feedback signal can be combined to achieve the detection scheme. For example,

if the device is on under normal operations, the gate signal will be ‘1’ (high state), and the detection feedback signal will be ‘0’ (low state). If the device is off, the gate signal will be ‘0’, and the detection feedback will be ‘1’. The gate signal and feedback signal are opposite under normal operating conditions. The logic combination of each SC event has been included in Table 4.6. In all short-circuit scenarios, the gate and feedback signals are identical ('00' or '11'). Thus, the normal operation and SC condition can be differentiated by combining the gate signal and the  $V_{ds}$  feedback signal. It should be noted that in the on/off transients, the logic combination can also be '11' and '00', which may mis-trigger the SC protection. Therefore, the on/off transients are blocked by the controller. A blank time at the on/off gate signal transient is introduced to avoid the mis-trigger of the SC protection. This blank time is composed of the analog blank time and the digital blank time, which will be illustrated in detail in the next section.

After the SC fault is detected, the STO will be implemented. In this research, the current source gate driver in 4.1.2 is used. The gate driver can output a multi-level gate current and has a fast dynamic response, which is proven to have several benefits in series-connected devices. The STO is very convenient to be implemented by this current source gate driver without any additional components. A small turn-off current pulse is applied to the gate after the SC protection is activated. The control algorithm of the controller is present in Fig. 4.48.

It should be noted that once the protection circuit of any device detects the fault in the series-connected string, the STO should be implemented for all the single devices in the serial string. Otherwise, the turn-off action will be unsynchronized, and the overvoltage may occur. Unlike traditional DeSat protection, where the STO is implemented locally at the secondary side, the STO signal of series-connected devices should be generated from the controller side and transmitted to every the serial device



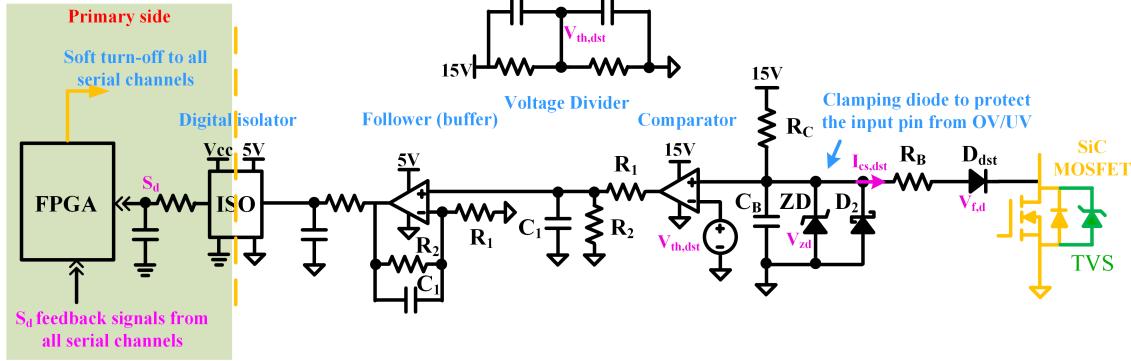
**Figure 4.48:** Flow Chart of Proposed Protection Scheme.

simultaneously.

## B. Detection Mechanism

The detection circuit is modified on the basis of DeSat circuit, as shown in Fig. 4.49. The  $V_{dst}$  is the input of the comparator, which is determined by the  $V_{ds}$  of the device. The comparator will generate a  $V_{ds}$  feedback signal according to the relationship between  $V_{dst}$  and the threshold voltage  $V_{dst,th}$ .

During the on state,  $I_{cs,dst}$  forward-biases D<sub>dst</sub> and the  $V_{ds}$  is low. Thus, the  $V_{dst}$



**Figure 4.49:** Schematic of Proposed Short-circuit Detection.

is clamped by the low  $V_{ds}$ , which is lower than  $V_{th,dst}$ . The feedback signal  $S_d$  keeps low. When an overcurrent SC occurs, the  $V_{ds}$  increases with the  $I_{ds}$ . In the meantime,  $V_{dst}$  will rise with  $V_{ds}$ . Once the current reaches the preset overcurrent threshold,  $V_{dst}$  will be charged higher than  $V_{th,dst}$ , and the feedback signal  $S_d$  will go high.

During the off state of the device, the diode  $D_{dst}$  blocks the high  $V_{ds}$ . Different from the DeSat, the detection function is not disabled with internal current source [25], because the  $V_{ds}$  feedback is also needed at off state to detect the fail-short of a single device among the series-connected devices. The  $V_{dst}$  will be charged to the clamping voltage  $V_{zd}$  of the zener diode by  $V_{cc}$  through the  $RC$  circuit. The  $V_{dst}$  is bigger than the threshold voltage  $V_{th,dst}$  and the comparator will output high state. Thus, under normal operation condition, the off state of the device result in the high state of the feedback signal  $S_d$ . However, if the device short-circuit happens, the  $V_{dst}$  will be clamped by the  $V_{ds}$  of the short circuit device through  $D_{dst}$ . Thus, the  $S_d$  will become low.

#### 4.2.4 Short-circuit Protection Circuit Design Guideline

The circuit design guideline includes detection circuit design, TVS diode selection, and STO gate current design. The design guideline will be based on the general

device's parameters so that it can be applicable to different devices.

### A. Detection Circuit

First, the threshold voltage ( $V_{\text{th,dst}}$ ) should be determined based on overcurrent SC scenarios. The lower threshold voltage result in shorter protection response time, which is preferred. But if the threshold voltage is too low, the protection may be mis-triggered. Thus, the threshold voltage is designed based on the maximum drain-source current under normal operation with a reasonable margin. For the unique fault scenario in serial devices applications, the threshold voltage is not an issue because the comparison difference of normal case and fault case is big, between on-state  $V_{\text{ds}}$  (10 V) and off-state  $V_{\text{ds}}$  (dc-link voltage level). The threshold voltage is configured according to the output characteristic of the device at the highest operation junction temperature (175 °C) because of the heavily temperature-dependent  $R_{\text{ds,son}}$  of SiC MOSFETs. Otherwise, fault protection is easily triggered if  $V_{\text{th,dst}}$  is set based on the ambient temperature while the operating junction temperature is high. The designed trigger-point current  $I_{\text{d,dst}}$  is set to be 40 A, which is determined as a doubled value of the rating current at 175 °C. According to the datasheet of the used SiC MOSFETs (C3M0075120K from Wolfspeed),  $I_{\text{d,dst}} = 40A$  at 175 °C corresponds to a 5.5 V drain-source voltage drop.

$$V_{\text{ds,dst}} = R_{\text{ds,son}} I_{\text{d,dst}} = 5.5V \quad (4.47)$$

where  $V_{\text{ds,dst}}$  is the device drain-source voltage drop at 175 °C, 40 A condition. Considering the voltage drops across  $D_{\text{dst}}$  and  $R_B$ ,  $V_{\text{th,dst}}$  is calculated as 7 V according to

$$V_{\text{th,dst}} = V_{\text{ds,dst}} + V_{\text{f,d}} + R_B \cdot I_{\text{cs,dst}} \quad (4.48)$$

where  $V_{f,d}$  is the forward voltage drop of the diode  $D_{dst}$ ;  $I_{cs,dst}$  is the current flow through  $D_{dst}$  when the device is on. The  $I_{cs,dst}$  can be calculated by (5).

$$I_{cs,dst} = (V_{cc} - V_{f,d} - V_{ds}) / (R_C + R_B) \quad (4.49)$$

since the  $I_{cs,dst}$  is around 5 mA, the diode's forward voltage drop will be  $V_{f,d} = 0.5V$  according to the diode datasheet. Second,  $D_{dst}$  is required to feature fast reverse-recovery and low junction capacitance  $C_{dst,j}$  to minimize the induced noise susceptibility of the detection circuit caused by the fast  $dV_{ds}/dt$ , according to

$$i_{dst,dvdt} = C_{dst,j} \cdot dV_{ds}/dt \quad (4.50)$$

The selected diode  $D_{dst}$  is US1M from Taiwan Semiconductor. The diode's low junction capacitance  $C_{dst,j,100V} < 2pF$  minimizes  $i_{dst,dvdt}$ , and thus, reduces detection circuit noise susceptibility. Lastly, the blank time design. In this circuit, the blank time consists of analog blank time and digital blank time. The analog blank time is achieved by the  $C_B$ ,  $R_C$  in Fig. 4.49. The digital blank time is achieved by the controller. The blank time ensures no nuisance tripping occurs during the on/off switching transient process until  $V_{ds}$  settles down. Therefore, the blank time is designed according to dynamic characterization experiments to avoid the spurious trip. The analog blank time is chosen to filter the high-frequency noises generated by the switching transient. The digital blank time is used to tune the total blank time per different operating conditions conveniently. The total blank time should be as small as possible since the SCWT of the device is relatively low. Basically, the design of the blank time is a trade-off between blocking transient states and short-circuit response time. The 300 ns blank time is large enough in this case, since the switching transient

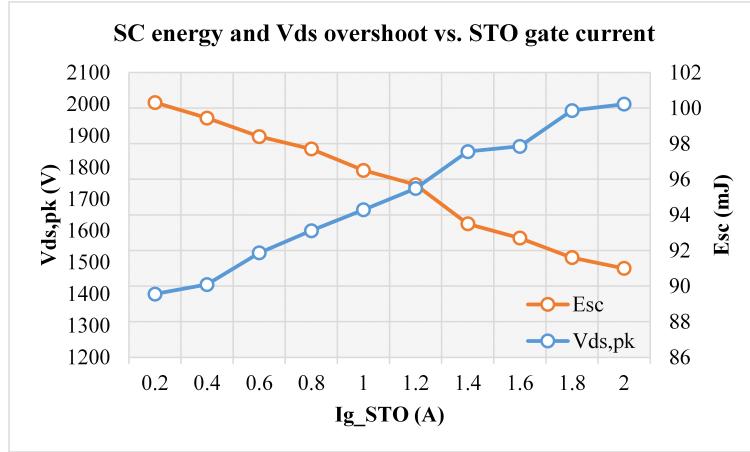
only takes smaller than 100 ns. The 300 ns is much shorter than the short-circuit withstand time (typical around 2  $\mu$ s). As a result,  $C_B = 100\text{pF}$  and  $R_C = 600\Omega$  are selected. According to 4.51,

$$t_{\text{blk,analog}} = \int_0^{V_{\text{th,dst}}} \frac{R_C \cdot C_B}{V_{\text{cc}} - V_{\text{CB}}} dV_{\text{CB}} \quad (4.51)$$

analog blank time  $t_{\text{blk,analog}} = 30\text{ns}$  is added to the digital blank time of 270 ns. The propagation delay time of the conditioning circuit is composed of the RC circuit and the delay time of the  $I_{\text{Cs}}$ , a total propagation delay of 60 ns after the comparator. With the detection circuit free of false-triggering in normal operation, SC assessment tests are then conducted.

## B. TVS Diode Selection

Even though the closed-loop voltage balancing methods can achieve  $V_{\text{ds}}$  voltage balancing, the  $V_{\text{ds}}$  voltage is still unbalanced during transients and start-up of the closed-loop control. Besides, the TVS diode can be used to protect the device from overvoltage, because the overvoltage of the device will be transformed to overcurrent (short-circuit). Thus, the SC protection method can protect the device. Therefore, the TVS diode for the series-connected SiC MOSFETs is necessary to protect the serial devices from overvoltage. The TVS operates by shunting excess current when the induced voltage exceeds the avalanche breakdown potential. For the single device application, the selection can be based on several parameters, such the breakdown voltage  $V_{\text{BR}}$ , clamping voltage  $V_{\text{clamp}}$ , surge current  $I_{\text{pp}}$ , etc. [186]. As for the series-connected devices, the clamping voltage is usually high ( $> 1 \text{kV}$ ). The TVS diodes can be directly series-connected to achieve higher breakdown voltage.



**Figure 4.50:** Short-Circuit Energy and Voltage Overshoot at Different STO Gate Currents.

### C. Soft Turn Off Gate Current Design

The STO gate current is determined based on the HSF test results, as shown in Fig. 4.50. The reason to choose HSF as the design reference of STO gate current is that the HSF is usually the worst-case of SC scenarios. Since the STO gate current is low, there is a delay time from the starting point of the  $V_{gs}$  falling edge to the starting point of the  $V_{ds}$  rising edge. This delay time is added to the total response time of the SC protection. Thus, more SC energy would be generated if the delay time were longer. However, if the STO gate current is high, the  $V_{ds}$  overshoots will be enormous. Therefore, the STO gate current is a trade-off between voltage overshoots and the SC dissipated energy  $E_{sc}$ . As shown in Fig. 4.50, when the STO gate current varies from 0.2 A to 2 A, the SC energy dissipation reduces from 100.3 mJ to 91 mJ while the overshoot of  $V_{ds}$  increases from 1.4 kV to 2 kV.

### D. Reliability Discussions

The design parameters of the proposed protection scheme are the threshold voltage and the blank time. In the following discussion, these two design parameters will

be analyzed in terms of false positives and false negatives. After that, the circuit components design consideration for these two parameters will be illustrated in terms of reliability. Since the proposed method will cover both traditional overcurrent fault and unique fault in series-connected devices, the design of these two parameters will be discussed in these two kind of fault conditions.

1. Threshold voltage ( $V_{\text{th,dst}}$ ).

### 1.1 Traditional fault scenarios

For traditional fault scenarios, the proposed fault detection scheme is based on the  $V_{\text{ds}}$  feedback signal at on-state. When the  $V_{\text{ds}}$  is higher than the threshold voltage at on-state, the overcurrent occurs and the on-state  $V_{\text{ds}}$  voltage drop is high. In this case, the threshold voltage should be bigger than the maximum on-state  $V_{\text{ds}}$  voltage drop at normal operating conditions. Otherwise, the lower threshold voltage may cause false positive issue (mis-trigger) in the condition of high normal on-state voltage drop. Therefore, the lower limit of the threshold voltage should be the maximum on-state voltage drop of normal operating conditions with some margin. As for the upper limit of the threshold voltage, the voltage drop in any possible overcurrent fault scenarios should be bigger than the threshold voltage. Otherwise, the overcurrent fault may not be detected, which is false negative issue.

### 1.2 Unique fault scenarios of series-connected devices

For the unique fault scenarios, the fault detection scheme is based on gate signal and  $V_{\text{ds}}$  feedback signal. If the  $V_{\text{ds}}$  feedback signal is high at gate on-state or low at gate off-state, this device is regarded as fault device. The  $V_{\text{ds}}$  normal off state voltage is  $V_{\text{dclink}}/N$ . Compared to the fail-short device (gate off-state voltage is nearly zero), the voltage difference is very big. Similarly, the  $V_{\text{ds}}$

normal on-state voltage drop is nearly zero. Compared to the fail-open device (gate on-state  $V_{ds}$  is dc-link voltage level), the voltage difference from normal device and fault device is large. Therefore, the false positive issue is less likely to happen if the threshold is bigger. In the unique case, the false negative issue is less likely to happen because the voltage difference between normal condition and fault condition is very large (dclink voltage level).

## 2. Blank time (tblk).

The blank time of traditional overcurrent scenarios is widely discussed in the previous literature. This blank time is to avoid the transition period of gate signal and  $V_{ds}$  feedback signal in the on/off transient states. By reducing the blank time, the protection response time can be decreased. However, if the blank time is too small, the false positives may occur.

## 3. Components design consideration

The components design has influence on the noise immunity of the protection circuit. For instance, when the  $dv/dt$  induced ringing is high, the fault logic signal may be generated at the output of the DeSat comparator or the output of the digital isolator. Therefore, the false positives or the false negatives may occur due to the logic error. What we do in the circuit design is to reduce noise coupling and filter out the high frequency distortions.

### 3.1 Noise coupling reduction

The noise coupling reduction is done by selecting a blocking diode Ddst with low junction capacitance. The junction capacitance of this diode generates high frequency current because of the dc loop resonance. This high frequency current distorts the DeSat loop, so the DeSat loop parasitic loop inductance should also

be minimized by the optimal layout. Besides the blocking diode Ddst selection, the comparator should be selected with high noise rejection capability.

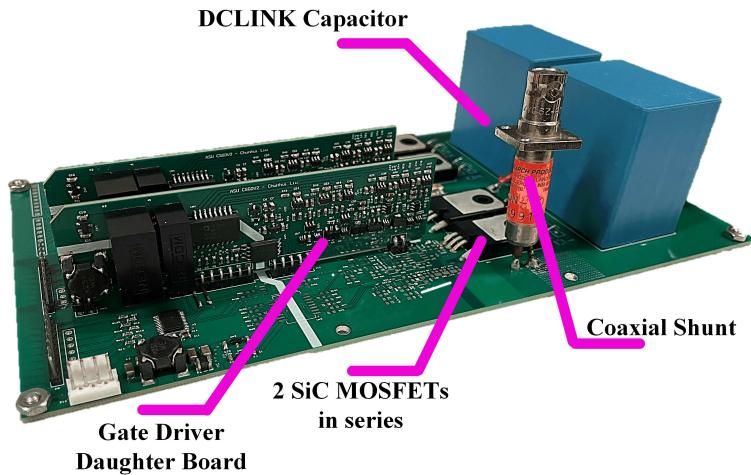
### 3.2 Filter out the high frequency distortions

The RC circuit is designed to increase the analog blank time as well as to filter out the high frequency distortions.

#### 4.2.5 Experimental Results

In this section, the test setup for short-circuit protection is explained firstly. After that, the SC protection performance for each SC scenario is validated and evaluated according to the evaluation metrics.

#### A. Test Setup



**Figure 4.51:** Short-circuit Test Bench.

The assembled experimental setup is presented in Fig. 4.51. The device under assessment is two series-connected 1.2 kV/30 A SiC MOSFETs C3M007512K from Wolfspeed [187]. The developed multi-level current source gate driver for the series-connected SiC MOSFETs has been elaborated in section 4.1.2. The dc-bus voltage is

regulated by a 2 kV DC power supply. A PCB half-bridge with 100 nH dc loop stray inductance has been developed. The dc-link capacitors are 20  $\mu$ F/1.1 kV B32776 from TDK. A series of ceramic capacitors are used as decoupling capacitors, which are placed close to the half-bridge to further minimize the power-loop parasitic inductance. When a SC occurs, the fault current is shared by the decoupling capacitors  $C_{dec}$  and the dc-link capacitors  $C_{dc}$  according to their impedance ratio as a function of the SC current frequency. More decoupling capacitors result in a faster current rise. To emulate the worst possible case, a sufficient total decoupling capacitance of 1  $\mu$ F is placed. A 50  $\mu$ H air-core inductor is used to evaluate the high-inductance SC faults. All the tests will be conducted under 1 kV dc-link voltage.

All measurements on the gate driver, such as  $V_{gs}$ , comparator output and other signals from FPGA, are measured with low voltage differential probes (P5205A). Drain current  $I_{ds}$  in SC is measured with a commercial coaxial shunt SDN series from T&M Research Products to obtain full current waveform during an SC with high bandwidth (400MHz).  $V_{ds}$  voltages across devices are measured with high-voltage differential probes (THDP0200).

## B. Short Circuit Test for Each Scenario

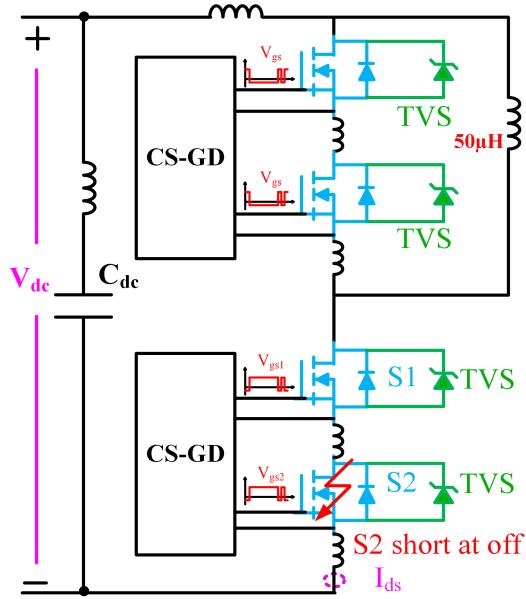
As discussed in the previous section, the SC scenarios of the series-connected SiC MOSFETs can be divided into single device failure (fail-short or fail-open) and short-circuit of the whole switch unit (traditional SC scenarios).

### 1. Single Device Failure

#### 1.1 Single Device Short Circuit at Off-state

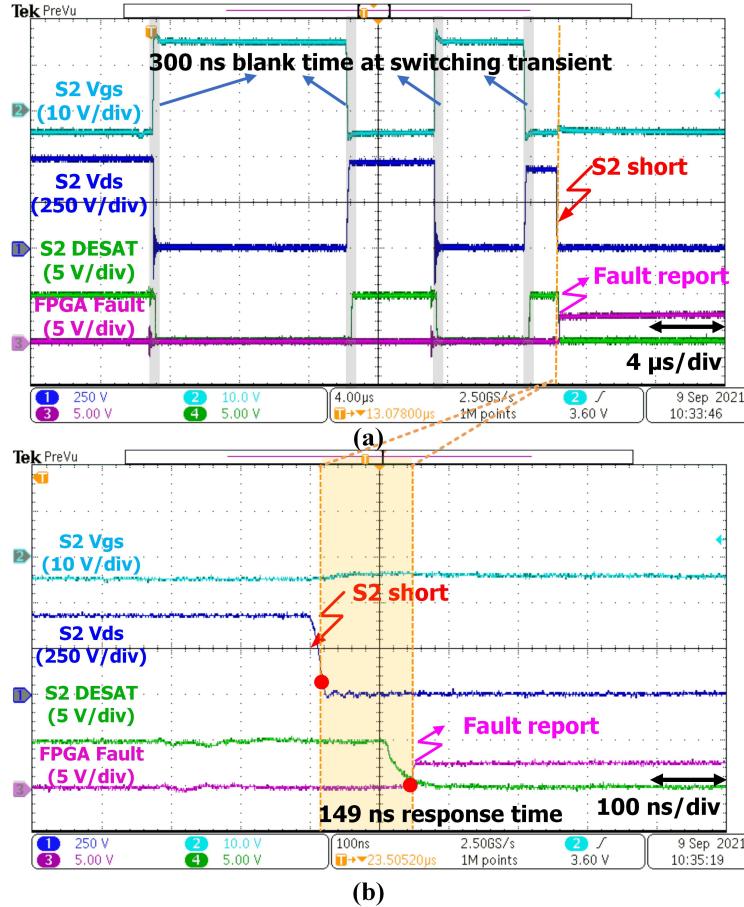
Considering that there is no difference between short-circuit and on-state of a single device, the single device SC is tested at the off-state of the whole switch

unit. This test is mimicked by turning on one (S2) of the serial devices at off-state, as shown in Fig. 4.52.



**Figure 4.52:** Test Plan of Single Device Fail-short.

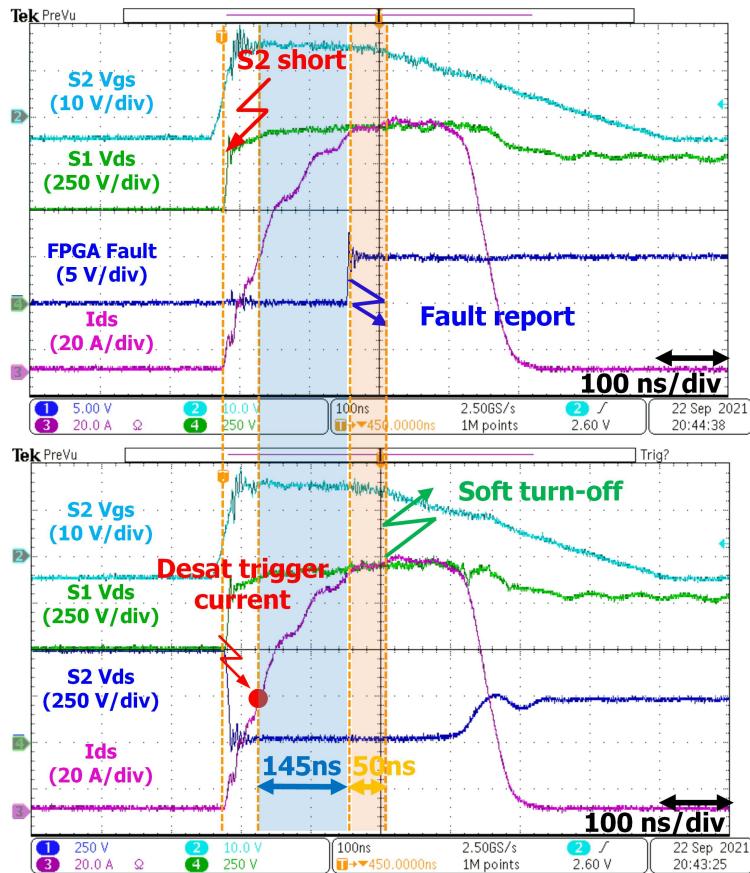
As is discussed in section III, the  $V_{ds}$  of other serial devices after short-circuit of one single device is  $V_{dc}/(n - 1)$ . Two situations should be considered based on the relationship between  $V_{ds}$  voltage and the TVS diode clamping voltage  $V_{TVS}$ . The other serial devices can successfully block the dc-link voltage if the  $V_{dc}/(n - 1)$  is smaller than  $V_{TVS}$ , as shown in Fig. 4.53(a). The gate signal of DUT is off when the S2 among the DUT is suddenly turned on to mimic the single device short circuit event. As shown in Fig. 4.53, the  $V_{ds}$  of S2 is reduced to nearly 0 V. Thus, the output of the SC detection will be pulled down. The gate signal and SC signal will be '00' at this condition. Thus, the FPGA fault signal is pulled high. The grey time slots are the blank times for each switching transient. In Fig. 4.53(b), the response time from the SC event to the FPGA fault report signal is 149 ns, which means the propagation delay time of the



**Figure 4.53:** Experimental Waveforms of Fail-short of A Single Device Among Series-connected String When  $V_{dc} < (n - 1)V_{TVs}$ : (a) Zoom-out View; (b) Zoom-in View.

detection circuit is 149 ns. It should be noted that this fault type is detected by the detection circuit of the SC device itself. Thus, the FPGA can obtain information about which device has failed.

If the  $V_{dc}/(n - 1)$  is bigger than  $V_{TVs}$ , the  $V_{ds}$  of the other serial devices will be clamped by their parallel TVS diodes. The low impedance of the dc-link loop will result in shoot-through. As shown in Fig. 4.54, the  $V_{ds}$  of S1 and S2 are equal before the SC event. After short-circuit of S2, the  $V_{ds}$  of S1 rises and is clamped by the TVS diode. In a short period after the S2 short-circuit, the  $V_{ds}$

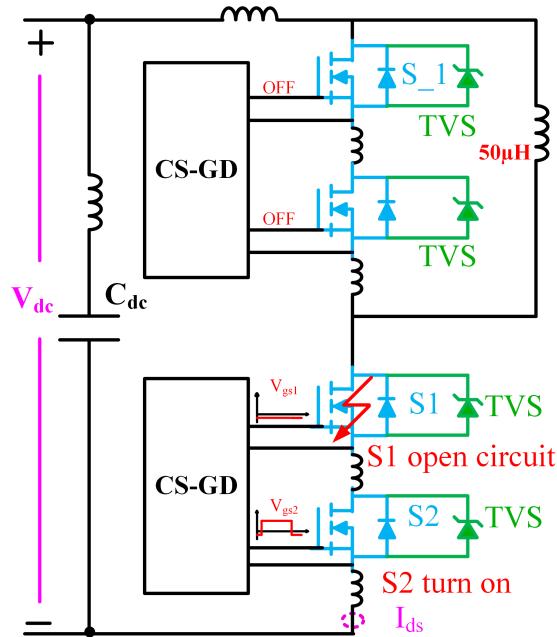


**Figure 4.54:** Experimental Waveforms of Fail-short of A Single Device Among Series-connected StringWhen  $V_{dc} > (n - 1)V_{TVs}$ .

of S2 is pulled low, and the current has not risen to the threshold current of the detection circuit. This period is 50 ns which is sufficient for the SC detection circuit to pull down the SC signal since the analog blank time is only 30 ns. Therefore, the SC state of S2 is ‘00’, which is regarded as a single device short-circuit by the FPGA. Then, the FPGA will latch this SC state and generate a fault report signal as well as a soft turn-off signal. After the current reaches the threshold current of the detection circuit, the SC detection signal will be pulled up again, and the SC state of the S2 becomes ‘01’. Even though the SC state becomes ‘01’, which is considered normal in the proposed protection scheme,

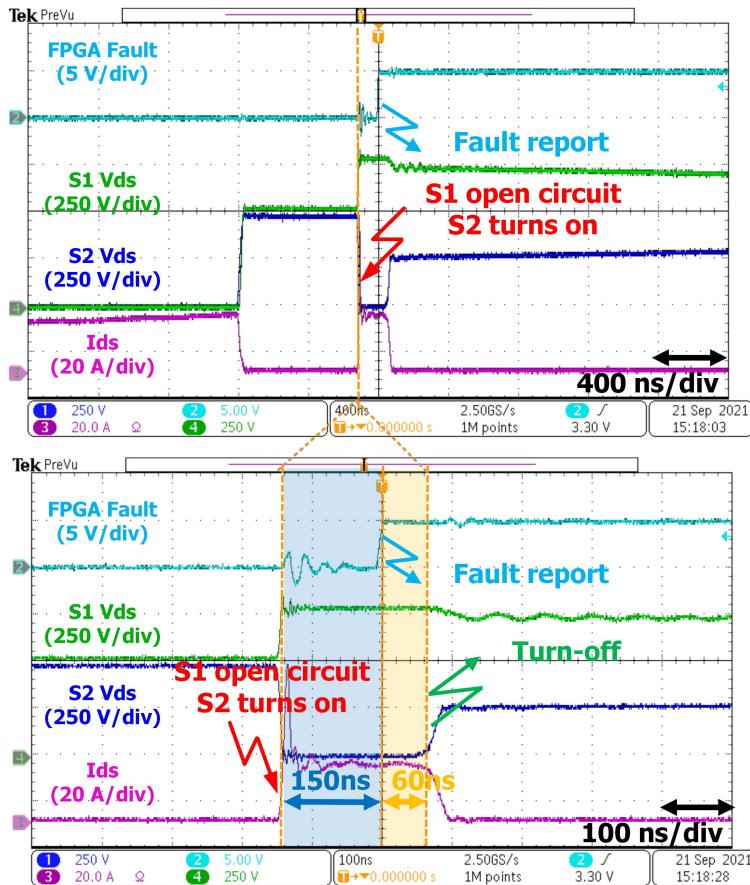
the previous fault state ‘00’ is already latched. Thus, the soft-turn-off action is not affected. The time delay from the pull-down of S2  $V_{ds}$  to the pull-up of fault report (also soft turn-off) signal is 150 ns. And it takes 50 ns from the FPGA fault signal to the start of a soft turn-off ( $V_{gs}$  starts to fall), which is the propagation delay of the soft turn-off circuit. The shoot-through at this SC scenario is mild because of the equivalent shoot-through voltage source is only  $[V_{dc} - (n - 1)V_{Tvs}]$ .

### 1.2 Single Device Open Circuit at On-state



**Figure 4.55:** Test Plan of Single Device Fail-open.

No abnormal phenomena will occur if the open circuit happens during the off-state. It is because the open-circuit acts the same as the off-state of a single device. Therefore, the single device open circuit is tested at the on-state of the whole switch unit. As shown in Fig. 4.55, this test is mimicked by keeping one of the serial devices off while turning on the other serial devices at the turn-on



**Figure 4.56:** Experimental Waveforms of Fail-open of A Single Device Among Series-connected String.

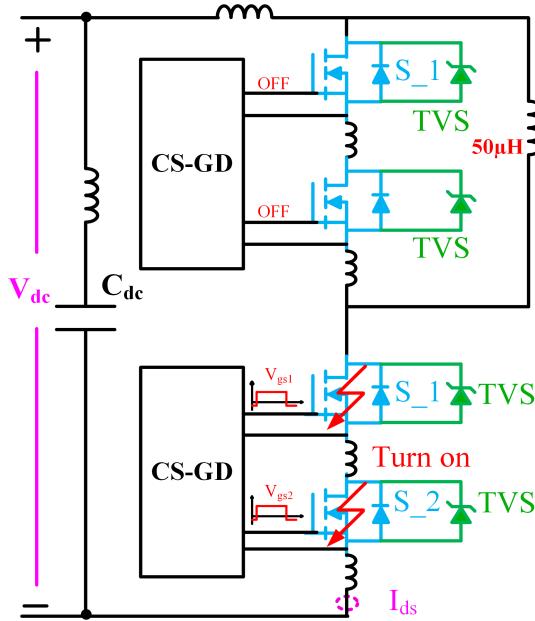
of the serial string. The complimentary switch unit is off during the turn-on of the DUT. As for the test in this article, the S1 is open while the S2 turns on. Thus, the S1 is to mimic the open-circuit device. The experimental result is shown in Fig. 4.56. Before S1 turns on, the S1 and S2 share the dc-link voltage while the high-side switch unit conducts the load current. After S1 turns on, the  $V_{ds}$  of S1 is pulled down, and the  $V_{ds}$  of S2 is charged towards dc-link voltage. However, the TVS diode clamps the  $V_{ds}$  of S2 at  $V_{TVS}$ . After that, the S1-S2 string is equivalent to a voltage source ( $V_{TVS}$ ) in series with  $R_{dson}$  of S2. The  $I_{ds}$  of S1-S2 experiences a high current spike composed of load current and reverse

recovery current of the high-side switch unit. No overcurrent happens at this fault event. The gate logic of S2 is ‘1’ while the SC detection signal is ‘1’. After 150 ns of feedback circuit propagation delay, the FPGA receives the feedback signal and outputs a fault signal to trigger the soft turn-off. Even though the overcurrent does not occur, the SC detection scheme can still recognize the fault event and take the action of soft turn-off within 150 ns.

## 2. Short-circuit of Whole Series-connected String

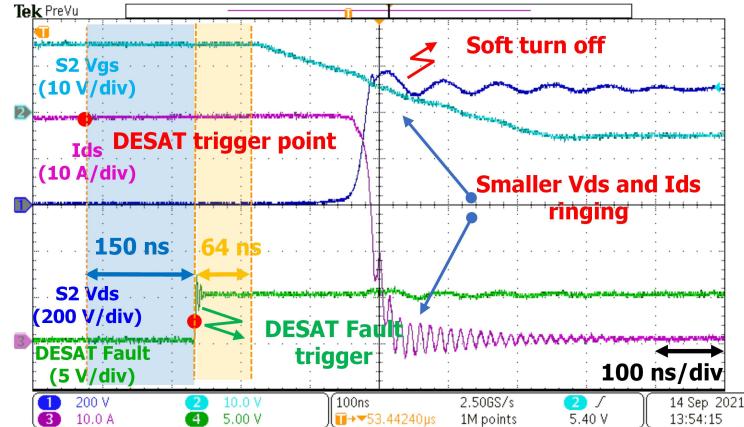
The short-circuit of the whole series-connected string is similar to the traditional single device short-circuit. The FPGA will detect the overcurrent fault if the gate signal and the  $V_{ds}$  feedback signal are ‘11’.

### 2.1 High-inductance Short-circuit

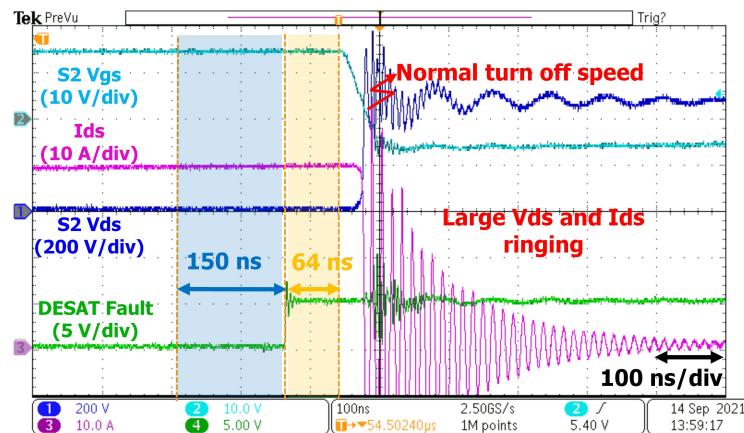


**Figure 4.57:** Test Plan of High-inductance SC of the Whole Series-connected String.

High inductance short circuit is mimicked by turning on the low-side switch unit through a  $50 \mu\text{H}$  load inductor, as shown in Fig. 4.57. And Fig. 4.58



**Figure 4.58:** Experimental Waveforms of High-inductance SC of Whole Series-connected String With Soft Turn-off.

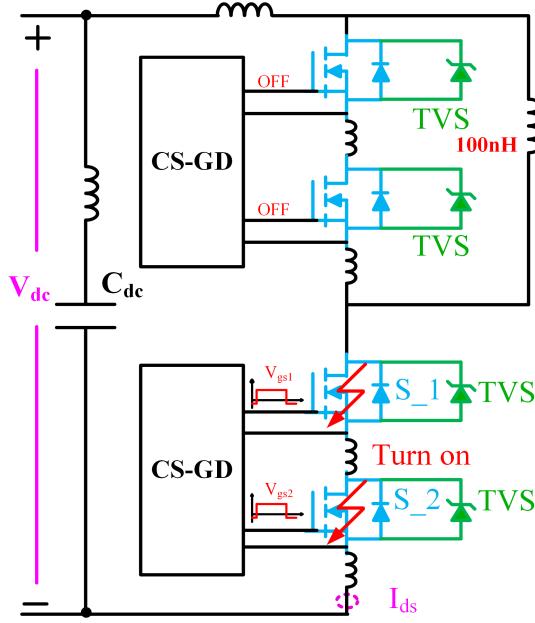


**Figure 4.59:** Experimental Waveforms of High-inductance SC of the Whole Series-connected String With Normal Turn-off Speed.

shows the typical waveforms of high inductance short-circuit. Load faults are relatively slow SC events. The response time from the point where the threshold current is exceeded to the point where the detection signal is triggered is 150 ns. After the FPGA outputs the fault and soft turn-off, it takes 64 ns to start the soft turn-off. If the normal turn-off gate current is applied, as shown in Fig. 4.59, the high switching speed induces a large oscillation of  $V_{ds}$  and  $I_{ds}$ . The overshooting of the  $V_{ds}$  may damage the device. Thus, the soft turn-off is

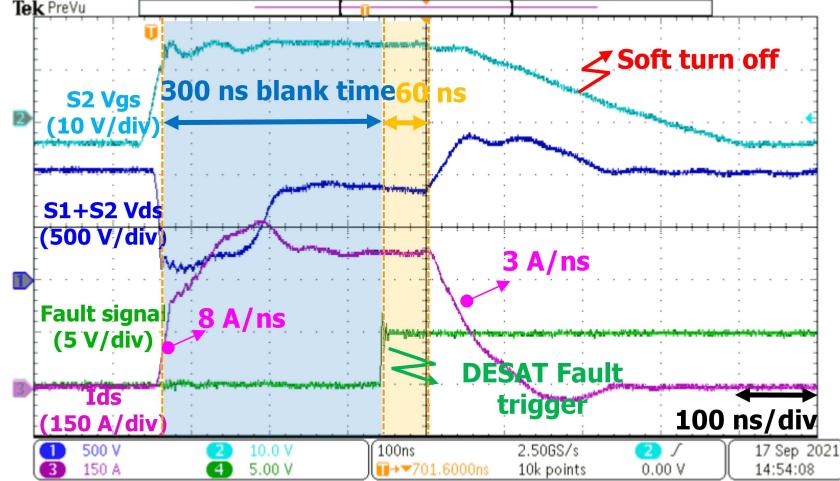
necessary for eliminating the SC event.

## 2.2 Hard-Switching Fault



**Figure 4.60:** Test Plan of HSF of the Whole Series-connected String.

The test of the HSF is to cause the shoot-through of the phase-leg by turning on the DUT, as shown in Fig. 4.60. The upper switch unit is a short circuit by a copper bus bar. As mentioned in the previous section, the dc loop inductance is around 100 nH. Fig. 4.61 shows the HSF experimental waveforms. At the beginning of the HSF, the S1 and S2 turn on, and the  $I_{ds}$  rises abruptly at 8 A/ns speed. This is because nearly all the dc-link voltage is applied to the dc loop parasitic inductance. The  $V_{ds}$  of S1 and S2 is still around 100 V. Although the gate logic signal and the SC detection signal have already become ‘11’, the fault is not reported by the FPGA after the delay time (150 ns) of the detection circuit. Because under this condition, the SC has 300 ns blank time after the switching transient. This blank time is to avoid mis-trigger of the SC fault. Thus, after 300 ns of the gate signal becomes high, the FPGA detects

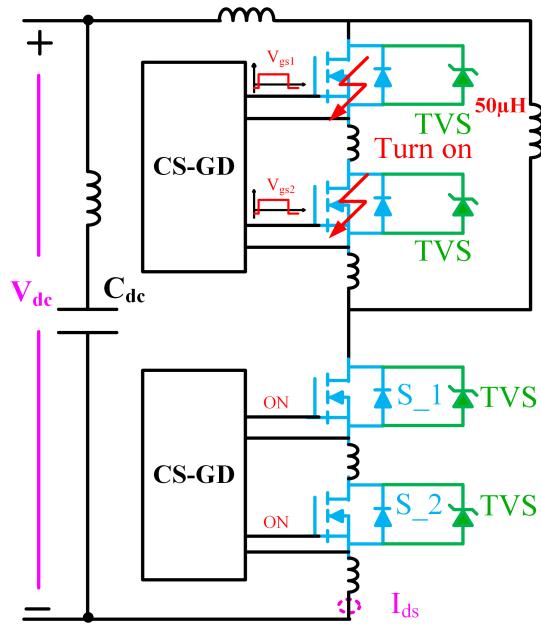


**Figure 4.61:** Experimental Waveforms of HSF of the Whole Series-connected String.

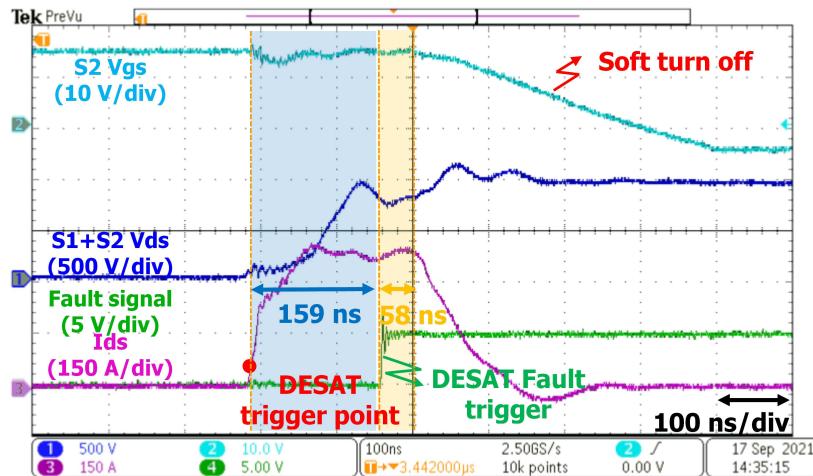
the SC fault and reports the fault signal immediately. It takes around 60 ns propagation delay for the device to start soft turn-off. The proposed protection strategy takes 360 ns to clear the HSF event. The current peak reaches 460 A, and the voltage peak is 1400 V. The total SC energy is 100.31 mJ.

### 2.3 Fault Under Load

The test of FUL is conducted by turning on the upper switch unit when the DUT is already on, as shown in Fig. 4.62. The FUL experimental waveforms are shown in Fig. 4.63. The  $V_{ds}$  of DUT starts to rise with the current after the turn-on of the upper switch unit. What is different from the HSF is that the DUT is already at on-state for a long time. Therefore, the blank time of DUT has already passed, and the FPGA is ready to monitor the SC event at the beginning of the FUL. The 159 ns between the moment where DeSat triggers and the moment where FPGA detects the fault is the propagation delay of the detection circuit. And after the propagation delay of the soft turn-off circuit, the device starts to turn off gently. The  $di/dt$  at the beginning is 8 A/ns, and

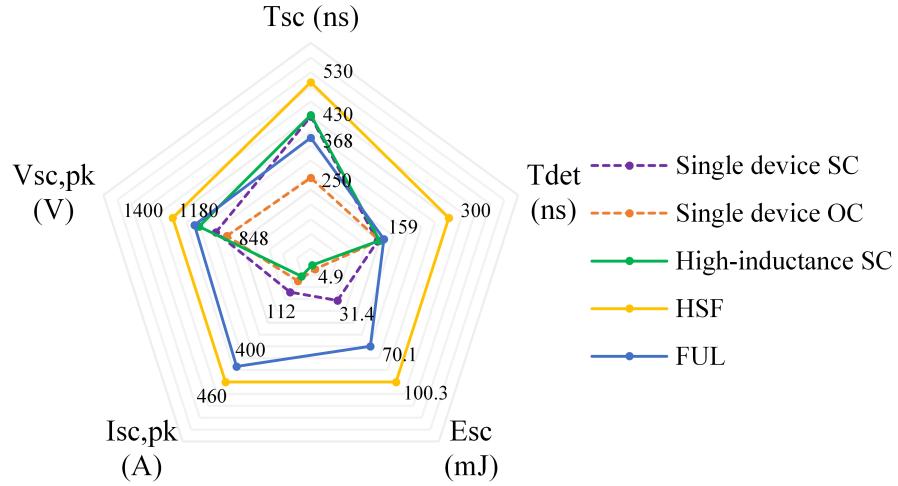


**Figure 4.62:** Test Plan of FUL of the Whole Series-connected String.



**Figure 4.63:** Experimental Waveforms of FUL of the Whole Series-connected String.

the current peak is around 400 A. The  $V_{ds}$  voltage spike is 1200 V. For the FUL event, the response time of the protection is 217 ns, which is smaller than that of the HSF event. It is because the blank time (300 ns) at the turn-on transient of HSF prolongs the response time. Thanks to the shorter response time, the SC energy of FUL is 70.1 mJ.



**Figure 4.64:** Comparison of Each SC Scenario Using the Proposed SC Protection Method.

According to the discussion on the SC behavior, the performance of the proposed short-circuit protection for each scenario is compared based on the critical assessment metrics summarized in Table 4.5. A lower value of each metric infers less electrical or thermal stress imposed by a SC event. The overall performance is compared by comprehensively weighting all five metrics, as shown in Fig. 4.64. Because the STO reaction time  $T_{reac}$  is around 60 ns for every SC scenario, this metric is not included in the comparison. It can be concluded that the HSF is the worst-case condition for the proposed SC protection method. The reason is that the blank time for blocking the switching transient delays the response time of the SC protection.

### C. Reliability Test

**Table 4.7:** Reliability Test of Overcurrent Cases with Different Threshold Voltage at Room Temperature.

$V_{th,dst}(V)$	$I_{load}(A)$	20	30	50	60
2	+	+	Y	Y	
5	Y	Y	Y	Y	
10	Y	Y	-	-	

Table 4.7 shows the experimental results of overcurrent fault cases at different threshold voltage at room temperature. ‘+’ means false positive, ‘-’ means false negative, and ‘Y’ means protection circuit operates normally. It can be seen that when the threshold voltage is low, the false positive may happen. When the threshold voltage is high, the false negative may happen.

**Table 4.8:** Reliability Test of Single Device Fail-open and Fail-short Cases with Different Threshold Voltage at Room Temperature.

$V_{th,dst}(V)$	$I_{load}(A)$	20	30	50	60
2	+	+	Y	Y	
5	Y	Y	Y	Y	
10	Y	Y	Y	Y	

Table 4.8 show the experimental results of single device fail-open and single device fail-short cases at different threshold voltage at room temperature. Each test condition is tested with normal device and faulty device, respectively. The faulty cases can be protected in time for all the test conditions. However, the false positive occurs at

**Table 4.9:** Reliability Test of All the Fault Scenarios with Different Blank Time at 5.5 V Threshold Voltage.

$t_{blk}$ (ns) \ $I_{load}$ (A)	20	30	50	60
2	+	+		
5	Y	Y	Y	Y
10	Y	Y	Y	Y

normal device operating condition when the threshold voltage is low.

As for the blank time's impact on the reliability, the test results for all the fault scenarios are the same. Table 4.9 shows the experimental results of all the fault scenarios at different blank time. It can be found that when the blank time is at 100 ns, the false positive happens.

#### 4.2.6 Conclusions

The SC scenarios of series-connected devices are more complex than that of a single device. This article proposes a systematic fault analysis methodology to find all the possible SC scenarios. Because some unique SC scenarios do not cause overcurrent phenomenon, the existing SC protection methods (overcurrent-based) cannot cover all the SC scenarios of series-connected devices. In this article, the  $V_{ds}$  detection circuit combined with gate logic signal is designed to comprehensively detect all the SC scenarios for series-connected SiC MOSFETs. Besides, the STO of series-connected devices for terminating the SC event is different from single device applications. It is because the  $V_{ds}$  voltage sharing should be guaranteed when STO is implemented. Thus, different from single device applications, where the STO is activated at the secondary side of the gate driver, the signal of STO for the series-connected devices

is sent to each serial device synchronously from the controller side. During the on/off switching transient, the logic combination of the gate signal and the  $V_{ds}$  feedback signal may cause mis-trigger of the SC protection. Thus, the blank time is introduced to block the switching transient. However, due to the blank time, the SC protection performance of the HSF is compromised. It is because the blank time after the turn-on transient increases the SC response time. For the proposed SC protection method, the HSF is the worst-case. The experimental results validate that the proposed SC protection method can successfully protect the serial devices from further destruction under each SC scenario.

## Chapter 5

### MEGA-HERTZ HIGH VOLTAGE EMAT LCC RESONANT INVERTER USING SiC MOSFETS

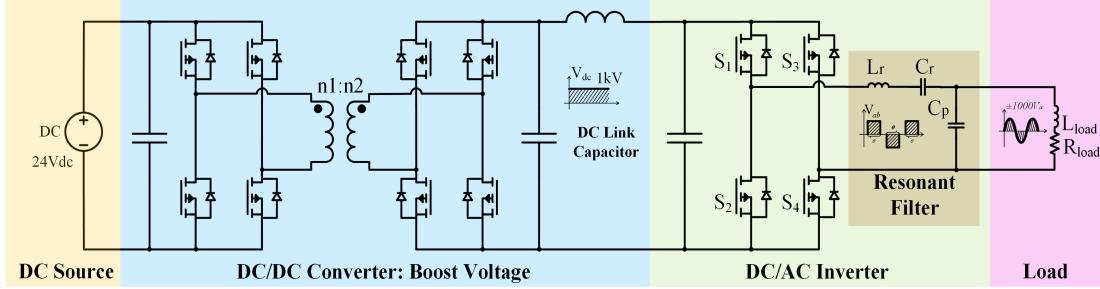
Previous chapters have illustrated how to drive the high switching speed WBG devices. Except for driving the WBG devices, there are system level considerations in the practical design of the WBG based converter. In this chapter, a LCC resonant inverter operating in burst mode is developed using SiC MOSFET discrete devices. To measure thickness of the metal in a non-contact manner is required in many industrial areas, such as pipeline in-service defect inspection [100], flaw detection in steel products and  $raI_{Lr}oad$  inspection, etc [101]. Electro-Magnetic Acoustic Transducer (EMAT) sensing technology [102, 103] is a competitive candidate for this thickness measurement application. The EMAT sensor, which serves as the load of the LCC resonant inverter, is an inductive load and has large load variation range. Therefore, the LCC resonant filter design guideline is proposed to cope with this special load. Moreover, under the burst mode condition, the start-up and ending transient should be suppressed so that the performance of the EMAT sensor will not be compromised. The transient state analysis is used to propose a new start-up method, which pre-charges the filter tank to a state close to the final steady state. Since there is no additional hardware and pre-charge timing issue, it can be open-loop and much convenient. At last, an echo extraction receiving circuit is designed to scale down the

high voltage transmitting signals while maintaining the weak receiving signals.

### 5.1 Benefits of SiC MOSFETs

As mentioned previously, one of the challenges faced by the EMAT pulser is to achieve high voltage and high frequency simultaneously. In the pulser application, MARX generator with solid state switches is widely used [105, 106]. It basically charges capacitors in parallel and discharges them in series to elevate the output voltage. Some improved topologies can achieve narrow pulses [107–109]. However, the equivalent pulse frequency cannot reach the megahertz level, and the circuit is very complicated, with five or higher number of stages. Moreover, these MARXs cannot produce the sinusoidal output voltage, which is a critical requirement for EMAT power supply. Additionally, the overvoltage and overcurrent protection of MARX is very complicated, which also brings obstacles to its application on EMAT sensors with harsh environments and difficult maintenance [110–112]. The simplest and most reliable topology of the inverter is the H-bridge. However, conventional Si IGBTs and Si MOSFETs cannot switch at megahertz and kilovolt to complete the required conversion. Si MOSFETs at megahertz switching frequency can only withstand a few hundred volts. Si IGBTs above 1 kV can only sustain a switching frequency of several kilohertz, limited by low switching speed and high switching loss [8]. Therefore, the state-of-the-art solution of EMAT power supply adopts a three-stage design: a low-to-intermediate voltage step-up DC/DC converter (e.g., 24 V to 200 V), a full bridge inverter based on Si MOSFETs, and a high-frequency pulse transformer boosting the voltage to the target (e.g.,  $\pm 800$  V) [113]. Due to the resonance between transformer parasitic capacitance and load coil inductance, this topology suffers from high THD on the AC output side. SiC MOSFETs can operate at megahertz and kilovolt because its switching speed is 10 times faster than Si

MOSFETs [8, 114], eliminating the high-frequency pulse transformer and simplifying the system into two stages: DC/DC boost stage and inverter stage. Moreover, the resonant filter can be implemented at the inverter output to achieve better THD, as shown in Fig. 5.1.



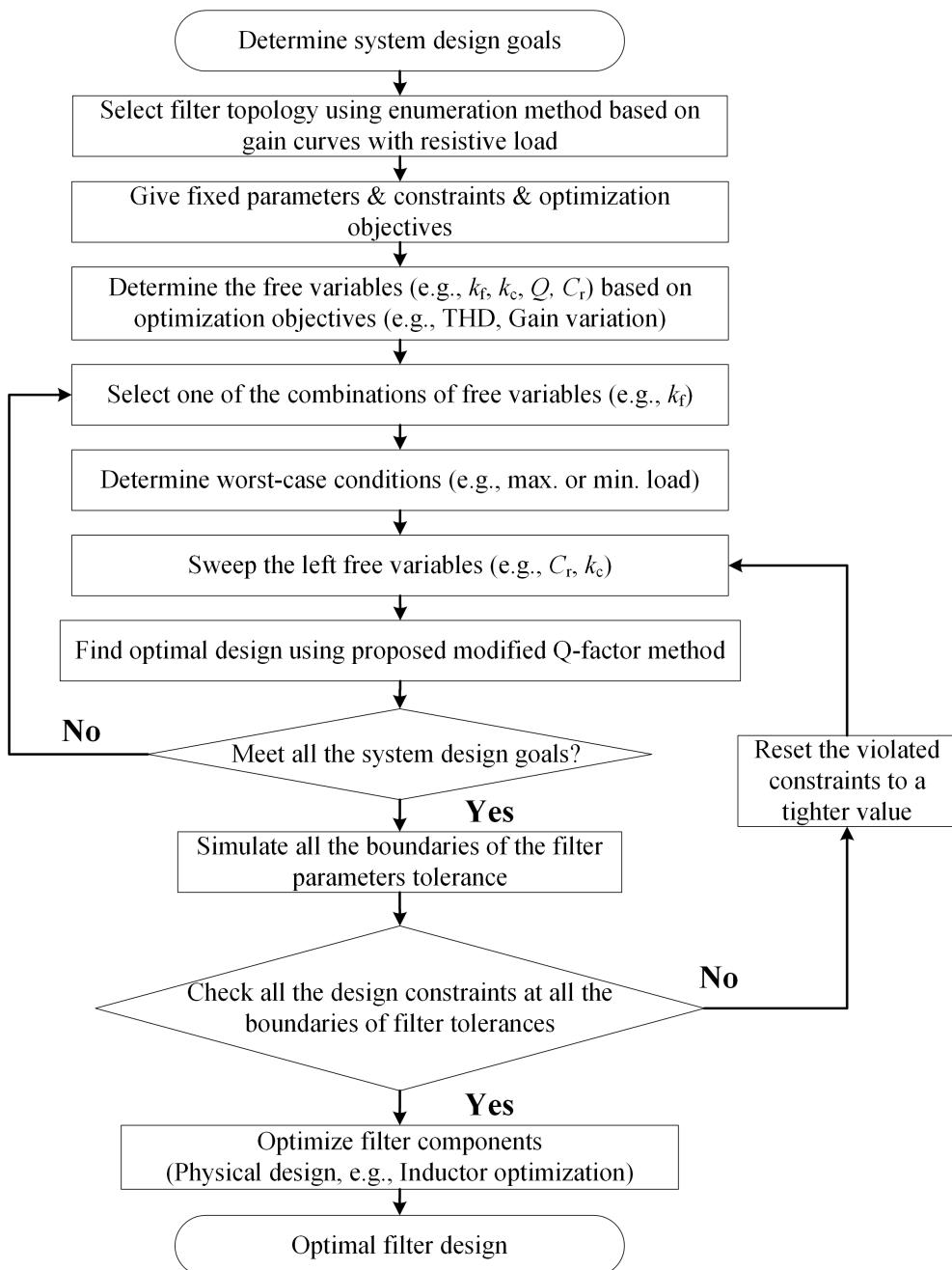
**Figure 5.1:** Circuit Diagram of  $24V/\pm 1kV$   $1.5MHz$  Pulser Inverter.

## 5.2 Resonant Filter Selection and Optimization

In the proposed circuit shown in Fig. 5.1, the output of the inverter can only be a square wave with the desired amplitude ( $1\text{ kV}$ ) and fundamental frequency ( $1.5\text{ MHz}$ ). To obtain the sine wave output, SPWM modulation is widely used. However, it requires the inverter to operate at several times of fundamental frequency. It is impossible for the current SiC MOSFET technology to switch at tens of megahertz to control the harmonics through SPWM modulation. Therefore, the resonant filter should be designed to convert the inverter square wave to the sine wave. The design flowchart of the resonant filter is depicted in Fig. 5.2.

The filter design process includes filter topology selection, filter parameter optimization and filter physical component design. The filter design goals are summarized as follows:

1. Low THD for whole load range, which means large attenuations for low-order



**Figure 5.2:** Resonant Filter Optimal Design Flowchart.

harmonics;

2. ZVS for whole load range, which means sufficient inductive inverter output current should be guaranteed;
3. Less than 20% voltage gain variation for entire load range;
4. Appropriate voltage and current stress on the filter elements.

### 5.2.1 Filter Topology Selection

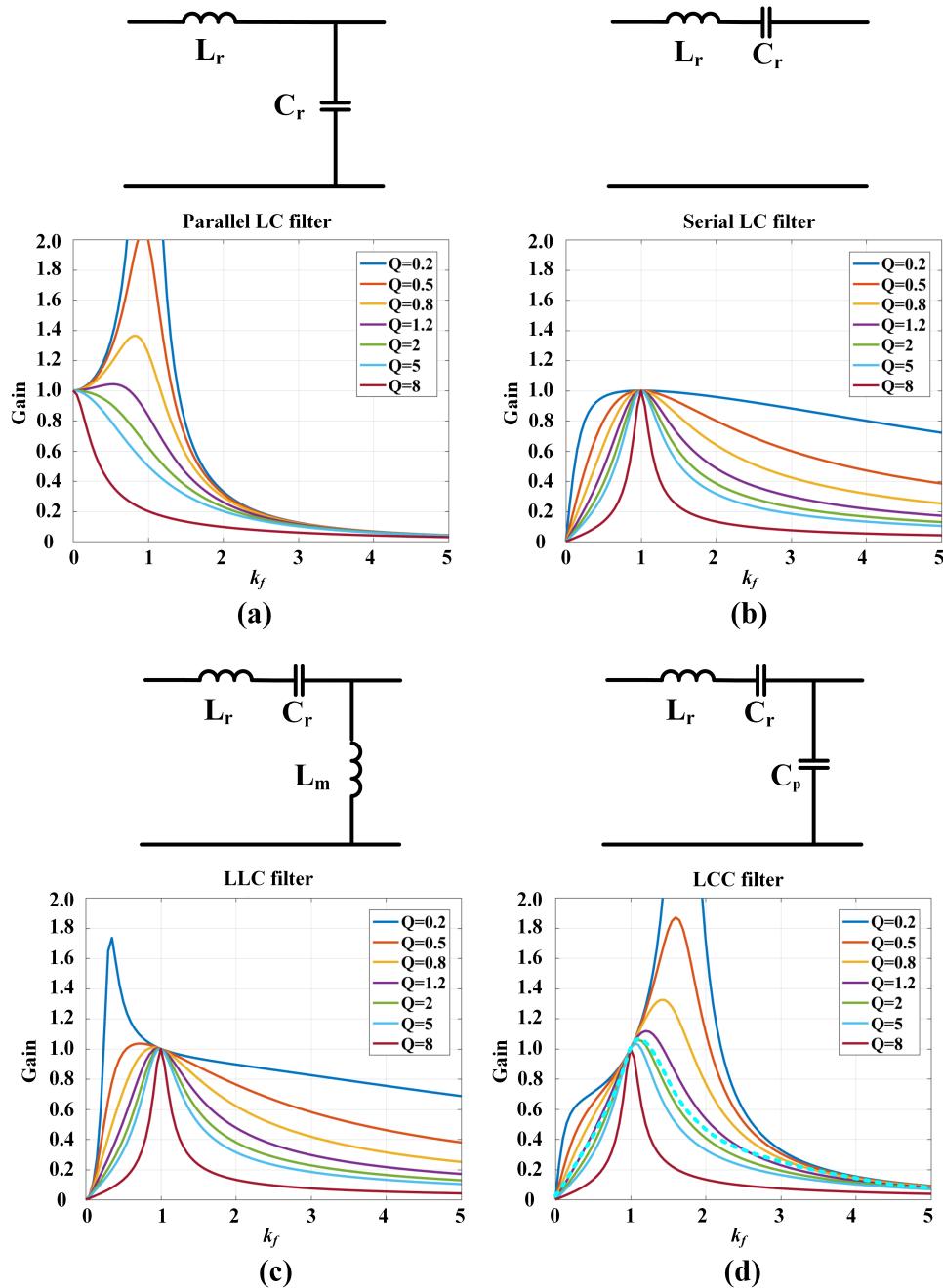
Based on the design goals, possible filter candidates can be selected according to the resonant tank selection methodology in [122, 188]. The parallel LC filter, series LC filter, LLC filter and LCC filter are four potential candidates. It is necessary to understand how the voltage gain behaves as a function of the frequency ratio ( $k_f$ ) and Q factor. Traditionally, the frequency ratio ( $k_f$ ) and Q factor ( $Q_{tra}$ ) are defined as 5.1 and 5.2.

$$k_f = \frac{\omega_0}{\omega_r} \quad (5.1)$$

$$Q_{tra} = \frac{\omega_0 L_r}{R} \quad (5.2)$$

where  $\omega_0$  is the switching frequency, which is 1.5 MHz in this design;  $R$  is the load resistance;  $L_r$  is the filter inductance;  $\omega_r$  is filter series resonant frequency.

In the gain function, the frequency ratio  $k_f$  is the control variable. As such, a good way to explain the behavior of the gain function is to plot gain curves with respect to  $k_f$  at given load conditions. The gain curves of these four filters with different Q factors are plotted in Fig. 5.3.



**Figure 5.3:** Gain Curve for (a) Parallel LC Filter (b) Serial LC Filter (c) LLC Filter (d) LCC Filter.

The traditional gain curve method (Q factor) is based on the FHA model [125, 126] with a resistive load  $R$  whose impedance does not change with frequency (x-axis of the gain curve plot). Thus, it is reasonable to use Q factor range to represent the load range. In the EMAT application, the load is inductive, and its impedance increases with frequency. The new Q-factor and the load are not one-to-one correspondent. Thus, the conventional filter design method is not applicable. Take the LCC filter in Fig. 5.3(d) as an example, considering the load impedance change, the actual gain curve of the inductive load with  $Q = 2$  at resonant frequency should be the blue dashed line. However, at topology selection stage, the gain curve can still be plotted with the assumption of fixed load impedance. It is because the filter characteristics themselves are not affected by load conditions.

**Table 5.1:** Characteristics Summary of Filter Candidates.

Filter topology	Harmonics suppression	Gain variation at ZVS region
Parallel LC	Good	Big
Serial LC	Fair	Big
LLC	Bad	Small
LCC	Good	Fair

Another function of the filter tank is to help the H-bridge inverter achieve ZVS. In this way, the threat of EMI problems and high  $dv/dt$  induced overvoltage failure of SiC MOSFETs can be mitigated to a large extent. Although the classic soft-switching oriented LLC filter is superior to guarantee unity-gain at resonant frequency under various load, it has a relatively flat voltage gain curve around resonant frequency. Therefore, the harmonics attenuation is not sufficient to achieve low THD. The same issue occurs on serial LC filter unless the Q factor is very high, as shown in Fig.

5.3(b). But a high Q factor leads to high voltage/current stress and large component size [51]. For this kind of non-soft-switching oriented filter, the switching frequency should be higher than the resonant frequency to operate at the ZVS region [188]. The drawback of this strategy is that the voltage gain will fluctuate drastically when the load changes. The serial LC filter has large gain at the ZVS region while the voltage gain of harmonics is also big. The parallel LC filter, as presented in Fig. 5.3(a), has sufficient harmonics attenuation, but the voltage gain at operating frequency is relatively low. The LCC filter combines the benefits of these two filters, large harmonics attenuation (parallel LC filter) and large gain at ZVS region (serial LC filter). The concerned objectives of these four filters are summarized in Table 5.1. The LCC filter is the best candidate to achieve high attenuation of harmonics at ZVS region and acceptable voltage gain variation in wide load range.

### 5.2.2 Optimization of Resonant Filter Parameters

The resonant filter design procedure is a multiobjective optimization problem under system constraints. The resonant elements consist of series inductor ( $L_r$ ), series capacitor ( $C_r$ ) and parallel capacitor ( $C_p$ ). The resonant elements and the load condition directly determine the filter performance. The constraints and optimization objectives can be derived and quantified from the system design goals. The optimization process is illustrated as follows.

#### 1) Specify Fixed Parameters:

The fixed parameters include the switching frequency ( $\omega_0$ ), the inverter dead-time ( $t_d$ ) and the load range ( $R_{load}L_{load}$ ). The load in this system is inductive, and its parameter is determined by the coil structure, the thickness of the tested metal and the material of the tested metal. Basically there are two kind of metals at the boundary of the load range, the aluminum bar and the cast iron. The thickness of

metal is from 5 millimeter to 50 millimeter. The load parameters are measured using impedance analyzer *Agilent 4294A* and summarized in Table 5.2.

**Table 5.2:** Extreme Load Parameters.

Load material	Thickness	Load parameters at operating freq. $\omega_0$
Cast iron	5 mm	$16.9 \Omega + 1.9 \mu H$
	50 mm	$24.1 \Omega + 3.2 \mu H$
Aluminum	5 mm	$15.3 \Omega + 0.4 \mu H$
	50 mm	$21.7 \Omega + 0.6 \mu H$

2) Determine the Constraints:

The constraints can be derived from the system design goals listed at the beginning of this section. The first constraint is the variation range of the voltage gain over the entire load range. Therefore, this constraint is quantified as a voltage gain range of 0.8-1.2.

$$0.8 < G_v(\omega_0) < 1.2 \quad (5.3)$$

where  $G_v(\omega_0)$  is the voltage gain at switching frequency. The LCC filter gain  $G_v$  can be expressed as 5.4. The definitions of capacitance ratio  $k_c$ , series resonant frequency  $\omega_r$  and modified Q-factor  $Q_{\text{new}}$  are expressed below:

$$G_v = \frac{1}{\sqrt{(1 - k_c \times k_f^2 + k_c)^2 + (Q_{\text{new}} \times (k_f - 1/k_f))^2}} \quad (5.4)$$

$$k_c = C_p/C_r \quad (5.5)$$

$$\omega_r = 1/\sqrt{L_r C_r} \quad (5.6)$$

$$Q_{\text{new}} = \frac{\omega_r L_r}{\sqrt{R_{\text{load}}^2 + (\omega_0 L_{\text{load}})^2}} \quad (5.7)$$

where  $C_p$  is the parallel capacitance;  $C_r$  is the series capacitance;  $R_{\text{load}}$  is the load resistance;  $L_{\text{load}}$  is the load inductance. The second constraint is to guarantee ZVS soft-switching. The gain curve at the operation region should have negative slope, as expressed by 5.8. Meanwhile, at switching transient, it requires sufficient energy stored in the filter inductance to charge the junction capacitance to full dc-link voltage, as expressed in 5.9 [189, 190].

$$\left. \frac{dG_v}{dk_f} \right|_{\omega=\omega_0} < 0 \quad (5.8)$$

$$W_{\text{filter}} = \frac{1}{2} L_r I_L^2 > W_{\text{jct}} = Q_{\text{oss}} V_{\text{dc}} \quad (5.9)$$

where  $Q_{\text{oss}}$  is the equivalent charge at dc-link voltage considering the nonlinear  $C_{\text{oss}}$ ;  $I_L$  is the inductor current at switching transient;  $V_{\text{dc}}$  is the dc-link voltage;  $W_{\text{jct}}$  is the energy needed for the junction capacitance, and the filter stored inductive energy is  $W_{\text{filter}}$ . If  $W_{\text{filter}}$  is bigger than  $W_{\text{jct}}$ , ZVS can be guaranteed with suitable dead-time [189].

The last constraint is the voltage and current stress on the resonant elements. The voltage stress on  $C_p$ ,  $C_r$  and current stress on  $L_r$ ,  $C_r$ ,  $C_p$  determines the components' size and cost. The equations below are the voltage and current stress on each filter component with desired constraints:

$$V_{C_p} = V_{\text{load}} \quad (5.10)$$

$$V_{Cr} = \left| \frac{1}{k_f} \times Q_{new}(\omega_0) \times (k_f \times k_c / Q_{new}(\omega_0) + 1) \times V_{load} \right| < 1.8V_{load} \quad (5.11)$$

$$I_{Lr} = |(k_f k_c / Q_{new}(\omega_0) + 1) \times I_{load}| < 1.5I_{load} \quad (5.12)$$

$$I_{Cp} = |k_f k_c / Q_{new}(\omega_0) \times I_{load}| < 0.5I_{load} \quad (5.13)$$

$$I_{Cr} = |(k_f k_c / Q_{new}(\omega_0) + 1) \times I_{load}| < 1.5I_{load} \quad (5.14)$$

where  $I_{load}$  and  $V_{load}$  are the load current and voltage.

### 3) Optimize THD of the Output Voltage:

The optimization target can be any single design goal or a weighting function of multiple design goals. In this design procedure, the THD of the output voltage is selected as the optimization objective, and other design goals have been quantified as design constraints at the previous step. It is because the THD of the output voltage plays a most important role in EMAT measurement accuracy. Assume the inverter output voltage is a square wave. Based on the Fourier series of the square wave, THD can be expressed as 5.15.

$$\begin{aligned} THD_v &= \frac{\sqrt{\sum_{n=1}^{\infty} \left[ \frac{1}{3} G_v(3\omega_0) \right]^2 + \left[ \frac{1}{5} G_v(5\omega_0) \right]^2 + \left[ \frac{1}{7} G_v(7\omega_0) \right]^2 \dots}}{G_v(\omega_0)} \\ &= \frac{\sqrt{\sum_{n=1}^{\infty} \left\{ \frac{G_v[(2n+1)\omega_0]}{2n+1} \right\}^2}}{G_v(\omega_0)} \end{aligned} \quad (5.15)$$

From the qualitative gain curve of LCC filter in Fig. 5.3(d), the frequency ratio  $k_f$  should be bigger than one to operate at ZVS region. However, if  $k_f$  is too big, the

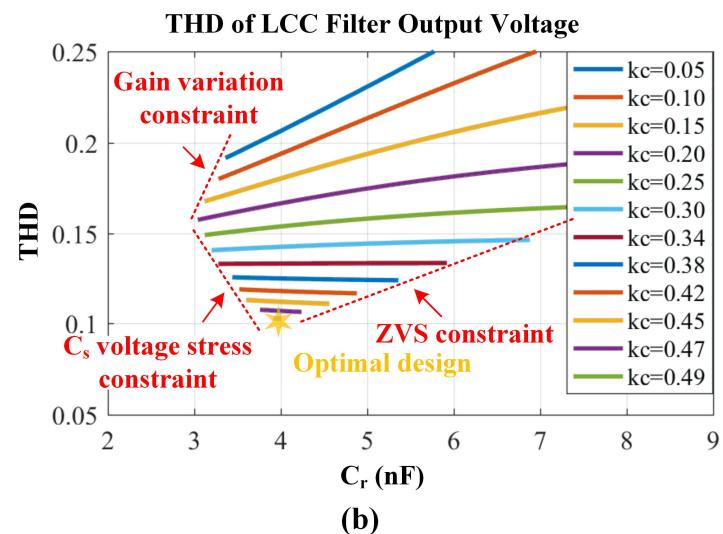
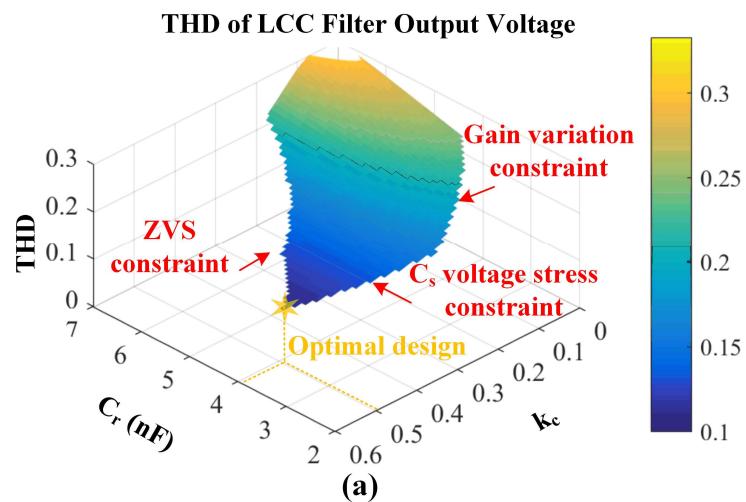
gain at operating frequency will be small. Thus,  $k_f$  is selected to be 1.2 as the pre-determined parameter. If this parameter does not meet the system goals afterwards,  $k_f$  will be re-selected. As for Q factor, one of the four extreme loads can be the worst-case for THD. Thus, per 5.7, the  $Q_{\text{new}}$  of four extreme loads will be selected as the worst-cases.

The tolerance effect is a design margin issue faced by all types of resonant converters. Therefore, the component tolerances should be within a reasonable range. Usually the design margin provided by the FHA design approach should be sufficient [191]. To be more accurate, simulation is necessary to confirm the design margin. In the last step of optimization process, all the boundaries of the filter tolerance will be simulated to check the constraints. If certain constraint is violated, this constraint will be reset to a more stringent value until all the constraints are met within tolerance.

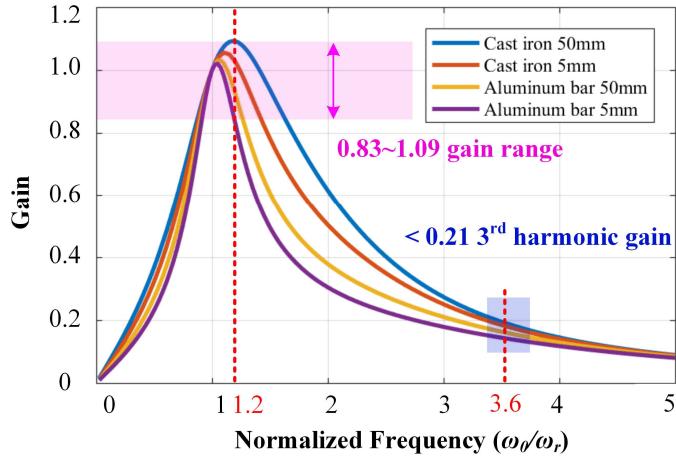
The optimization plots of THD for different ( $k_c$ ,  $C_r$ ) at worst-cases under constraints is shown in Fig. 5.4. The optimal THD at this worst-case is 10.99%. As mentioned before, it is not reasonable anymore to use different Q to represent the load range. Therefore, four extreme load conditions are directly listed to represent the load range of this application. By following the above process, the THD is optimized for this LCC filter, leading to optimized gain curves, as shown in Fig. 5.5. The optimal parameter set is ( $k_f = 1.2$ ,  $k_c = 0.49$ ,  $C_r = 3.9nF$ ). The passive parameters  $L_r$  and  $C_p$  can be calculated according to the following equations:

$$L_r = \frac{1}{\omega_r^2 C_r} \quad (5.16)$$

$$C_p = C_r \times k_c \quad (5.17)$$



**Figure 5.4:** THD Optimization of LCC Filter.



**Figure 5.5:** Gain Curves of Designed LCC Filter Under Extreme Load Conditions.

The final design values are:  $L_r = 4.2\mu H$ ,  $C_r = 3.9nF$ ,  $C_p = 1.95nF$ ,  $f_r = 1.24MHz$ .

### 5.2.3 Filter Components Physical Design Considerations

After the resonant tank parameters are optimized, the filter components can be selected considering the burst mode operation condition. The big difference between the burst mode operation and the continuous mode operation is the thermal stress. In the burst mode operation, the average loss in the whole repetitive frequency (e.g., 50 Hz) is very small. Therefore, the physical design considerations of the capacitor and the inductor is special.

#### 1. Capacitor Selection:

The AC voltage rating of the capacitor does not need to be derated following the curve of ‘AC voltage rating vs. operating frequency’ in the datasheet [192]. It is because the AC voltage rating at high frequency is limited by the thermal stress under continuous operating condition. In the burst mode condition, the capacitor should be selected based on the pulse current limitation ( $dv/dt$  capability in the datasheet [192])

and DC voltage rating. Thus, the AC voltage rating does not need to be derated with frequency, as long as the DC voltage rating is bigger than the peak AC voltage stress with some safety margin [193].

## 2. Inductor Design:

The inductor design includes the core design and the winding design. For resonant inductor, the inductance variation should be small to guarantee the steady performance of the resonant filter. The inductance ( $L$ ) physical equation is as 5.18.

$$L = \frac{\mu \cdot N^2 \cdot A_c}{l_m} \quad (5.18)$$

where  $\mu$  is the permeability of the core;  $N$  is the number of turns;  $A_c$  represents the core cross-sectional area;  $l_m$  is the magnetic circuit length.

If the design is complete, the physical parameters  $N$ ,  $A_c$  and  $l_m$  are fixed. However, based on the B-H curve, the permeability ( $\mu$ ) is related to the saturation level of the core flux density. Thus, the priority consideration of this inductor design is to make the maximum flux density ( $B_{\max}$ ) far from the saturated flux density ( $B_{\text{sat}}$ ).

Therefore, this problem becomes to choose a core with high saturation flux density. For the core material, the nanocrystalline core and powder core have high  $B_{\text{sat}}$ . However, compared with powder core, the nanocrystalline core usually does not have toroid shape, which is not convenient for assembly. Thus, the toroid powder core is selected. The  $B_{\text{sat}}$  of High-Flux series from Magnetics can be 1.5 Tesla, and it is cost-effective. The inductor design guideline of the powder core is the well-known area product (AP) method. In the burst mode operation, the only constraint is that the inductance drop at peak current does not exceed 20% of the DC inductance value. Since the inductor loss is not a constraint, the wire diameter of the winding can be small. What is special in burst mode is that the size of the inductor is not

compromised by the temperature rise or the window filling factor, etc., which are the common bottlenecks in the inductor optimization. The final design is the minimum inductor size to meet all the constraints.

The final filter components are listed in Table 5.3.

**Table 5.3:** Optimized LCC Filter Components.

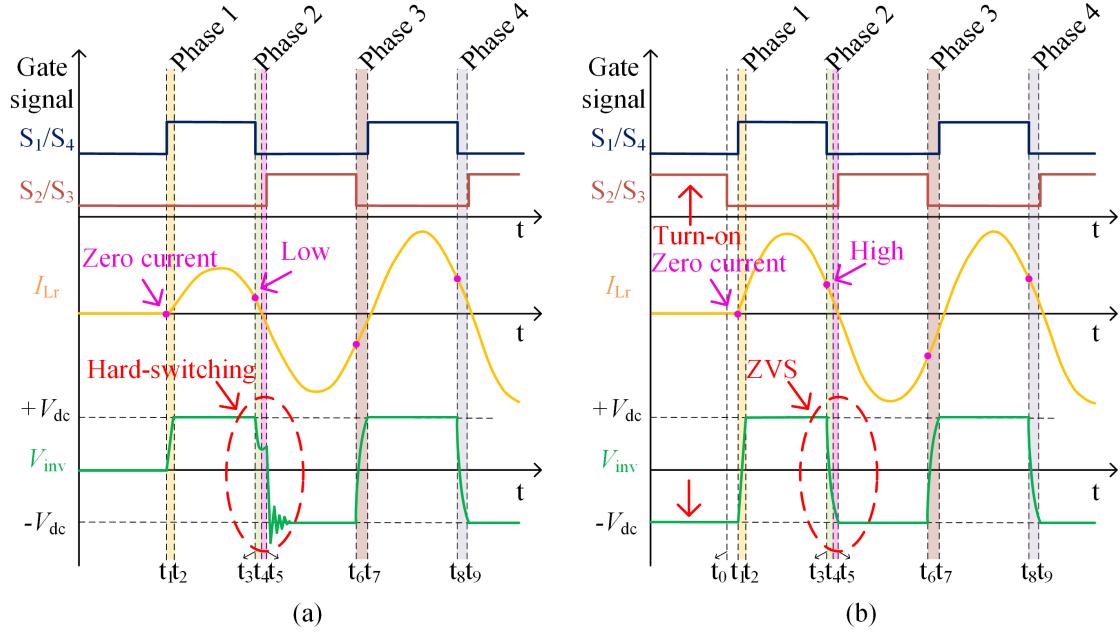
Components	Value	Part number	Note
<b>Inductor core</b>	$4.2 \mu H$	0058932A2	High-Flux power core
<b>Inductor number of turns</b>	11	-	-
<b>Inductor wire gauge</b>	12	-	-
$C_r$	3.9 nF	BFC238370392 (2 in parallel; 2 in series)	5 kV/104 A pulse rating
$C_p$	1.95 nF	BFC238370392 (2 in series)	5 kV/52 A pulse rating

### 5.3 Transient Elimination Strategy in Burst Mode Operation

In the burst mode operation, the system has to start and end repetitively. Therefore, the start-up and ending transient process should be dealt with properly.

#### 5.3.1 Pre-charge Strategy to Avoid First Pulse Low Energy

The start-up transient waveform is presented in Fig. 5.6(a). Although the filter has been designed to guarantee the ZVS operation, the initial pulse may still be hard-switching. It is because the filter is designed for the steady state operation, during which the filter has the initial energy. However, at the start-up transient, the filter is



**Figure 5.6:** Start-up Transient Waveforms: (a) Without Pre-charge Strategy; (b) With Proposed Pre-charge Strategy.

at zero state. Thus, the ZVS will not happen. The detailed analysis is illustrated as follows:

1. Phase 1 ( $t_1-t_2$ ):

The first switching process starts at the turn-on of S1/S4, which is a zero current turn-on process. Since the turn-on current is zero, there is no transient issue at phase 1.

2. Phase 2 ( $t_3-t_5$ ):

The second switching process starts at the turn-off of S1/S4. During this dead-time, the inductor current ( $I_{Lr}$ ) lags the inverter output voltage ( $V_{inv}$ ). This lagging current helps to discharge the junction capacitance of S2/S3. If the current is sufficient, the  $V_{ds}$  of S2/S3 can be discharged to zero before S2/S3

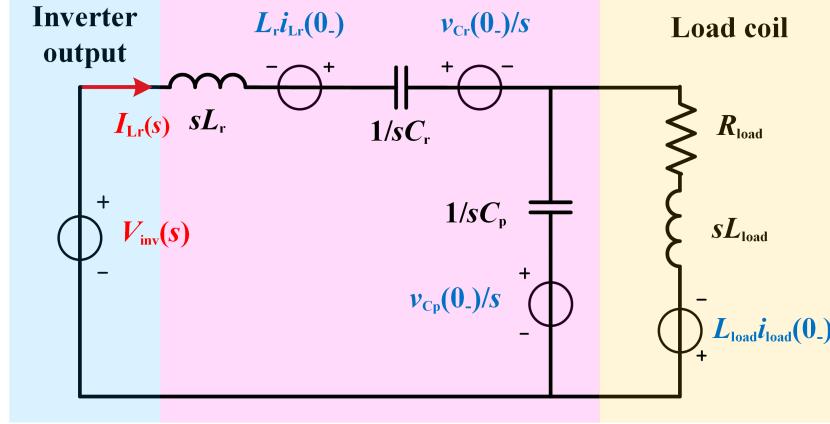
turn-on, and the ZVS turn-on can be achieved. However, the current amplitude at the first pulse is low and not enough due to the start-up transient. Therefore, the ZVS constraint 5.9 is not satisfied. From  $t_3$  to  $t_4$ , the inductor current charges the junction capacitance of S2/S3. The  $V_{ds}$  of S2/S3 does not reach full dc-link voltage ( $V_{dc}$ ) before the inductor current becomes zero. From  $t_4$  to  $t_5$ , the inductor current becomes negative and dis-charges the junction capacitance of S2/S3. Hence, the  $V_{ds}$  of S2/S3 slightly increases until the turn-on signal of S2/S3 comes. At  $t_5$ , S2/S3 turns on with high  $V_{ds}$  voltage. As a result, Phase 2 is a partial hard-switching process. This partial hard-switching process induces large  $V_{ds}$  overshooting, which may cause device overvoltage failure.

### 3. Phase 3 ( $t_6-t_7$ ):

The third switching process starts at the turn-off of S2/S3. Similarly, if the filter is close to the steady state, the inductor current at  $t_6$  will be sufficient to fully charge the junction capacitance of S1/S4 and the ZVS can be realized. In this way, the following switching process will also be ZVS. Otherwise, the partial hard-switching process continues until the filter has been charged enough energy.

In summary, the first switching process is zero current turn-on. Afterwards, the ZVS cannot be achieved at the initial switching transient due to the insufficient inductive current. Therefore, it is essential to implement a pre-charge strategy to eliminate the start-up hard-switching transition.

The filter equivalent transient circuit is depicted in Fig. 5.7. From the transient analysis, the inductor current ( $I_{Lr}$ ) can be expressed in s-domain as 5.19.



**Figure 5.7:** Equivalent Circuit of the Inverter Output Network.

$$\begin{aligned}
 I_{Lr}(s) = & \frac{V_{inv}(s) + L_r \cdot i_{Lr}(0_-) - \frac{v_{Cr}(0_-)}{s}}{sL_r + \frac{1}{sC_r} + \frac{1}{sC_p} // (R_{load} + sL_{load})} \\
 & + \frac{\frac{v_{Cp}(0_-)}{s}}{\frac{1}{sC_p} + (sL_r + \frac{1}{sC_r}) // (R_{load} + sL_{load})} \times \frac{R_{load} + sL_{load}}{(sL_r + \frac{1}{sC_r}) // (R_{load} + sL_{load})} \\
 & + \frac{L_{load} \cdot i_{load}(0_-)}{R_{load} + sL_{load} + (sL_r + \frac{1}{sC_r}) // \frac{1}{sC_p}} \times \frac{\frac{1}{sC_p}}{(sL_r + \frac{1}{sC_r}) // \frac{1}{sC_p}}
 \end{aligned} \quad (5.19)$$

where  $I_{Lr}(s)$  is the inductor current;  $V_{inv}(s)$  is the inverter output voltage;  $R_{load}$  represents the load resistance;  $L_{load}$  is the load inductance;  $i_{Lr}(0_-)$ ,  $i_{load}(0_-)$ ,  $v_{Cr}(0_-)$ ,  $v_{Cp}(0_-)$  are the serial inductor ( $L_r$ ) initial current, load initial current, serial capacitor ( $C_r$ ) initial voltage, parallel capacitor ( $C_p$ ) initial voltage, respectively.

All of the initial states are zero before implementing any pre-charge strategies. The pre-charge strategy is to change the initial states of the capacitance or inductance. It can be known from the analysis that making the inductor current ( $I_{Lr}$ ) increase faster after phase 1 is an effective way to eliminate the hard-switching. The initial load current and voltage before phase 1 should be zero as load requirement. Therefore,  $v_{Cp}(0_-) = i_{load}(0_-) = 0$ . The inverter output voltage is dc-link voltage between phase 1 and phase 2. Thus,  $V_{inv} = -V_{dc}/s$ . Equation 5.19 is rewritten as 5.20. From 5.20,

the denominator is fixed after the filter physical design is complete. The changeable parameters are the initial current of inductance ( $i_{Lr}(0_-)$ ) and the initial voltage of serial capacitance ( $v_{Cr}(0_-)$ ). The most effective way of increasing  $I_{Lr}$  is to make the initial voltage of serial capacitance ( $v_{Cr}(0_-)$ ) become a negative voltage. Thus, the pre-charge strategy is to turn on S2/S3 before phase 1. In this way,  $v_{Cr}(0_-) = -V_{dc}$ . The inductor current in time domain can be expressed as 5.21.

$$I_{Lr}(s) = \frac{\frac{V_{dc}}{s} + L_r \cdot i_{Lr}(0_-) - \frac{v_{Cr}(0_-)}{s}}{sL_r + \frac{1}{sC_r} + \frac{1}{sC_p} / (R_{load} + sL_{load})} \quad (5.20)$$

$$\begin{aligned} i_{Lr,new}(t) &= \mathcal{L}^{-1}\left\{\frac{2 \times \frac{V_{dc}}{s}}{sL_r + \frac{1}{sC_r} + \frac{1}{sC_p} / (R_{load} + sL_{load})}\right\} \\ &\Rightarrow = 2 \times i_{Lr,old}(t) \end{aligned} \quad (5.21)$$

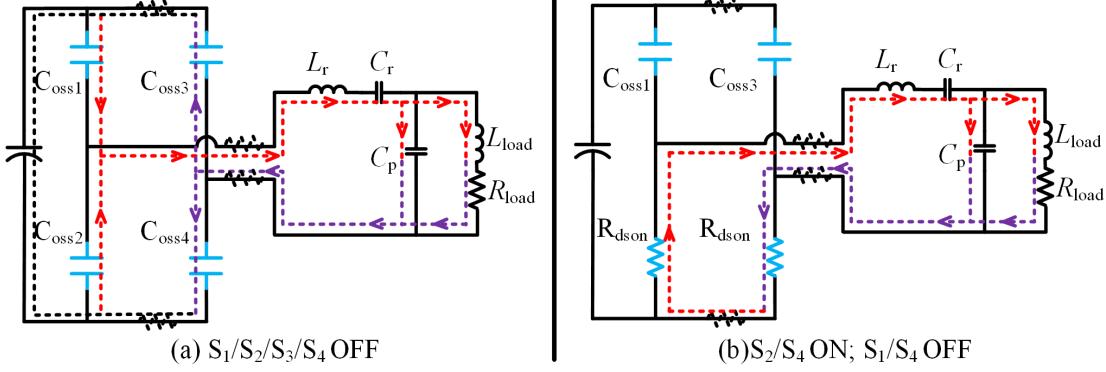
where  $i_{Lr,new}(t)$  and  $i_{Lr,old}(t)$  are the inductor current in time domain with and without pre-charge strategy, respectively.

Compared to the case without pre-charge strategy ( $v_{Cr}(0_-) = 0$ ,  $i_{Lr}(0_-) = 0$ ), the inductor current with pre-charge strategy is doubled. Fig. 5.6(b) demonstrates the start-up transient waveforms after implementing the pre-charge strategy. It should be noted that the first pulse is a little shorter than the following pulses. The reason is that the first switching process begins at  $V_{gs}$  turn-on signal. However, the following switching processes are ZVS, during which  $V_{ds} dv/dt$  starts at  $V_{gs}$  turn-off signal. This issue can be easily overcome by increasing the gate signal length of the first pulse.

### 5.3.2 Damping Method to Reduce the Oscillation Duration at the End of the Pulse

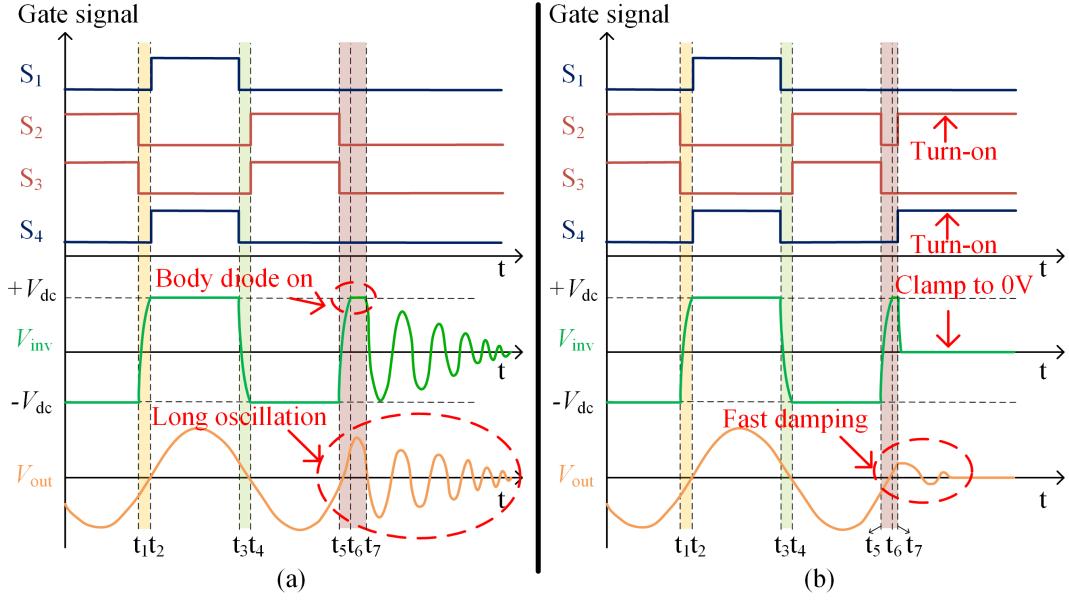
Different from 1.5 MHz continuous sinusoidal output, the EMAT sensor requires 3 to 5 pulses every 200 milisecond. Although the inverter can be turned off instantly at

the end of pulses, the load voltage presents long cycles of oscillation. It is because the energy stored in the passive filter continues to circulate between the devices' junction capacitances and filter networks.



**Figure 5.8:** The Oscillation Equivalent Circuit (a) Without Damping Strategy; (b) With Damping Strategy.

As shown in Fig. 5.8(a), after the inverter turns off, the devices are modeled as the junction capacitances ( $C_{\text{oss}}$ ). In Fig. 5.9(a), all the switches turn off at  $t_5$ . The filter residue energy oscillates between the filter and the junction capacitances. The energy can only be damped by the resonant loop parasitic resistance. If the residue energy is sufficient, it will discharge the junction capacitance to zero voltage and make the body diode of the device turn on, as  $t_5-t_7$  shown in Fig. 5.9(a). This will lead to additional equivalent switching operation of the inverter, making the ending transient oscillation longer. As mentioned before, the residue oscillation will affect the accuracy and the minimum thickness measurement capability of EMAT sensor. To address this challenge, a damping path is needed to diminish the filter remaining energy. This damping path is introduced by turning on both upper switches (S1/S3) or both lower switches (S2/S4), as shown in Fig. 5.8(b). The  $R_{\text{dson}}$  of SiC MOSFETs performs as the damping resistor. Because of the burst mode operation, the SiC MOSFET can be selected based on the device pulse current rating. Thus, the device  $R_{\text{dson}}$  can



**Figure 5.9:** Typical Waveforms of Ending Transient (a) Without Damping Strategy; (b) With Damping Strategy.

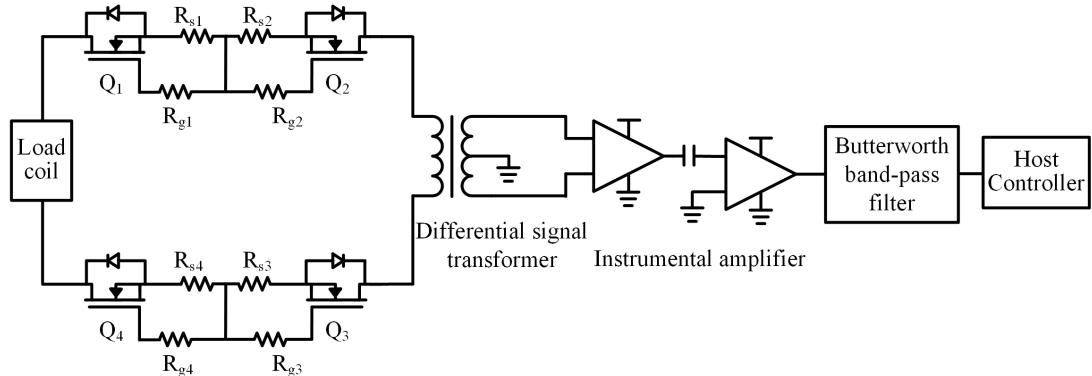
be relatively high. The typical waveforms with the proposed damping strategy are depicted in Fig. 5.9(b). After the last switching process ( $S_2/S_3$  turn-off), the  $S_2$  and  $S_4$  are turned on again to clamp the output voltage of the inverter at zero volt. Thus, the residue energy cannot stimulate additional equivalent switching pulses and can be damped fast by the resistive path. This damping method transforms the original uncontrolled oscillation state to a resistive damping state. As a result, the residue energy can be dissipated quickly. The effectiveness of this damping strategy will be validated in the experimental section.

### 5.3.3 Methods to Mitigate the Crosstalk Effect: Mis-trigger and Negative Overvoltage

During the switching transient, two risks of the device gate voltage failure have been found [86]. One is the  $V_{gs}$  mis-trigger during hard-switching transient (Phase

1). Another one is the negative  $V_{gs}$  overvoltage during ZVS soft-switching process. These two phenomena are so-called crosstalk effect [10, 11, 133]. In the burst mode operation, the first switching transient is hard switching at zero current. Afterwards, the switching transients are ZVS. The off-state gate voltage is usually set at -5 V to avoid the mis-trigger [10, 86]. The negative overvoltage issue is solved by adding fast clamping Schottky diode directly between the gate terminal and the gate voltage supply [22, 133]. Due to the parasitic inductance on the clamping path, the gate voltage cannot be clamped at the exact supply voltage level. However, at the switching speed level of this application, the gate negative overvoltage amplitude can be reduced to a safe range by the Schottky diode clamping. If the switching speed requirement is higher, the Schottky diode clamping method may not be sufficient and other cross-talk suppression methods [86] should be implemented.

#### 5.4 Echo Signal Receiving Circuit Design



**Figure 5.10:** The Schematic of the Receiving Circuit.

The receiving circuit is required to capture the microvolt echo signals sensed by the load coil. However, the load coil also contains the high voltage (kV) transmitting pulses. This high voltage transmitting pulses should be scaled down by the receiving

circuit to the echo signal level with small time delay. On the contrary, the receiving circuit should amplify the echo signals. By capturing the time length between the scaled-down transmitting signals and the receiving signals, the thickness can be calculated by 5.22. To curtail the high voltage transmitting pulses and to amplify the echo signals using a same circuit is a big challenge.

$$D_{\text{metal}} = \frac{1}{2}v \cdot \Delta T \quad (5.22)$$

where  $D_{\text{metal}}$  is the testing metal thickness;  $v$  represents the ultrasonic wave velocity in the testing metal;  $\Delta T$  is the time interval between the scaled down transmitting signal and the receiving echo.

#### 5.4.1 High Voltage Scale-Down Unit

The schematic of the receiving circuit is illustrated in Fig. 5.10. Four depletion MOSFETs with the part number IXTP 01N100D are used to block the AC high voltage pulses. The depletion MOSFET combined with a gate resistor and a source resistor (i.e.,  $Q_1-R_{s1}-R_{g1}$ ) can be used as a high-voltage curtailing and low-voltage conducting unit. In Fig. 5.10,  $Q_1$  is normally on. Initially, the voltage across the resistor  $R_{s1}$  is 0 V, hence, the gate to source voltage ( $V_{gs}$ ) of  $Q_1$  is 0 V. At zero  $V_{gs}$ , there will be current flowing through  $Q_1$ . If the receiving signal comes, the current ( $I_d$ ) is small because the receiving signal is in microvolt level. Thus,  $V_{gs}$  of  $Q_1$  is still near zero, far from the turn-off threshold voltage. The echo signals can pass through. When the high voltage is applied, there will be a current ( $I_d$ ) flowing in the circuit. Due to this current, there will be a voltage drop across the resistor  $R_{s1}$ , which in turn reduces  $V_{gs}$  of  $Q_1$  to a negative value, and  $Q_1$  will be in linear region. In this mode, the drain current ( $I_d$ ) is saturated and does not depend on  $V_{ds}$ . As a result, the high

voltage can be blocked. The current through  $Q_1$  is given by 5.23.

$$I_d = I_{dss} \cdot \left(1 + \frac{V_{gs}}{V_{gs,th}}\right)^2 \quad (5.23)$$

where  $I_d$  is the drain current of  $Q_1$ ;  $I_{dss}$  represents the drain current at  $V_{gs} = 0$ ;  $V_{gs,th}$  is the threshold voltage of  $Q_1$ .

The  $V_{gs}$  can be calculated by the voltage drop across  $R_{1s}$ , as expressed in 5.24.

$$V_{gs} = I_d \cdot R_{1s} \quad (5.24)$$

Based on 5.235.24, the  $R_{1s}$  can be designed to scale down the current level of the transmitting signals. The detailed operation principle of this depletion MOSFET is demonstrated in [131].

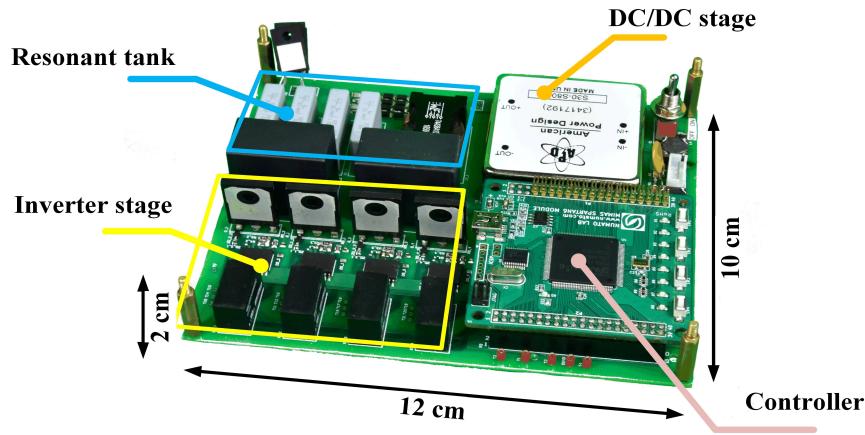
Because the circuit has to take the AC voltage, two depletion MOSFETs are anti-series to form a bi-directional blocking unit, as  $Q_1$  and  $Q_2$  shown in Fig. 5.10. However, the voltage rating of this depletion MOSFET is 1 kV, which is not sufficient to sustain the load voltage. Therefore, two anti-series units are placed at positive path ( $Q_1, Q_2$ ) and negative path ( $Q_3, Q_4$ ), respectively, to achieve 2 kV blocking voltage. This high voltage scale-down circuit is a conduction path when the load voltage is low. Thus, the microvolt echo signals can pass through.

#### 5.4.2 Echo Signal Amplification Circuit

To amplify the echo signals at microvolt level, the noise should be carefully dealt with. In order to remove the possible common mode noise from the main power board, a high bandwidth differential signal audio transformer with the part number PWB2010-1LB is placed between the high voltage blocking circuit and the amplification circuit. Moreover, two ultralow noise instrumentation amplifiers with the fixed

gain of 2000 are used to amplify the echo signals. Among abundant amplifier options, AD8428 of Analog Devices is selected, which compared to similar ICs has high gain, high bandwidth and low noise, simultaneously. The offset voltage drift is also an important parameter to be considered. It is because the amplitude of the original echo signals is in the range of the voltage drift level. Therefore, a DC blocking capacitor is placed between two amplifiers to block the offset voltage generated by the amplifier output. Last, a Butterworth band-pass filter is used to get the signals with the required frequency of the Host Controller.

## 5.5 Experimental Results Analysis



**Figure 5.11:** Pulser Prototype (Shielding Box Removed).

The SiC MOSFET with the part number C2M0080120D from Wolfspeed is used as the main power device to satisfy the voltage rating and pulse current rating. The dc-link capacitor is selected to meet the requirement of the dc voltage rating, 10% peak to peak voltage fluctuation and pulse current rating. The prototype without the EMI shielding box is shown in Fig. 5.11. The following experimental results include LCC filter performance evaluation, start-up and ending transient elimination

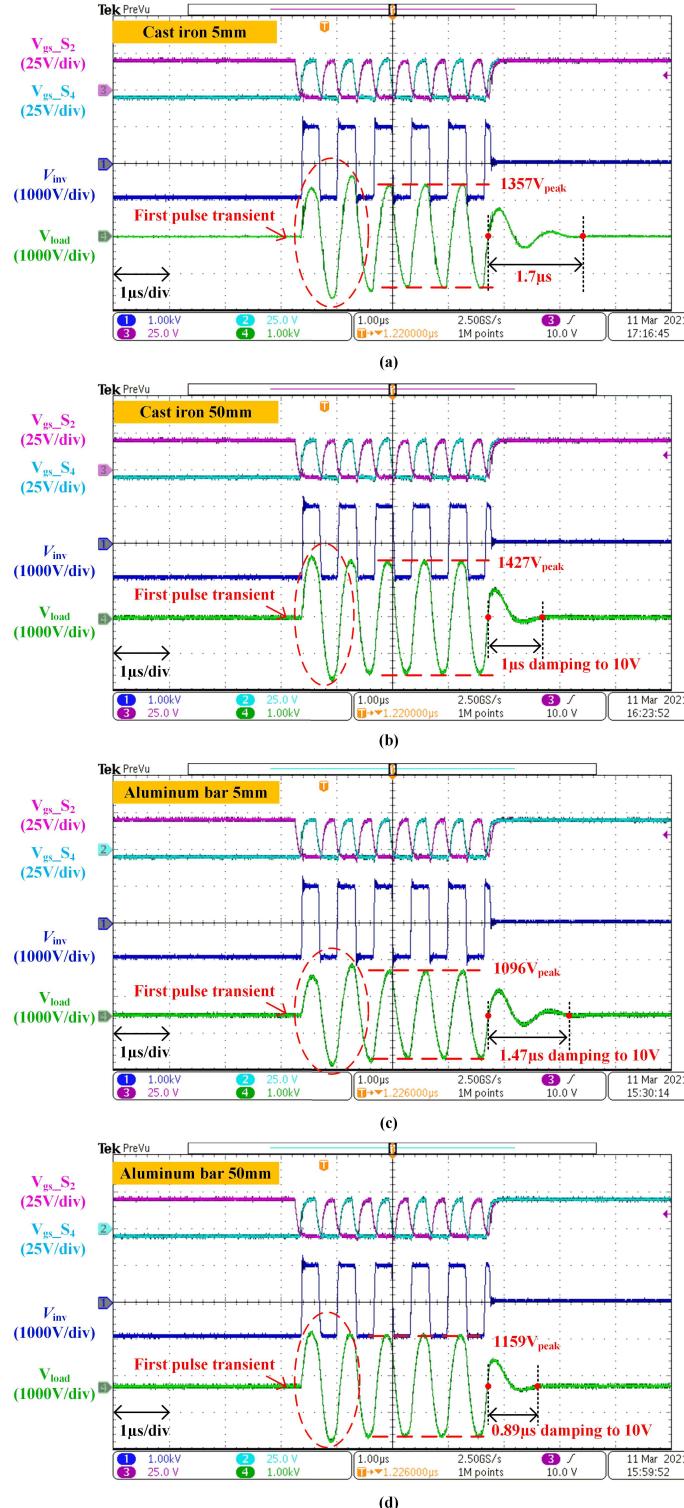
and receiving circuit validation.

**Table 5.4:** Typical Parameters of the Experimental Results.

Load Material	Cast iron		Aluminum	
<b>Thickness</b>	5mm	50mm	5mm	50mm
<b>Load parameters at operating freq. <math>\omega_0</math></b>	16.9 $\Omega$ +1.9 $\mu H$	24.1 $\Omega$ +3.2 $\mu H$	15.3 $\Omega$ +0.4 $\mu H$	21.7 $\Omega$ +0.6 $\mu H$
<b>Gain</b>	1.08	1.12	0.86	0.91
<b>THD (with first pulse)</b>	11.87%	11.57%	11.31%	10.64%
<b>THD (without first pulse)</b>	10.91%	9.84%	10.38%	8.22%
<b>ZVS</b>	YES	YES	YES	YES

### 5.5.1 LCC Filter Performance Evaluation

The LCC filter performance will be evaluated in terms of voltage gain, THD and ZVS soft-switching at lower and upper limits of the load range. Fig. 5.12 shows the experimental results. In this experiment, the dc-link voltage is 1000 V, and the switching frequency is 1.5 MHz. The first pulse has different amplitude from the following pulses because of the start-up transient. Although the pre-charge strategy is used, the first pulse is improved but cannot be identical with the steady state. The typical parameters are summarized in Table 5.4. The voltage gain is calculated based on FHA. The input voltage amplitude is  $1kV \times 4/\pi$ , which is derived by Fourier series of the square wave. The voltage gain at different extreme load conditions are within the range of 0.8-1.2. The data of the output voltage is imported into MATLAB, and the THD is calculated by the FFT analysis tool in SIMULINK. The THD including all five pulses is bigger than the THD without first pulse. It is because different amplitude



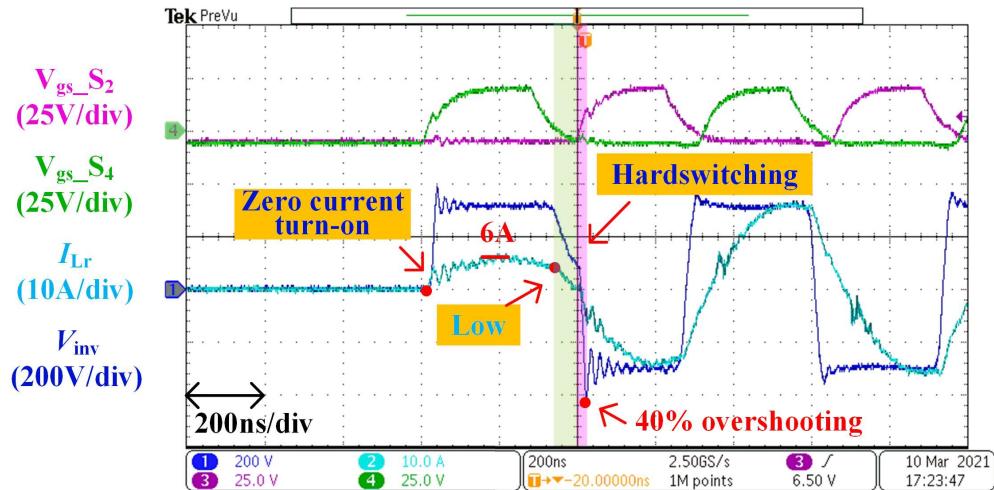
**Figure 5.12:** Typical Waveforms Under Four Extreme Load Conditions: (a) Cast Iron 5 mm; (b) Cast Iron 50 mm; (c) Aluminum Bar 5 mm; (d) Aluminum Bar 50 mm.

of the first pulse results in different level of harmonics. The biggest THD without first pulse are 10.91%, which is a little smaller than the theoretical optimization result. It is because there are deviation between the physical parameters and the theoretical parameters of the resonant components. Lastly, the ZVS is achieved after the first switching process. Due to the ZVS switching, the  $V_{ds}$  overshooting voltage keeps below 11%. Therefore, the LCC filter design and optimization method considering inductive load conditions are verified.

### 5.5.2 Transient Mitigation Strategy Verification

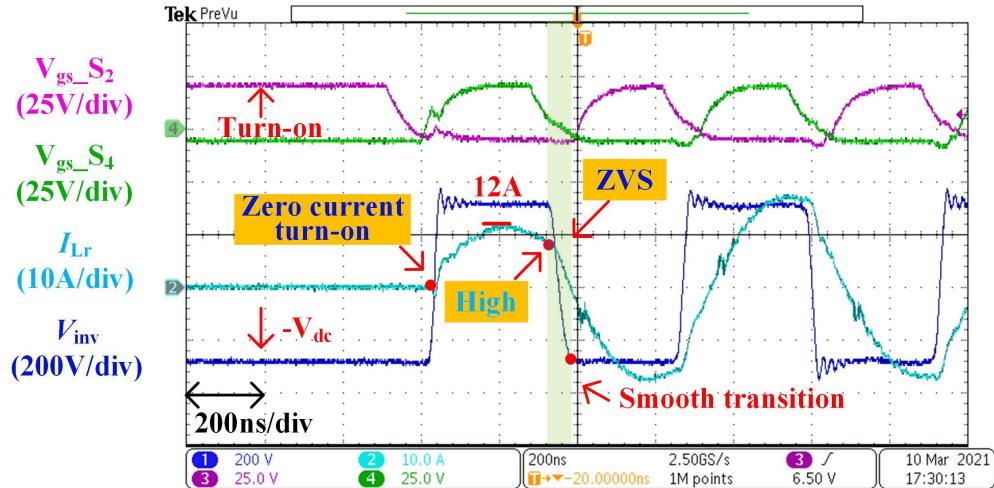
The transient mitigation includes start-up transient, pulse ending transient and crosstalk. The corresponding comparative experiment is conducted at the same load condition to verify the proposed strategy.

#### 1) Pre-charge Strategy Verification



**Figure 5.13:** Start-up Transient Without Proposed Pre-charge Strategy.

Without the proposed pre-charge strategy, the partial hard-switching occurs at the second switching process, as shown in Fig. 5.13. For the first pulse, the invert-

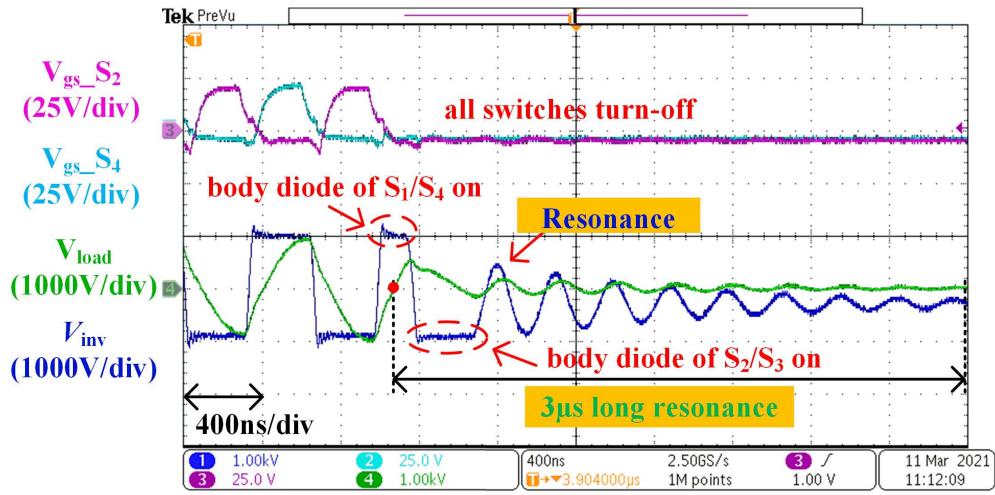


**Figure 5.14:** Start-up Transient With Proposed Pre-charge Strategy.

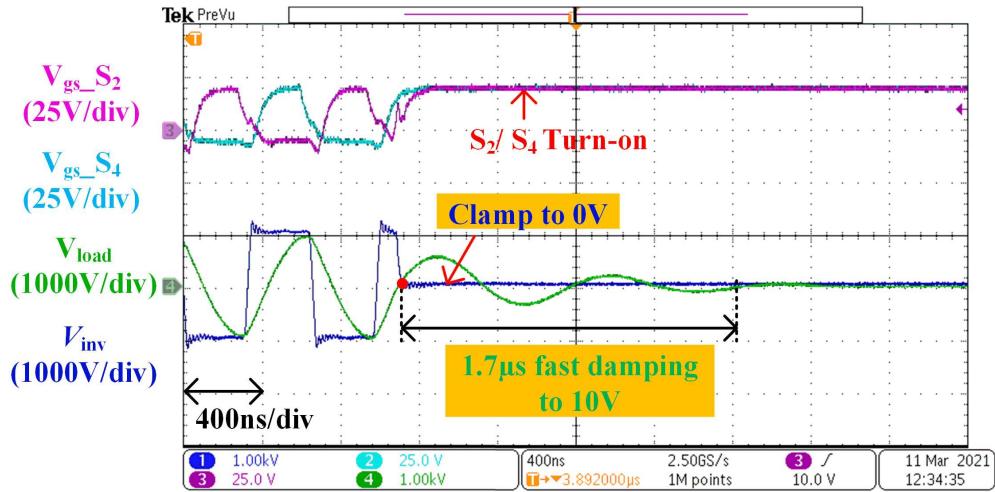
er output current ( $I_{Lr}$ ) at turn-off process is low and insufficient to fully discharge the junction capacitance. Therefore, the hard-switching process happens after the inverter output current decreases to zero. This hard-switching process results in 40% voltage overshooting. After the pre-charge strategy is implemented (shown in Fig. 5.14), the S2 and S3 are turned on in advance of the first pulse. The first switching process is still zero current hard turn on, and the second switching process achieves ZVS. It is because the pre-charge strategy makes the inverter output current doubled during first half cycle (peak current from 6 A to 12 A). As a result, the inverter output current ( $I_{Lr}$ ) is sufficient to discharge the device junction capacitance to zero volt before turn-on. After second switching process, all the following pulses are switched at ZVS.

## 2) Pulse End Damping Strategy Verification

For the pulse ending transient, the time from the pulse end to the load voltage amplitude dropping to 10 V is taken as the evaluation criterion. If all the switches are turned off at the pulse end, the inverter output voltage ( $V_{inv}$ ) oscillates several cycles.



**Figure 5.15:** Ending Transient Without Proposed Damping Strategy.



**Figure 5.16:** Ending Transient With Proposed Damping Strategy.

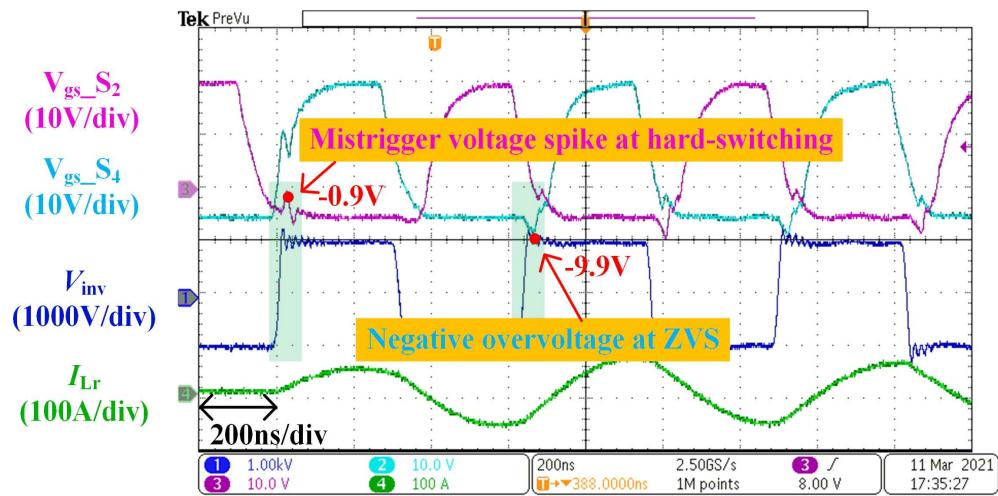
At the beginning of the oscillation in Fig. 5.15, the resonant voltage can reach dc-link voltage. During this time, the body diodes of diagonal switches are forward biased to clamp the inverter output voltage at dc-link voltage. This phenomenon is similar as the additional switching process, increasing the oscillation time. Meanwhile, the resonant frequency is higher when all the switches are off. It is because the device junction capacitance is in the resonant loop. However, since the damping resistance in the resonant network is the loop parasitic resistance, the damping time is long. It takes  $3 \mu\text{s}$  for the load voltage amplitude dropping to 10 V. After implementing the proposed damping strategy at the same operation condition, the S2 and S4 are turned on after the pulse end, as shown in Fig. 5.16. The inverter output voltage is clamped to 0 V, and the oscillation loop is the resonant filter loop. Thus, the oscillation frequency is smaller than that without the damping strategy. In addition, the oscillation amplitude decreases faster, because the damping resistance in the oscillation loop includes on-state resistance of S2 and S4. As a result, the load voltage decreases to 10 V within  $1.7 \mu\text{s}$ .

### 3) Crosstalk Suppression Performance

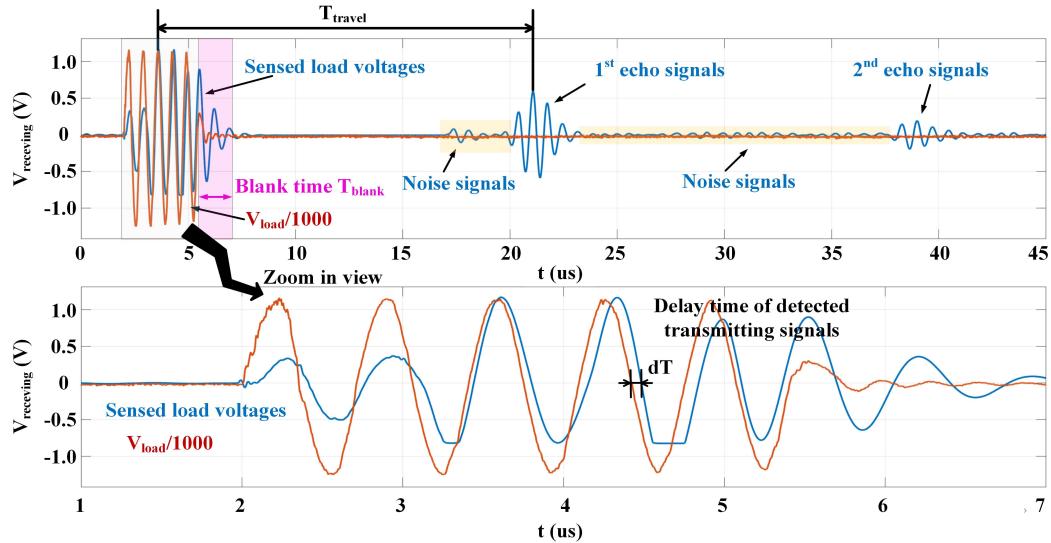
The crosstalk suppression performance is evaluated at full power. The experimental results are shown in Fig. 5.17. For the first switching process, the potential mis-trigger voltage spike reaches -0.9 V. The value is smaller than the device turn-on threshold voltage. For ZVS of the following switching process, the negative overvoltage reaches -9.9 V, which is also in the safe operation region of SiC MOSFETs.

#### 5.5.3 Receiving Circuit Validation

The signals after conditioning of the receiving circuit and the original transmitting load voltages are shown in Fig. 5.18. The load voltage (red) is divided by one thousand to fit the scale of the receiving signals (blue). The sensed load voltage is



**Figure 5.17:** Performance of the Crosstalk Suppression Methods.



**Figure 5.18:** Typical Scale-down Transmitting Signals and the Amplified Echo Signals by the Receiving Circuit.

curtailed from thousand volts level to one volts level. The THD of the transmitting load voltage is low. Therefore, the amplitude of the noise signals are below 0.1 V. The signal-to-noise ratio of the receiving signal is bigger than 63.4 dB, which makes it easy for the extraction of the echo signals.

It should be noted that the receiving circuit introduces time delay (*delayT*) of the sensed load voltage (blue). According to 5.22, the actual thickness ( $D_{\text{metal,actual}}$ ) and the measured thickness ( $D_{\text{metal,measured}}$ ) of the testing metal are expressed in 5.25 and 5.26, respectively. The time delay represents system measurement error. The error can be expressed as 5.27. This error can be compensated in advance through the software. The test results of four different loads are listed in Table 5.5.

**Table 5.5:** Measurement Data of Receiving Circuit Under Four Different Loads.

Material	Thickness/mm	delayT/ $\mu s$	$T_{\text{travel}}/\mu s$	$\varepsilon$	$T_{\text{blank}}/\mu s$
Cast iron	50	0.07	17.5	0.40%	1.0
	5	0.07	1.75	4.00%	1.7
Aluminum bar	50	0.07	17.2	0.41%	0.89
	5	0.07	1.73	4.07%	1.47

$$D_{\text{metal,actual}} = v \cdot \frac{T_{\text{travel}}}{2} \quad (5.25)$$

$$D_{\text{metal,measured}} = v \cdot \frac{T_{\text{travel}} + \text{delay}T}{2} \quad (5.26)$$

$$\varepsilon = \frac{\text{delay}T}{T_{\text{travel}}} \times 100\% \quad (5.27)$$

Moreover, the blank time after the pulse is only  $1.7 \mu\text{s}$  at the worst-case. Thus, the minimum traveling time is the sum of the pulse duration ( $T_{\text{pulse}}$ ,  $3.3 \mu\text{s}$  for 5 pulses of  $1.5 \text{ MHz}$ ) and the blank time ( $T_{\text{blank}}$ ,  $1.7 \mu\text{s}$ ). If the metal material is known, the travelling speed ( $v$ ) and the minimum measurement thickness ( $D_{\min}$ ) of the certain metal can be obtained, as presented in 5.28.

$$D_{\min} = v \cdot \frac{T_{\text{pulse}} + T_{\text{blank}}}{2} \quad (5.28)$$

## 5.6 Conclusions

This chapter proposes a LCC resonant inverter for the EMAT sensor application. The SiC MOSFETs are used to meet the high amplitude (kV) and high frequency (MHz) load voltage requirement. Meanwhile, it achieves low THD, ZVS switching and relatively stable voltage variation range within a wide load range. The traditional resonant filter design is based on the resistive load condition. However, in EMAT application, the load is inductive. Therefore, the resonant filter design methodology and optimization guideline are proposed for the inductive load. The ‘modified Q-factor’ method is innovated for the non-resistive load condition. The multiobjective optimization method is demonstrated for the filter design. Different from the continuous operation, the thermal stress of the burst mode operation is not critical. Thus, the physical design of the filter components has its own uniqueness. The resonant inductor and capacitor design considerations in the burst mode operation are summarized in this chapter. The proposed design methodology and design considerations can be extended to other burst mode applications. Another special issue in the pulser is the pulse start-up and ending transient. The start-up transient influences the soft-switching performance and the sensor measurement accuracy. The ending oscillation affects the minimum thickness measurement capability. By changing the

switching states before and after the pulses, the start-up partial hard-switching process is eliminated, and the pulse ending oscillation is damped effectively. In addition, to attenuate the high amplitude transmitting voltage and to amplify the micro-volts echo voltage simultaneously, an advanced signal conditioning circuit is designed. By utilizing depletion mode MOSFETs, the transmitting voltage is effectively curtailed to microvolt level. Meanwhile, the receiving circuit amplifies the receiving signals by thousand times. Finally, the LCC filter design and the transient elimination methods are verified by experimental results under four worst-case load conditions. It can achieve the voltage of 1 kV at 1.5 MHz, which is twice of the state-of-the-art solution. When the load changes in a large range, the worst-case THD of the load voltage is around 10%, which is 20%-30% lower than the state-of-the-art solution. The residue voltage of the ending pulse is attenuated from 1 kV to 10 V within 1.7  $\mu$ s.

## Chapter 6

### CONCLUSION AND FUTURE WORK

The philosophy of replacing conventional Si devices with WBG devices is an ongoing trend. However, realizing the full potential of WBG semiconductor devices is very challenging due to its high slew rates and high sensitivity to the parasitics. This report investigates some of the emerging applications of WBG power devices. The topics of WBG based converter covered in this report include crosstalk effect, monolithic integration of power devices, series connected WBG devices, protection, high frequency magnetics and resonant filter design. The different gate driving techniques are proposed to solve these issues.

To suppress the crosstalk effect, this report introduces a smart self-driving multi-level gate driver. Using original  $V_{gs}$  with simple RC delay as control signal of the auxiliary circuit, the proposed SMGD has following advantages over the other crosstalk suppression techniques: 1. No additional control signals; 2. No additional dc/dc power supply and signal isolation stages for the auxiliary switch; 3. Easy to be implemented on the commercial gate driver IC. A SMGD based on the commercial gate driver ADuM4135 is developed. This method is easy to be implemented in the gate driver IC. The future work of this crosstalk suppression is to integrate this self-driving circuit into the gate driver IC.

To further increase the power density of the converter, monolithic integration of power devices and its control logics are preferred. Due to the lateral structure of GaN HEMTs, the integration of power switches, protection circuit, gate driver and logic circuit is convenient for GaN HEMTs. However, the integration of power switches

is challenging because of the substrate bias induced  $R_{dson}$  degradation. To address this issue, several methods are investigated, including substrate bias manipulation, passive components insertion between substrate and ground, and current injection from gate. Finally, a three level gate driver is implemented with P-N junction inserted between substrate and ground. This combined strategy significantly improves the conductivity of the high-side channel. The findings of this research provide some promising methods for solving this issue from the perspective of semiconductor technology. The future work will focus on the semiconductor solutions of this issue, such as thicker buffer, buffer quality improvement, or high current resistant gate material.

Another hot topic of WBG devices is the serial connection of the WBG devices. Chapter 4 investigate the voltage balancing issue and the short-circuit protection issue of series connected SiC MOSFETs. A current mirror based current source gate driver with active control scheme and high bandwidth protection circuit is proposed to address these two issues. Due to the high dynamic response and high resolution of the proposed current source gate driver, the voltage balancing issue under both soft-switching scenario and hard-switching scenario is solved properly. Besides the traditional high-inductance and low-inductance short circuit scenarios, the failure of single device among the serial devices can also cause overcurrent or overvoltage failure of the serial string. The proposed short-circuit protection method can cover all the short-circuit scenarios of series connected devices. The proposed short-circuit scheme is implemented in the proposed current source gate driver with soft turn-off function. The response time of the proposed short-circuit protection method is within 300 ns, which is sufficient to protect the high speed WBG device string. The future work about the CSGD is to improve the power density and to compare with the commercial voltage source gate driver.

A 1.5 MHz/1 kV/80 A pulse power inverter is developed using SiC MOSFETs. The high frequency resonant tank design methodology is illustrated. Moreover, the practical design considerations of capacitors and inductors in the WBG converter are discussed. A practical transient state analysis method is proposed to cope with the start-up and ending transient issues of WBG based inverters. Compared to the state-of-the-art pulse inverter, the designed inverter has low output THD with higher power density and smaller box volume. The crosstalk, EMI, fault protection, PCB layout of gate loop and power loop and other engineering design considerations are also investigated. In the future, the 24 V to 1 kV high boost ratio isolated dc/dc stage of this product should be optimized, and the cost should be lowered.

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