Electrical Subsystem

Digital Circuits using Verilog

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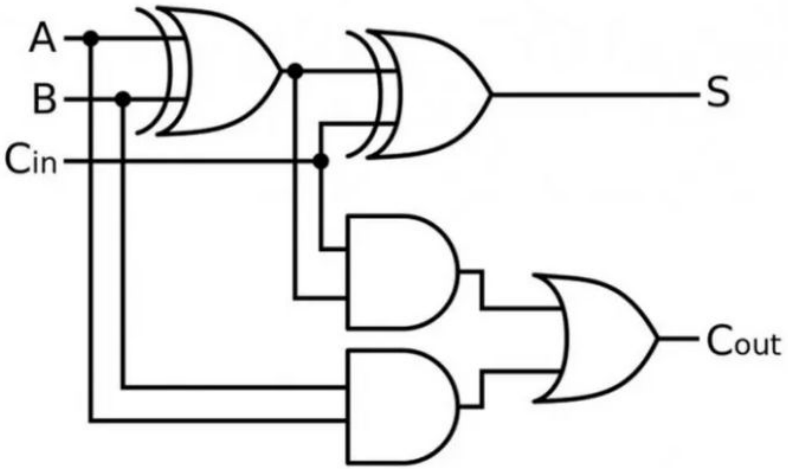
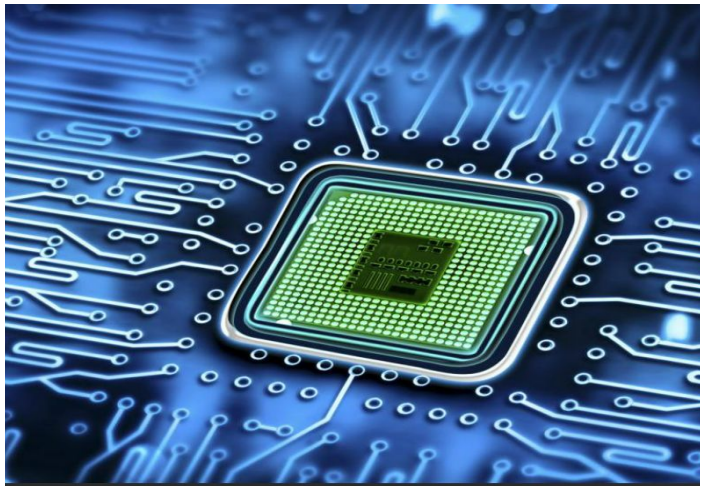
Co-Mentor: **Tanmay**

Verilog:

A Hardware Description Language (HDL) to describe digital circuits.



Simple Digital Circuit

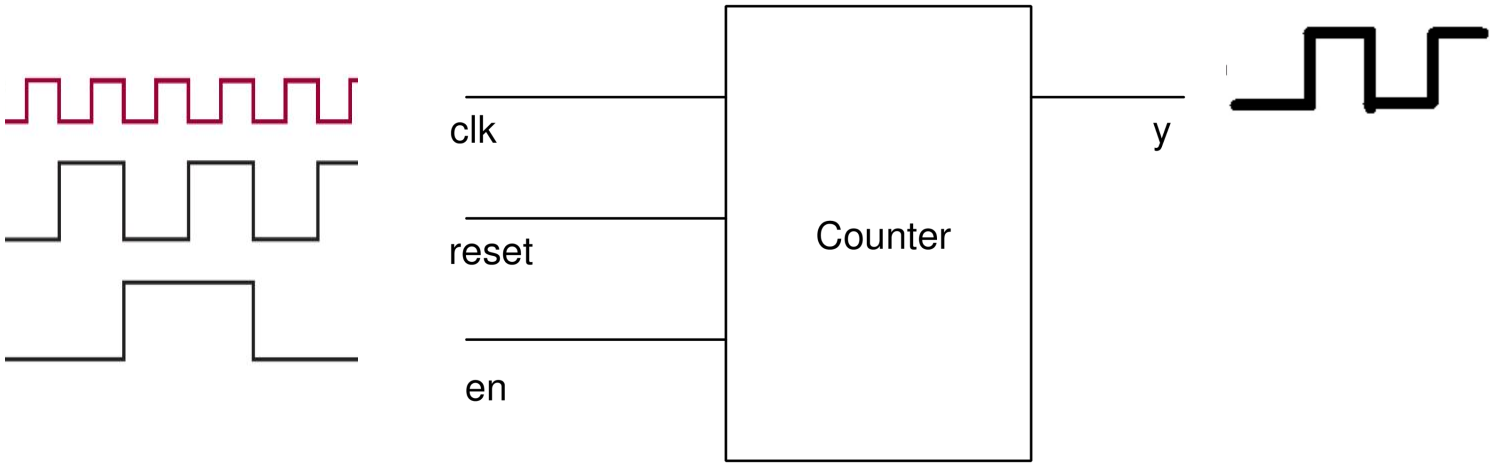


Aim:

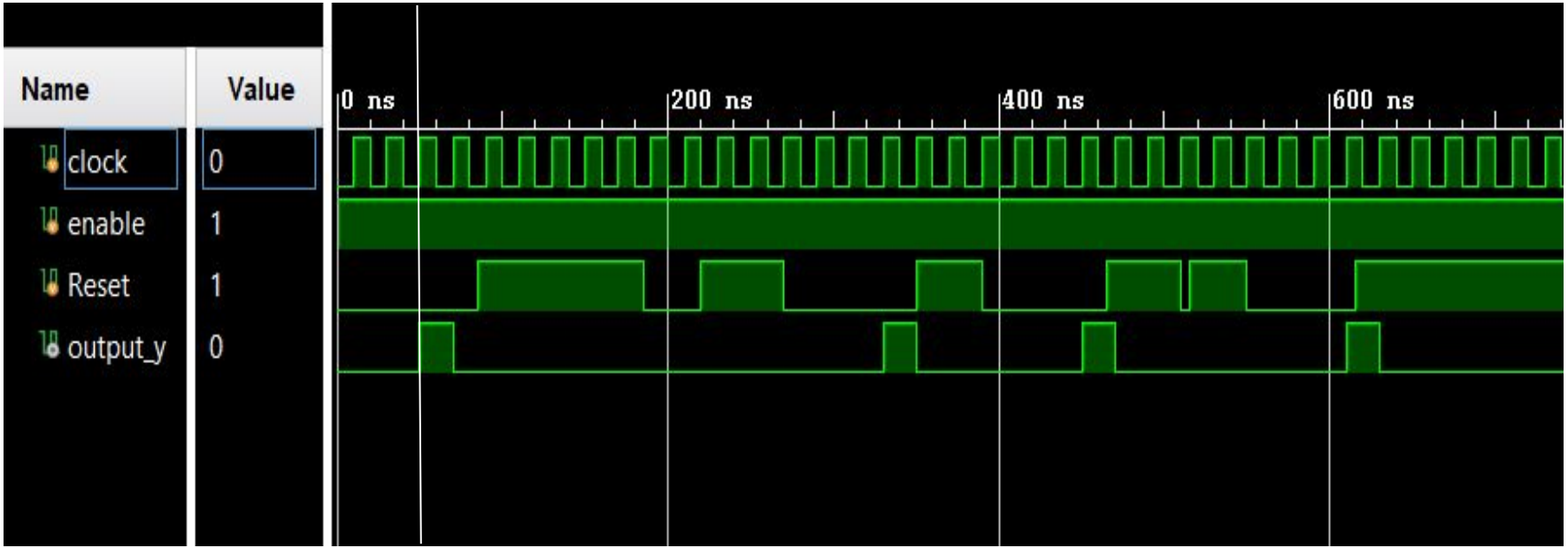
To learn Verilog(HDL), implement a simple circuit
& to solve a problem using the simple circuit

Part-A:

To design a mod-n counter in Verilog



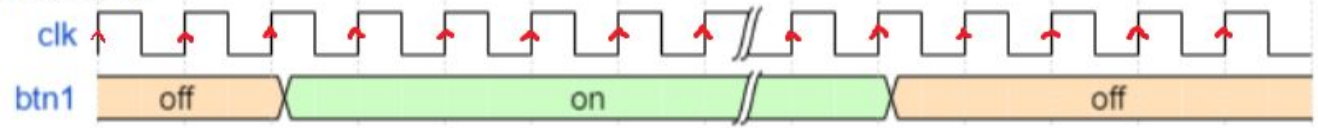
Mod-n counter:



Part-B:

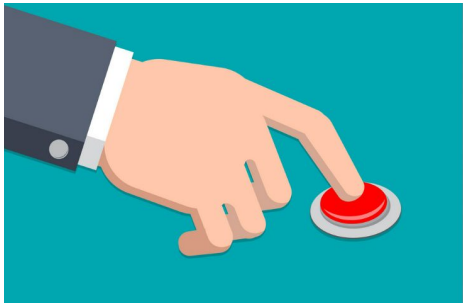
To solve a design problem

Waveform:

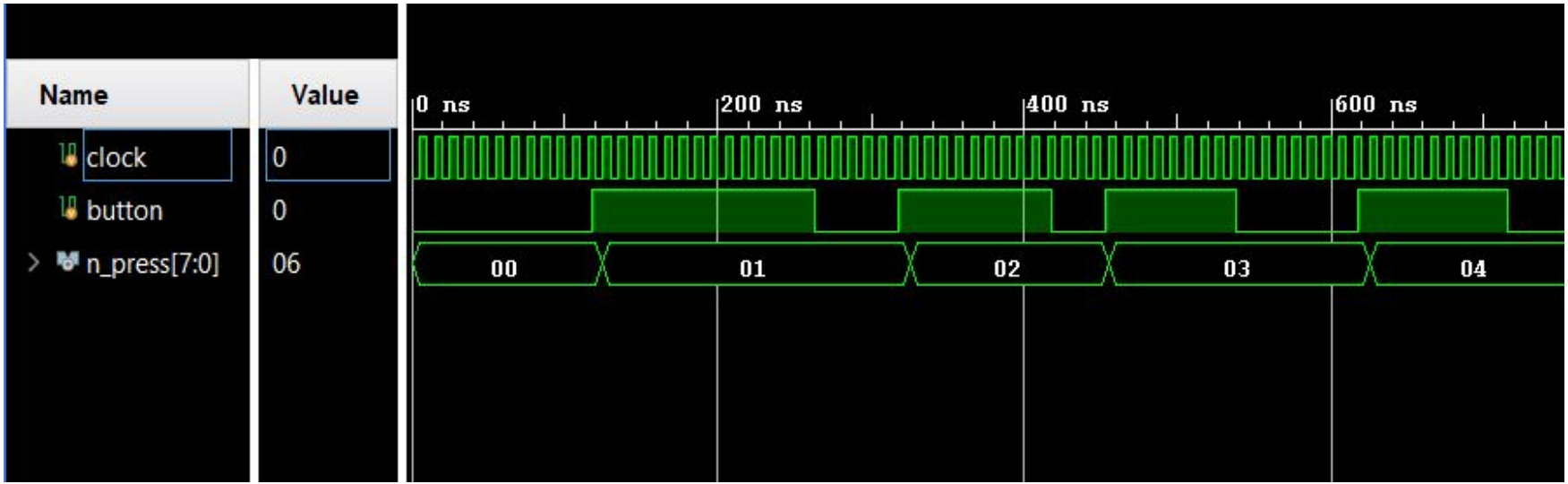


NOTE: The split in waveform here is used to indicate that it repeats for a long period of time.

- Circuit registers multiple button presses for a single press

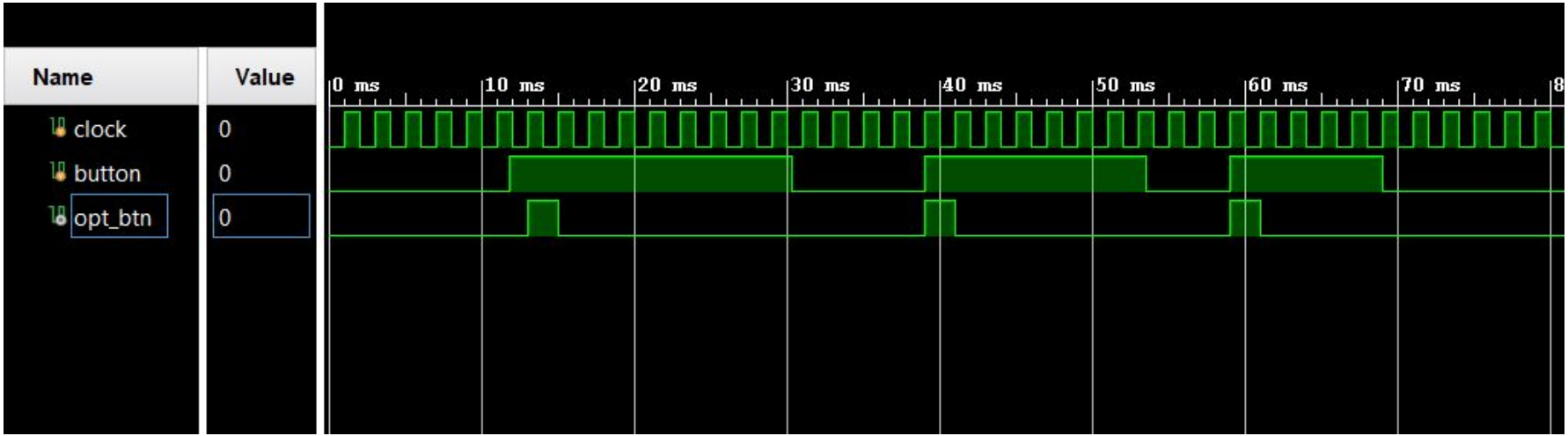


Counting no.of button presses



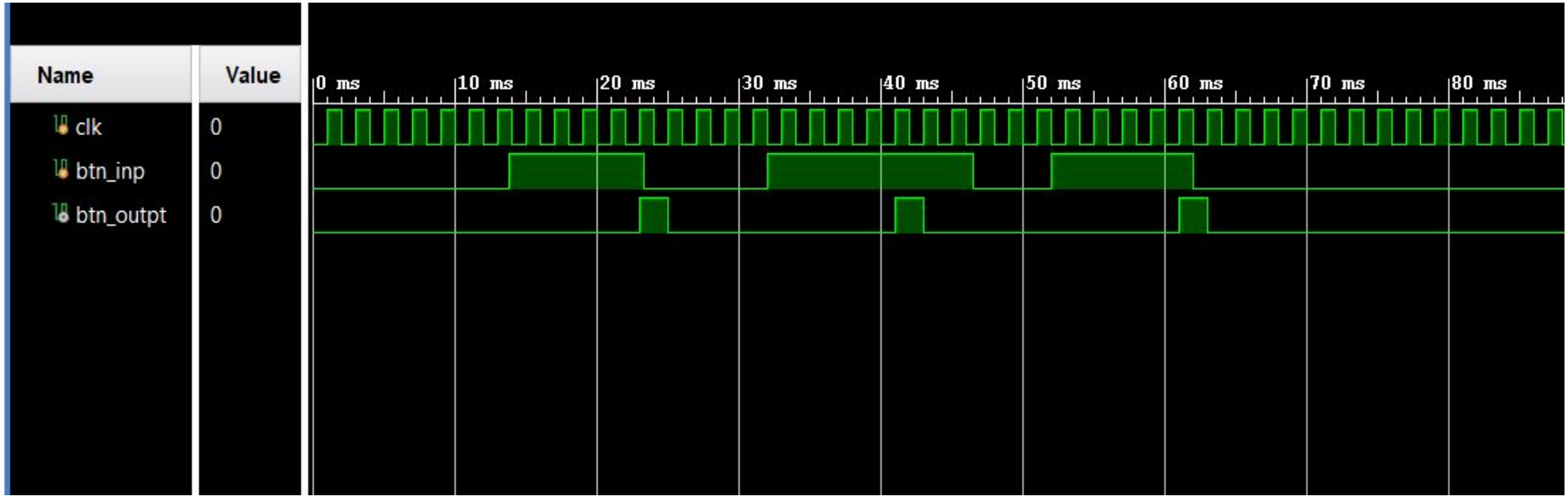
*Checks prev & present value of btn & increases count

Button Output (without Mod-n counter)

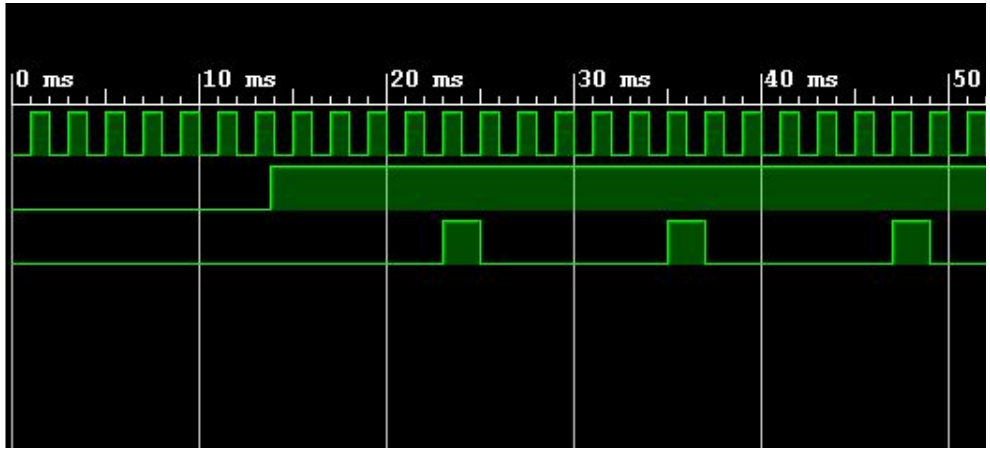


*Checks prev & present value of btn

Button Output (using Mod-n counter)

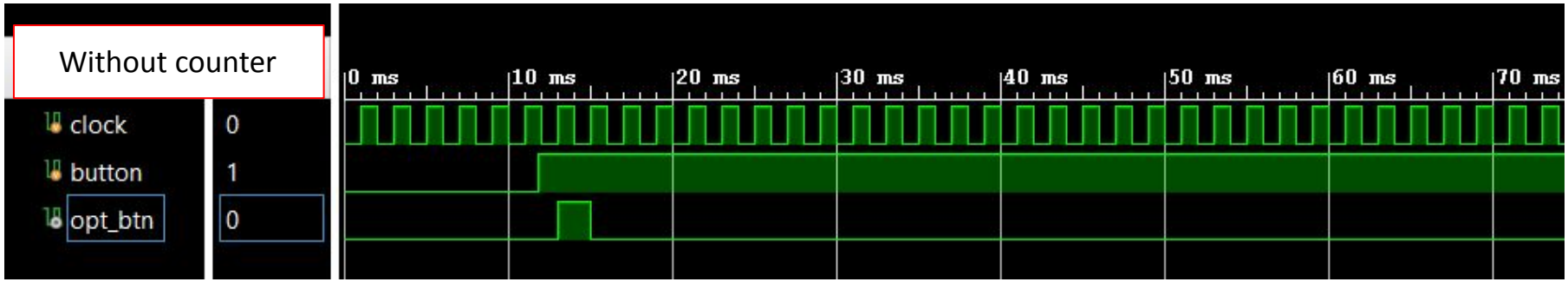


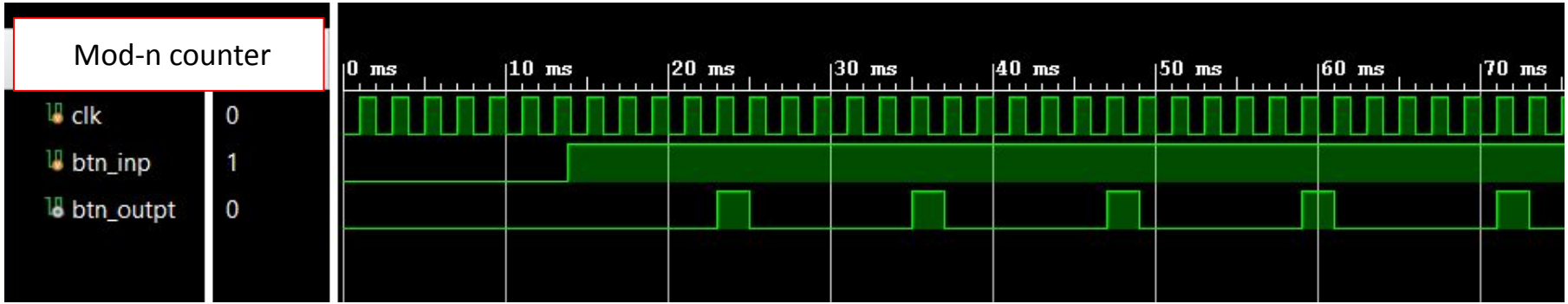
If a person intentionally press the button for long time how will it return output?



Multiple photos for one click

A long button press





Week1

- Started with Verilog
- Installed Vivado software
- Ref: https://www.nandland.com/verilog/tutorials/index.html

Verilog Tutorials

- Introduction To Verilog for beginners with code examples
- Always Blocks for beginners

- Your First Verilog Program: An LED Blinker
- Recommended Coding Style for Verilog

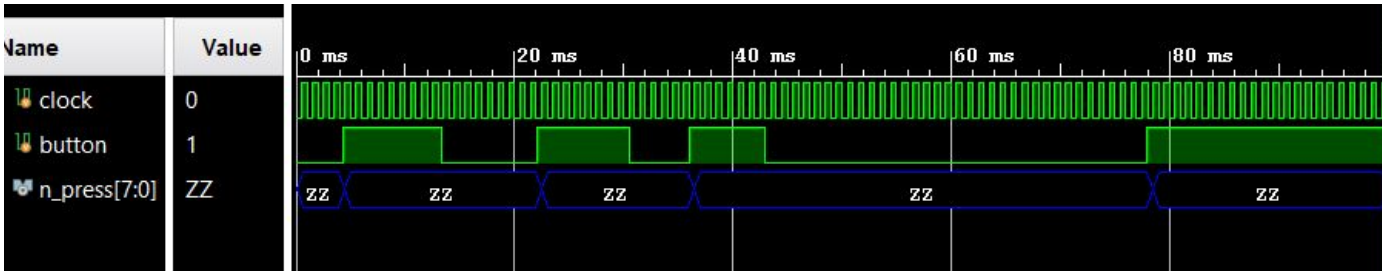
Week 2&3

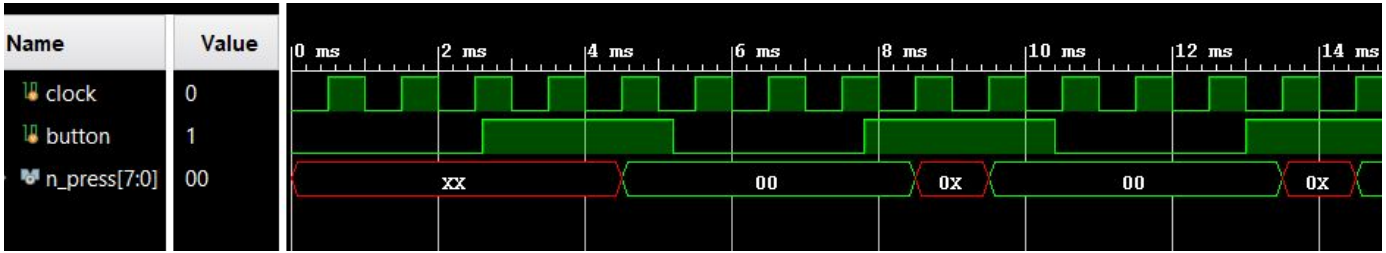
- Finished the counter description
- Found potential solution for design problem

**Verilog description of above problems:*
https://drive.google.com/drive/folders/1EcUGWLFiv1lnILN0XWHiXGRrb1gPZbTi?usp=sharing

Simulation Errors:

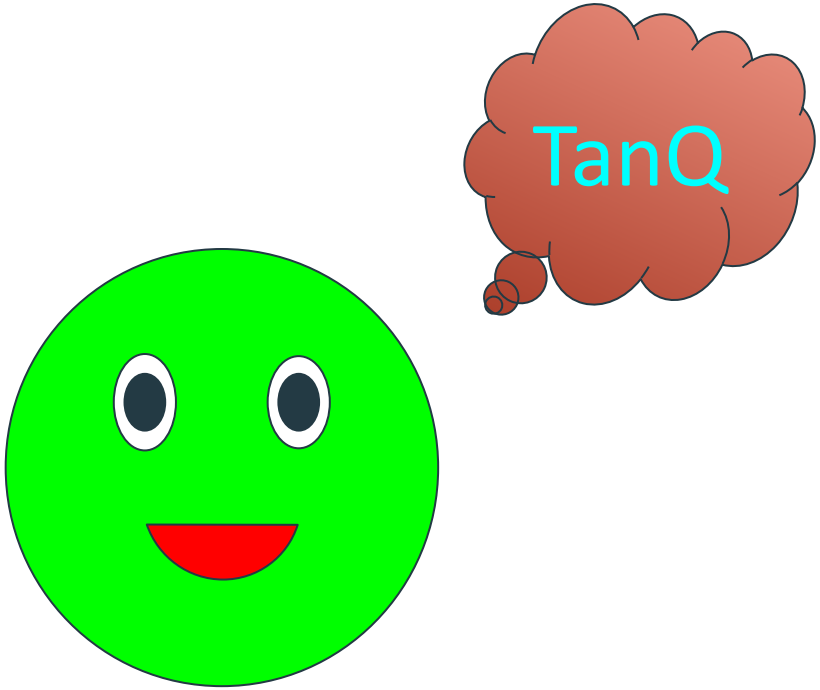
[Vivado 12-4473] Detected error while running simulation. Please correct the issue and retry this operation.






TEAMWORK

Time Management


TanQ