Company :	**NVIDIA**
Company Name :	**NVIDIA**
Nature Of Business :	**Semiconductor**
Designation :	**Hardware Intern**
Tentative Job Location :	Bnagalore

Description :

GPU ARCHITECTURE TEAM

GPU architecture team is engaged in the development of industry leading high performance and power efficient GPUs.

Specific areas include architecture modeling, analysis and performance verification. The team works on GPUs across all application domains such as gaming for PC and mobile devices, professional graphics & visualization and high-performance computation.

Skills you will use/develop:

- **C++ modeling, test development**
- **RTL design, debug**
- **ASIC design & verification tools, methodologies**
- **Computer architecture, Graphics, GPU micro-architecture, parallel computing**
- **Performance evaluation, analysis and debug**
- **Perl/Python scripting**

Areas you will be working on:

COMPUTER ARCHITECTURE; MEMORY SYSTEMS ARCHITECTURE, COMPILER ARCHITECTURE/ PERFORMANCE MODELING

GPU ASIC DESIGN / VERIFICATION TEAM

Today NVIDIA’s GPUs simulate human intelligence, running deep learning algorithms and acting as the brain of super computers, robots, and self-driving cars that can perceive and understand the world We are seeking a passionate, innovative, and highly motivated senior verification engineer to join us in the development of the next generation of PCI Express controllers used in NVIDIA's GPUs and SOCs In this position, you will be responsible for verification of the ASIC design, architecture and micro architecture using advanced verification methodologies You are expected to understand the design and implementation, define the verification scope, develop the verification infrastructure and verify the correctness of the design You will be working with architects, designers, pre and post silicon verification teams to accomplish your tasks

What you’ll be doing

- **Develop test plans, tests and verification infrastructure for PCIE at IP/sub system/SOC level**
- **Create verification environment using UVM methodology**
- **Create reusable bus functional models, monitors, checkers and scoreboards**
- **Drive functional coverage driven verification closure**
- **Work with architects, designers and post silicon teams**

Ways to stand out from the crowd

- **Good knowledge of PCIE protocol Gen 3 and above**
- **Good debugging and problem-solving skills**
- **Good communication skills and ability desire to work as a team player**

TEGRA SOC DESIGN & VERIFICATION

Tegra ASIC team (Design Verification)

As a Hardware Engineer at NVIDIA you will design and implement the industry's leading Graphics, Video and Mobile Communications Processors. Specific areas include 2D and 3D graphics, mpeg, video, audio, network protocols, high-speed IO interfaces and bus protocols, and memory subsystem design. You will be responsible for Architecture and micro-architecture design of the ASICs, RTL design and synthesis, Logic and Timing verification using leading edge CAD tools and Semiconductor process technologies

Areas you will be working on:

- **ASIC, RTL, DESIGN AND VERIFICATION OF PROCESSORS**
- **Low Power verification**
- **Power Estimation and Modeling**
- **PCIe Design verification**
- **Functional / Formal verification**

CPU VERIFICATION TEAM

As a design and verification/validation engineer in the ARM CPU team, you will be working on the next generation of 64bit ARM CPUs and SOCs. As part of this assignment the intern will get a chance to learn about computer architecture at a very granular level, System Verilog, Design Verification, SOC Verification, Verification methodologies and C/C++ programming. The intern also will get an opportunity to get familiar with industry standard tools in verification and validation. During the course of the internship, the intern will contribute to building test benches, developing architectural simulators, modifying random instruction generators and creating stimulus for verification and validation of different units of the CPU and SOC.

Areas you will be working on

- **Computer Architecture**
- **Digital Design and Programming in C/C++/Perl**
- **ARM, CPU Design and Verification/ Validation**

Eligibilty :

Program	AE	BSBE	CE	CHE	CSE	EE	ES	ME	MSE	PHY	CHM	MTH	ECO	DES	IME	HSS
BT-BS	No	No	No	No	No	Yes	No	No	No	No	No	No	No	--	--	--
MT	No	No	No	No	No	No	No	No	No	--	--	--	--	--	No	--
DoubleMajor	No	No	No	No	No	Yes	No	No	No	No	No	No	No	--	--	--
dual	No	No	No	No	No	Yes	No	No	No	No	No	No	No	--	--	--
dualB	No	No	No	No	--	--	--	No	No	No	No	No	No	--	No	--
dualC	--	--	--	--	--	--	--	--	--	--	--	--	--	--	No	--
Mdes	--	--	--	--	--	--	--	--	--	--	--	--	--	No	--	--
MBA	--	--	--	--	--	--	--	--	--	--	--	--	--	--	No	--
Phd	No	No	No	No	No	No	No	No	No	No	No	No	No	--	--	No
Msc	--	--	--	--	--	--	--	--	--	No	No	No	No	--	--	--
MSR	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

Stipend per month :	**INR 50,000 per month**
Other Facilities Offered :	**Accommodation + to and fro travel (provided its not virtual internship)**
Bond :	**False**
CPI CutOff :	**0.0**
Medical Requirments :	
Resume Shortlist :	**True**
Resume Shortlist Criteria:	**N/A**
Aptitude Test:	**True**
Aptitude Test Duration:	**30 mins**
Group Discussion:	**False**
Technical Test:	**True**
Technical Test Duration:	**30 mins**

Technical Interview:	**True**
Technical Interview Duration:	**1 hour**
Number of Techincal Interview Rounds:	**1**
HR Interview:	**False**
Additional Information:	