Joshua Mathew

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Objective

A quick learning Electrical Engineering and Applied Math double major with experience working in **research and industry**. Primary interests are Digital Signal Processing, Applied Computing, and Hardware Engineering. Seeking a position with a merger of mathematics and electronics, unique problems to solve, and engaging work culture.

Education

University of California, Los Angeles (UCLA) CGPA:3.78
B.S. in Electrical Engineering and B.S. in Applied Mathematics *June 2023*

- Mathematics Coursework: Linear Algebra, Probability and Statistics, Mathematical Modeling, Numerical Methods, Group Theory, Graph Theory, Real and Complex Analysis, Partial Differential Equations, Differential Geometry
- Engineering Coursework: Digital Signal Processing, Communications Systems, Computer Architecture, Numerical Computing, Biomedical Transducers, Feedback Control Theory, Machine Learning, Analog/Digital Circuits

Experience

Undergraduate Researcher October 2022 – Present
Communications Systems Lab UCLA *Los Angeles, CA, United States*

- Implemented an AWGN Generator in **Verilog** to accelerate FER/BER simulations of 2+ codes on **Xilinx FPGAs**
- **Directed** a group of 3 undergraduates in re-design of an FPGA accelerated convolutional list decoder; offered mentoring to expand theoretical understanding of material; **delegated** project tasking for over a 15 week window
- Discovered a key memory optimization for HW-accelerated list decoding; presented findings in an **honors thesis**

Sensors Intern June 2022 – February 2023
Systems and Technology Research *Woburn, MA, United States*

- Generated repositories to process **20+GB** of RF field test data utilizing **Python** and **MATLAB**; coordinated between 5 field operators and 3 programmers to develop a user-friendly GUI based on field test procedure
- Developed embedded **C** software to interface between PIC micro-controllers and RFSoCs using a PPP protocol
- Expanded functionality of an existing API in **C** and **Python** interfacing with EMF32 MCs to control a low pass filter

Undergraduate Researcher June 2020 – August 2021
Algorithmic Research in Networked Information Lab UCLA *Los Angeles, CA, United States*

- Produced Python scripts for simulation of Noisy Group Testing Algorithms to model efficient COVID testing schemes
- Designed and integrated a quantizer in **PyTorch** for a multi modal object tracking convolutional neural network

Projects

IEEE DAV *Verilog, Quartus, ModelSim Altera, Max 10 DE Lite* 2021-2022

- Collaborated with a team to implement an RTL digital audio visualizer on a MAX 10 DE Lite FPGA using **Verilog**
- Utilized **I2C** and **VGA** protocols to coordinate logic between FPGA and peripheral microphones and displays
- Created RTL implementations of **FFT** and arithmetic operations to enhance **DSP** fundamentals

IEEE Aircopter *C, Autodesk EAGLE, STM32F4* 2020-2021

- Co-produced a design for a 4-channel motor driver PCB controlled by a STM32F4 MCU using **Autodesk EAGLE**
- Employed SMT and re-flow techniques to assemble circuit elements and quad copter components on PCB
- Established **PID** control using Quaternion arithmetic via embedded C software development on the MCU

Technical Skills

Languages/Libs : Verilog, MATLAB, Python, C/C++, x86 Assembly, PyTorch, Numpy, SciPy
Design Tools : Vivado, Icarus Verilog, GTKWave, Quartus, ModelSim, Autodesk EAGLE, Visual Studio Code, Git, Jira
Hardware : Xilinx ZCU106, EFM32, Max 10 DE Lite, Arduino, PIC16F87XA, Analog Discovery 2, STM32F4