PULKIT AGRAWAL

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Education

Birla Institute of Technology and Sciences (BITS) Pilani, Goa Campus, India CGPA: 8.39/10
Bachelor of Engineering in Electronics & Instrumentation Engineering *Aug 2015 – May 2019*

Krishna Public School, Raipur, India
Grade 12th - 94/100 *Aug 2014 – May 2015*
Grade 10th - 10/10 *Aug 2012 – May 2013*

Experience

Research Assistant (Remote) - Prof. Akash Kumar Oct 2020 – Present
CFAED, Technische Universität Dresden, Germany

- Creating a **Multi-Level Intermediate Representation (MLIR)** based framework to support machine learning applications on heterogeneous platforms.

Firmware Engineer Sept 2020 – Present
Amplify Mobility Pvt. Ltd. *Hyderabad, India*

- Developing **C/C++** based firmware for AC & DC Electric Vehicle Charging Stations.
- Implementing application protocol, **Open Charge Point Protocol (OCPP)**, for the charging stations designed using **STM32** and **ESP32** micro-controller.
- Interfacing peripheral like RFID, GSM module, and STPM32 (Energy Metering device) with **ESP32** over **SPI/UART communication**.

Senior Analyst Aug 2019 – Feb 2020
Capgemini India Pvt. Ltd *Hyderabad, India*

- Worked with **Java** for implementing various object-oriented programming based problem statements in multi-layered architecture.

ASIC Design Intern July 2018 – Dec 2018
Nvidia Hardware *Bangalore, India*

- Worked with the **SOC Clocks Team** worked on generating Register-transfer-level (RTL) for *Tegra SOC* - *'Orin'* using a novel automated framework.
- Used **Synopsys SpyGlass** to generate lint reports to categorize about 35,000 errors. Wrote **Python/Perl** based scripts to automate the rectification process.
- Additionally, used the reports to find the root cause of the error, and fixed all the dependent errors by fixing the origin.

Technical Skills

Languages: Python, Perl, C/C++, Embedded C, Verilog, MASM (Assembly Language)
Developer Tools: Git, PyCharm, Arduino IDE, Keil μVision, Eclipse, ModelSim Altera

Relevant Coursework

Computer Architecture, Digital Design, Microprocessors and Interfacing, Operating Systems, Real-Time Systems, Data Structures and Algorithms, Network Embedded Applications, Introduction to C Programming.

Projects

Priority Readers and Writers | *Multi-threaded Programming, C* | Oct 2019 - Nov 2019

- Implemented a multi-threaded **C** program using **POSIX Threads** library, for reading and writing in a shared buffer. It gives readers priority over writers concerning the shared resource.
- Used pthreads, mutexes, and condition variables to synchronize access to the shared resource.

Multiplications of 'N' complex numbers | *Multi-threaded Programming, C* | Oct 2019 – Nov 2019

- Implemented a multi-threaded **C** program using **POSIX Threads** library, for multiplying 'N' complex numbers.
- Created pairs of 'N' complex numbers and performed concurrent multiplication using threads. Stored the result of each pair using dynamic memory allocation.
- Values from the multiplication of each pair were then used to create new pairs until the result was obtained.

RISC Processor Synthesis | *Computer Architecture, Verilog* March 2018 – April 2018

- Implemented 32-bit **MIPS Architecture** with a simple Arithmetic Logic Unit (ALU) and Control Unit in **Verilog**.
- Designed a Hazard Unit to take care of any potential hazards and wrote test benches to test the pipeline architecture.

Approximate Adder Circuits | *Cadence RTL Compiler, Verilog* Jan 2018 – April 2018

- Implemented various single-level and multi-level approximation adder architectures in **Verilog** and compared them with exact architecture.
- Used **Cadence RTL Compiler** to synthesize the design and the post-synthesis reports to compare the architectures.

Scheduling Algorithms for Real-Time System | *ADA Language, Cheddar Simulator* | Aug 2017 – Sept 2017

- Implemented user-defined scheduling algorithms for real-time systems in **ADA Language** used by **Cheddar Simulator** (developed by UC Berkeley.)
- Designed a hybrid algorithm, dynamic-priority scheduling class, where the tasks with zero laxity was given the highest priority.

Position of Responsibility

Undergraduate Teaching Assistant Jan 2019 – May 2019

Real-Time Systems, Under Prof. Biju K Raveendran, BITS Pilani, Goa, India

- Mentored a class of 21 postgraduate and PhD students.
- Designed assignment and study material for the students. Conducted Lab sessions and evaluated the lab assignments.

Undergraduate Teaching Assistant Jan 2019 – May 2019

Microprocessors and Interfacing, Under Prof. Anupama KR, BITS Pilani, Goa, India

- Mentored a class of 300+ undergraduate students.
- Designed and conducted sessions for **8086 microprocessor**-based design problems in **Proteus Design Suite**. Evaluated labs on Assembly programming using **MASM Language**.

Undergraduate Teaching Assistant Jan 2018 – May 2018

Microprocessors and Interfacing, Under Prof. Anupama KR, BITS Pilani, Goa, India

- Mentored a class of 280+ undergraduate students.
- Prepared model solutions for tutorial sessions. Assisted the professor in clearing doubts of the students during the tutorial session.

Undergraduate Teaching Assistant Aug 2017 – Dec 2017

Digital Logic Design Laboratory, Under Prof. Sudeep Baudha, BITS Pilani, Goa, India

- Mentored a class of 300+ undergraduate students.
- Assisted the professor in conducting lab sessions. Helped students in implementing digital design problems in bread-board using various ICs, and debugging the issues.

Others

Interested in Photography and Videography. Learned video editing software, **Adobe Premiere Pro** and **Adobe After Effects**. Created a YouTube channel to showcase my projects. Most of my projects are alternate music videos of some famous songs like, *Photograph* by *Ed Sheeran*, etc.