Register number _____

SRM Institute of Science and Technology
College of Engineering and Technology
School of Computing
SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu
Academic Year: 2023-24 (EVEN)
B.Tech-Computer Science & Engineering **SET – C-Answer Key**

Test: CLA-T3 **Date: 03.05.2024**
Course Code & Title: 18CSE419T & GPU Programming **Duration: 2 periods**
Year & Sem: III Year /VI Sem **Max. Marks: 50**

Course articulation matrix:

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO-1	3														3
CO-2		3	2												3
CO-3		3	3												3
CO-4		3	3												3
CO-5			3	1									2		3

Part – A(1*10=10 Marks)
Answer All the Questions

Q. No	Questions	Marks	BL	CO	PO	PI Code
1	Which command will display information about available accelerators? a) acc info b) acclinfo **c) pgaccelinfo** d) #pragma accinfo	1	1	CO 4	2	**2.2.1**
2	When using parallel directive which command is implied? a) Auto **b) Independent** c) Seq d) Dependent	1	1	CO 4	2	**2.2.1**
3	Which cluse converts multi-dimensional loop nest into a single -dimensional loop? a) Parallel clause b) Reduction clause **c) Collapse clause** d) tile	1	1	CO 4	2	**2.2.1**
4	The lowest level of parallelism is a) Gang b) Worker **c) Vector** d) warp	1	1	CO 4	2	**2.2.1**
5	The primary use of the _____ clause is to split up one large vector into multiple smaller vectors a) Gang b) Worker **c) Vector** d) thread	1	1	CO 4	2	**2.2.1**
6	OpenACC adopts **a) weak consistency memory model** b) strong consistency memory model c) fork-join memory model d) constant memory model	1	1	CO 5	3	**3.2.1**
7	In OpenACC memory model	1	1	CO 5	3	**3.2.1**

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	a) host memory and device memory are combined **b) host memory and device memory are separated** c) only device memory available d) no connection between host and device					
8	_____will create the memory on the GPU and transfer the data from CPU to GPU. a) Copy(list) **b) Copyin(list)** c) Copyout(list) d) Create(list)	1	1	CO 5	3	**3.2.1**
9	GPU is connected to CPU through **a) PCI bus** b) NVIDIA connector c) ACG connector d) ICP bus	1	1	CO 5	3	**3.2.1**
10	Scalars are _____ when used in a parallel region and _____ when used in a kernel region. a) Private, firstprivate b) Firstprivate, private **c) Public, private** Private,public	1	1	CO 5	3	**3.2.1**
	Part – B (4*4=16 marks) **Answer any four Questions**					
Q. No	**Question**	**Marks**	**BL**	**CO**	**PO**	**PI Code**
11	Sketch the OpenACC execution model and explain. ● The OpenACC target machine has a host and an attached accelerator device, such as a GPU. ● Most accelerator devices can support multiple levels of parallelism. ● Figure 15.2 illustrates a typical accelerator that supports three levels of parallelism. ● At the outermost coarse-grain level, there are multiple execution units. Within each execution unit, there are multiple threads. ● At the innermost level, each thread is capable of executing vector operations. ● Currently, OpenACC does not assume any synchronization capability on the accelerator, except for thread forking and joining. ● Once work is distributed among the execution units, they will execute in parallel from start to finish.	4	2	CO4	2 & 3	**2.2.1**
12	State the purpose of implied data regions in OpenACC.	4	3	CO5	3	**2.2.1**
13	Compare and contrast OpenACC and CUDA Besides, OpenACC programs are more sensitive to data changes than the equivalent CUDA programs with optimizations, but CUDA is more sensitive to data changes than OpenACC if there are no optimizations. Overall we found that OpenACC is a reliable programming model and a good alternative to CUDA for accelerator devices.	4	3	CO4	2 & 3	**2.2.1**
14	List the data clauses of OpenACC.	4	3	CO5	3	**2.2.1**
15	With a code snippet show how async and wait are used in OpenACC.	4	3	CO5	3	**2.2.1**
	Part – C (2*12=24 marks) **Answer any Two Questions**					
16	In loop optimization illustrate the role of	12	3	CO5	3	**2.2.1**

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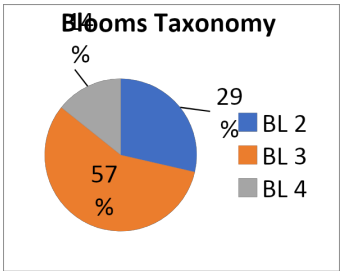
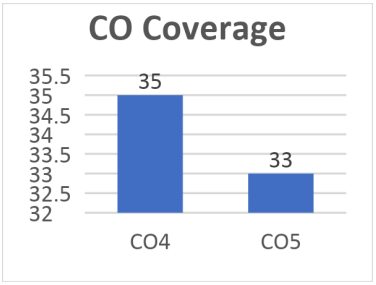
	(i). Collapse clause (ii). Tile clause					
17	Demonstrate with a proper code segment the following: (i) OpenACC data directive (ii) Structured data directive	12	3	CO4 & CO5	2 & 3	**2.2.1**
18	Brief on the following: (i). OpenACC data management process (ii). OpenACC execution model	12	3	CO4	2 &3	**2.2.1**





Approved by Audit Professor/ Course Coordinator

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