Register number _____

SRM Institute of Science and Technology
College of Engineering and Technology
School of Computing
SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu
Academic Year: 2023-24 (EVEN)
B.Tech-Computer Science & Engineering **SET - C**

Test: CLA-T2 **Date: 28.03.2024**
Course Code & Title: 18CSE419T & GPU Programming **Duration: 2 periods**
Year & Sem: III Year /VI Sem **Max. Marks: 50**

Course articulation matrix:

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO-1	3														3
CO-2		3	2												3
CO-3		3	3												3
CO-4		3	3												3
CO-5			3	1									2		3

Part – A(1*10=10 Marks)
Answer All the Questions

Q. No	Questions	Marks	BL	CO	PO	PI Code
1	The kernel code is identified by the ---------- qualifier with VOID return type a) __host__ b) – global— c) –device— d) void	1	2	CO 3	2 & 3	**4.2.1**
2	The CUDA architecture consists of ---------- parallel computing kernels and functions a) RISC b) CISC c) PTX d) ZISC	1	2	CO 3	2 & 3	**4.2.1**
3	In CUDA Programming blockDim.x represents a) Number of threads per block b) Number of blocks in a kernel c) Number of blocks in a grid d) Number of blocks in a warp	1	2	CO 3	2 & 3	**4.2.1**

4	What is the CUDA function call required to copy an array h_A from the CPU memory to the GPU memory as d_A?
	a) cudaMemcpy(h_A,d_A,size,cudaMemcpyHost to Device);
	b) cudaMemcpy(d_A,h_A,size,cudaMemcpyHost to Device);
	c) cudaMemcpy(h_A,d_A,size,cudaMemcpyDevice to Host);
	d) cudaMemcpy(d_A,h_A,size, cudaMemcpyDevice to Host);
		1	2	CO 3	2 & 3	**4.2.1**

5	If each CUDA block can hold a maximum of 512 threads then how many CUDA blocks would be created to process 4000 vector elements a) 7 b) 8 c) 10	1	2	CO 3	2 & 3	**4.2.1**

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	d) 16					
6	Which of the following memory locations is common for all the SMs in a typical CUDA GPU? a) Thread-local memory b) L1 cache c) L2 cache d) Shared memory	1	2	CO 3	2 & 3	**4.2.1**
7	What is the term used for the combination of CPU and GPU in a hybrid computing system? a) Homogenous computing b) Many-core architecture c) Hardware accelerator d) Heterogenous computing	1	3	CO 3	2 & 3	**4.2.1**
8	Which one is not an off-chip memory in GPU? a) Cache memory b) Global memory c) Texture memory d) Constant memory	1	3	CO 3	2 & 3	**4.2.1**
9	The page -locked memory is also referred to as a) Constant memory b) Zero-copy memory c) Pinned memory d) Texture memory	1	3	CO 3	2 & 3	**4.2.1**
10	If a variable a is host variable and dev_a is a device variable to allocate a memory to dev_a. Select the correct statement. a) Cudamalloc(&dev_a,sizeof(int)) b) Malloc(&dev_a,size of (int)) c) Cudamalloc (void **)&dev_a,size of (int)) d) Malloc (void **)&dev_a size of (int))	1	3	CO 3	2 & 3	**4.2.1**
Part – B (4*4=16 marks) Answer any four Questions						
Q. No	**Question**	**Marks**	**BL**	**CO**	**PO**	**PI Code**
11	Define constant memory and state its characteristics	4	3	CO 2	2 & 3	**4.2.1**
12	What is pinned memory in GPU? Write short notes on it.	4	3	CO 2 & CO 3	2 & 3	**4.2.1**
13	Discuss about CUDA's variable type qualifiers.	4	2	CO 3	2 & 3	**4.2.1**
14	Sketch GPU memory hierarchy and describe its functions	4	2	CO 3	2 & 3	**4.2.1**
15	What is local memory in GPU? What are the uses of it.	4	3	CO 3	2 & 3	**4.2.1**
Part – C (2*12=24 marks) Answer any four Questions						
16	Write a CUDA program to illustrate the vector addition using multiple thread block.	12	2	CO 3	2 & 3	**4.2.1**

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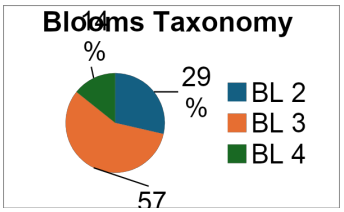
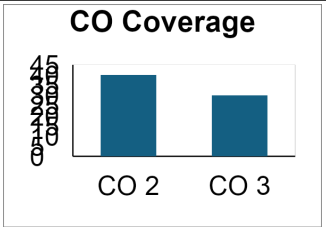
17	With a neat sketch illustrate the three ways of accessing the global memory from the GPU.	12	3	CO 3	2 & 3	**4.2.1**
18	Implement the code to illustrate the accessing of global memory of GPU for sorting.	12	3	CO 3	2 & 3	**4.2.1**





Approved by Audit Professor/ Course Coordinator

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