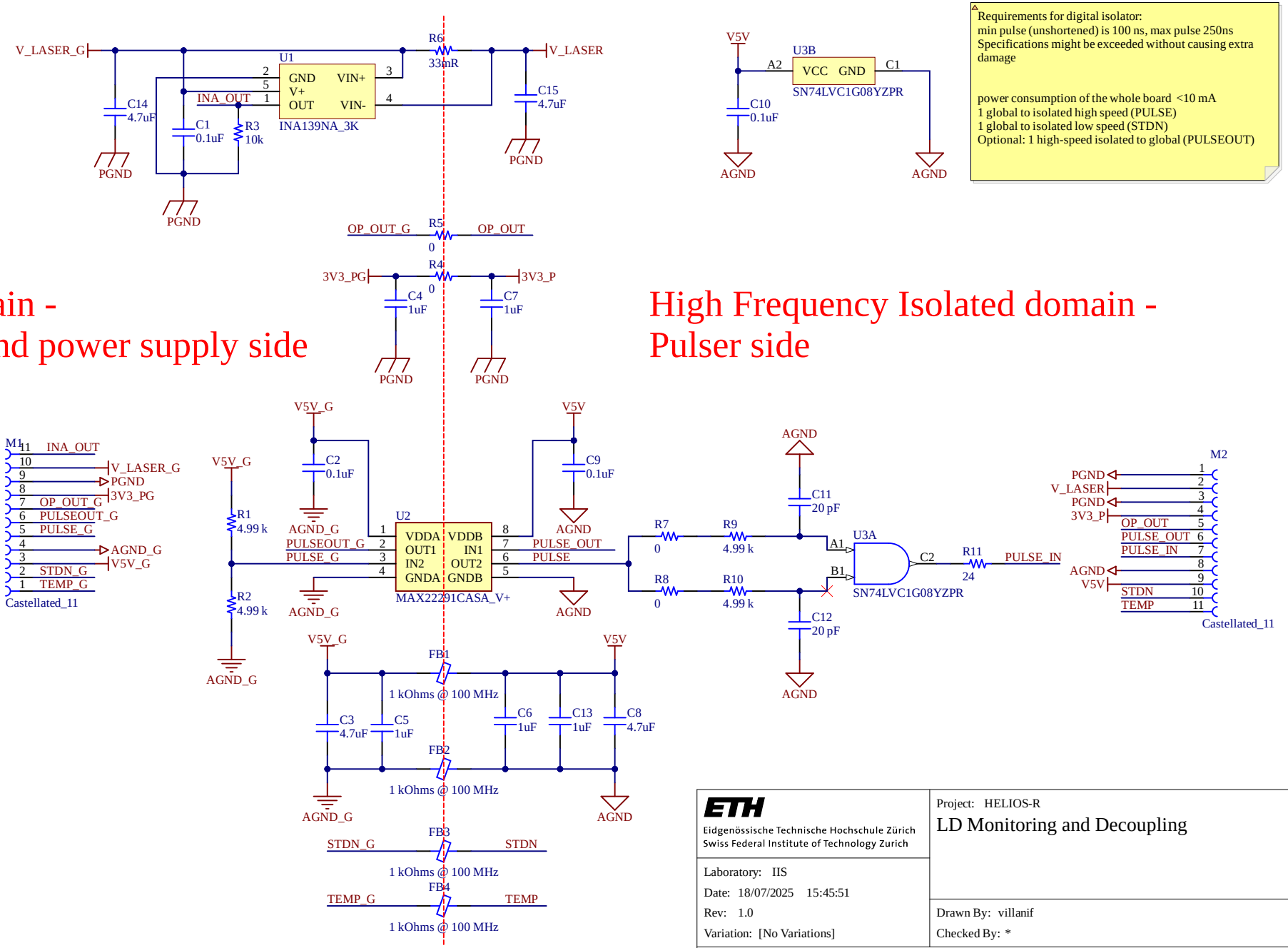
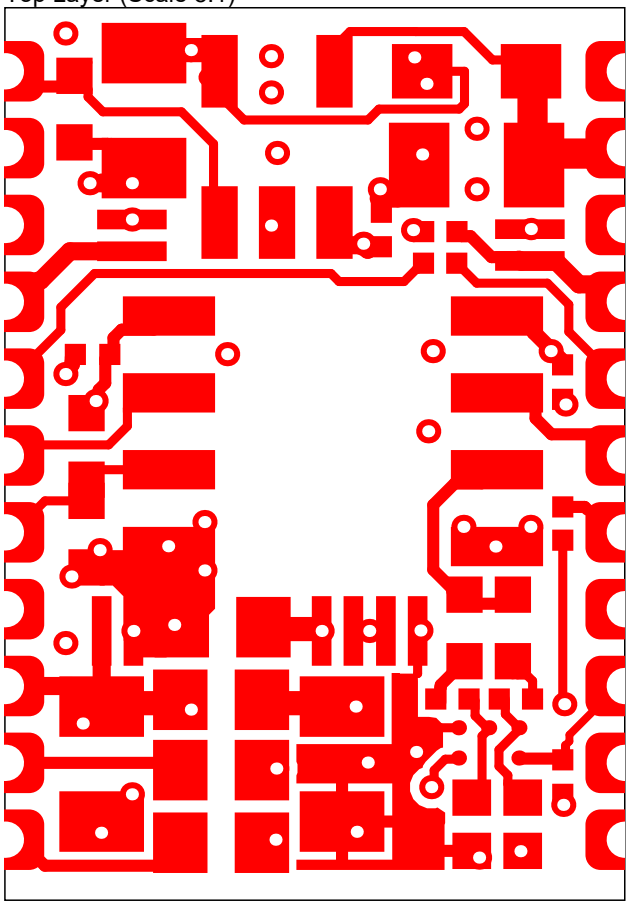
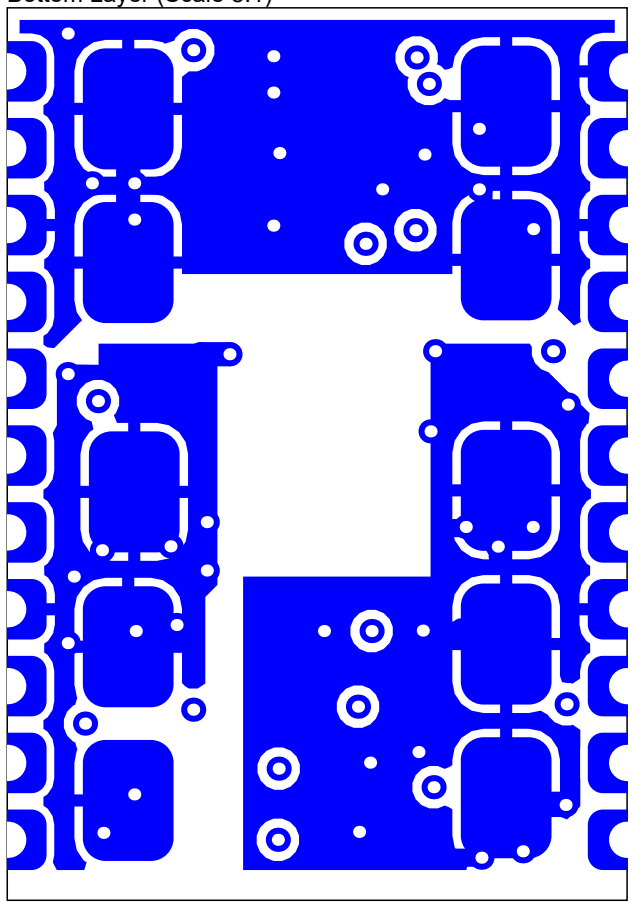

Global domain -
Controller and power supply side
High Frequency Isolated domain -
Pulser side
V_LASER_G
V_LASER
R6
33mR
U1
GND
V+
OUT
VIN+
VIN-
INA139NA_3K
INA_OUT
C14
4.7uF
C1
0.1uF
R3
10k
C15
4.7uF
PGND
V5V
U3B
VCC
GND
SN74LVC1G08YZPR
C10
0.1uF
AGND
Requirements for digital isolator:
min pulse (unshortened) is 100 ns, max pulse 250ns
Specifications might be exceeded without causing extra damage
power consumption of the whole board <10 mA
1 global to isolated high speed (PULSE)
1 global to isolated low speed (STDN)
Optional: 1 high-speed isolated to global (PULSEOUT)
OP_OUT_G
R5
OP_OUT
3V3_PG
R4
3V3_P
C4
1uF
C7
1uF
M1
INA_OUT
V_LASER_G
PGND
3V3_PG
OP_OUT_G
PULSEOUT_G
PULSE_G
AGND_G
V5V_G
STDN_G
TEMP_G
Castellated_11
V5V_G
C2
0.1uF
R1
4.99 k
R2
4.99 k
U2
VDDA
OUT1
IN2
GNDA
VDDB
IN1
OUT2
GNDB
MAX22201CASA_V+
C9
0.1uF
PULSE_OUT
PULSE
R7
0
R9
4.99 k
R8
0
R10
4.99 k
C11
20 pF
C12
20 pF
U3A
SN74LVC1G08YZPR
C2
R11
24
PULSE_IN
M2
FB1
1 kOhms @ 100 MHz
C3
4.7uF
C5
1uF
C6
1uF
C13
1uF
C8
4.7uF
FB2
FB3
STDN
FB4
TEMP
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
Project: HELIOS-R
LD Monitoring and Decoupling
Laboratory: IIS
Date: 18/07/2025 15:45:51
Rev: 1.0
Variation: [No Variations]
Drawn By: villanif
Checked By: *
File: ld_monitoring_decoupling.SchDoc
Sheet: 2 / 6

Top Layer (Scale 8:1)



Bottom Layer (Scale 8:1)



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Project: HELIOS-R

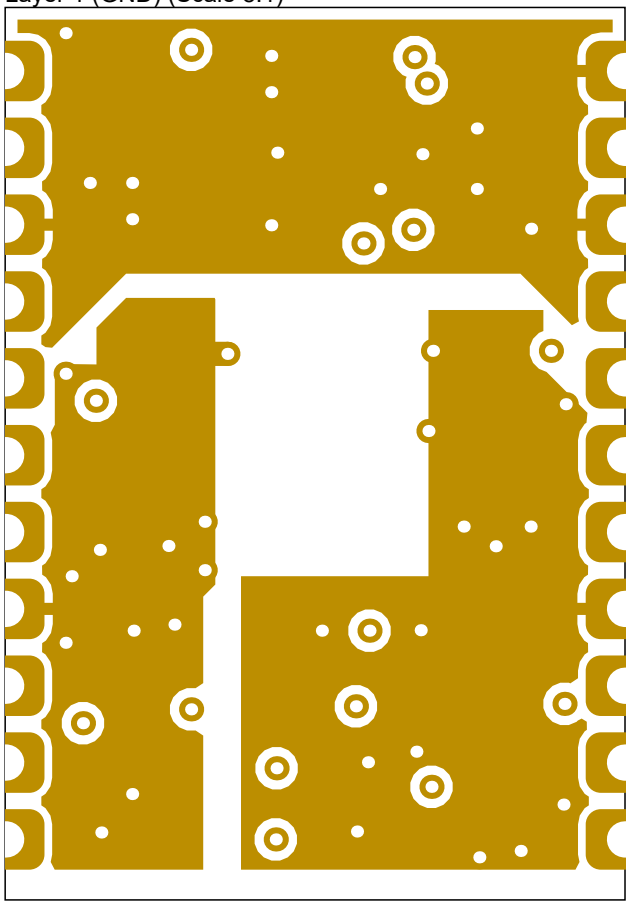
LD Pulser Driver - Layout

Laboratory: IIS
Date: 18/07/2025 15:45
Rev: 1.0
Variation: [No Variations]

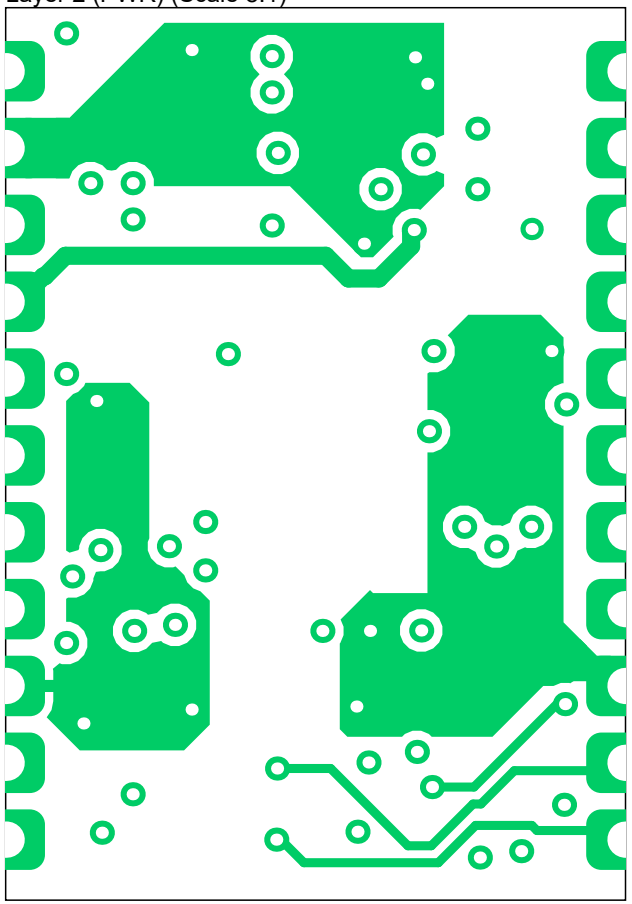
Drawn By: villanif
Checked By: *

File: PULSER_LAY.PCBDwf

Layer 1 (GND) (Scale 8:1)



Layer 2 (PWR) (Scale 8:1)



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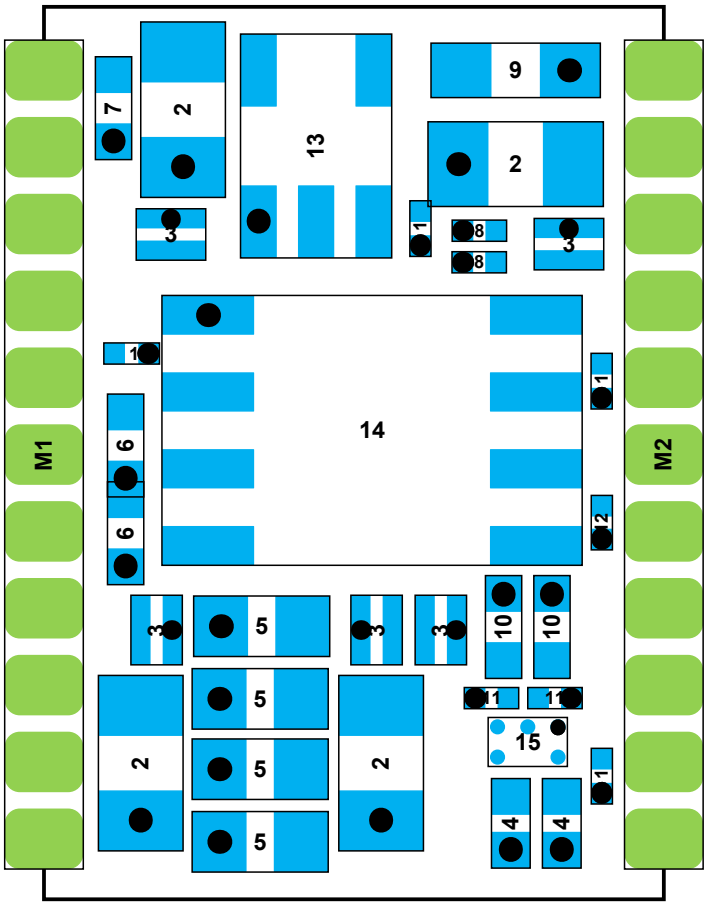
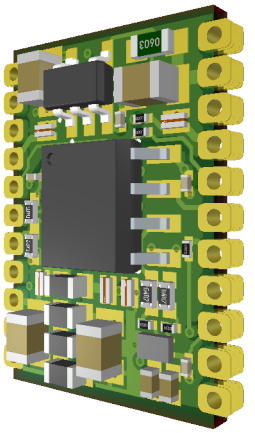
Laboratory: IIS Date: 18/07/2025 15:45 Rev: 1.0 Variation: [No Variations]	Drawn By: villanif Checked By: *
File: PULSER_LAY.PCBDwf	Sheet: 2 / 2

View from Top side (Scale 8:1)



Realistic View



Notes:
- Number on assembly view = line # of component
- Pin 1 is indicated by the black dot for each component
- Smallest components: 0201

Bill Of Materials

Line #	Designator	Quantity	Description	Manufacturer Part Number 1
1	C1, C2, C9, C10	4	CAP CER 0.1UF 35V X5R 0201	GRM033R6YA104ME14D
2	C3, C8, C14, C15	4	CAP CER 4.7UF 50V X6S 0805	GRM21BC81H475KE11K
3	C4, C5, C6, C7, C13	5	CAP LOW L CER 1UF 6.3V X7T 0204	LLL152D70J105ME01D
4	C11, C12	2	CAP CER 20PF 50V C0G/NP0 0402	GCM1555C1H200FA16D
5	FB1, FB2, FB3, FB4	4	FERRITE BEAD 1K OHM 0603 1LN	BLM18SP102SH1D
6	R1, R2	2	RES SMD 4.99KOHM 0.1% 1/16W 0402	ERA-2AEB4991X
7	R3	1	RES SMD 10KOHM 0.1% 63mW 0402	ERA-2AEB103X
8	R4, R5	2	RES SMD 0OHM 0.1% 1/20W 0201	ERJ-1GN0R00C
9	R6	1	RES 0.033 OHM 1% 1/4W 0603	
10	R7, R8	2	RES SMD 0OHM 1/10W 0402	ERJ-S020R00X
11	R9, R10	2	RES SMD 4.99 kOHM 1% 1/20W 0201	ERJ-1GNF4991C
12	R11	1	RES SMD 24 OHM 1% 1/20W 0201	ERJ-1GNF24R0C
13	U1	1	IC Inamp high-side current monitor	INA139NA/3K
14	U2	1	IC Digital Isolator, 2CH	MAX22291CASA/V+
15	U3	1	IC Single 2-Input Positive-AND Gate, YZP0005ADAD, LARGE T&R	SN74LVC1G08YZPR

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Laboratory: IIS
Date: 18/07/2025 15:46
Rev: 1.0
Variation: [No Variations]

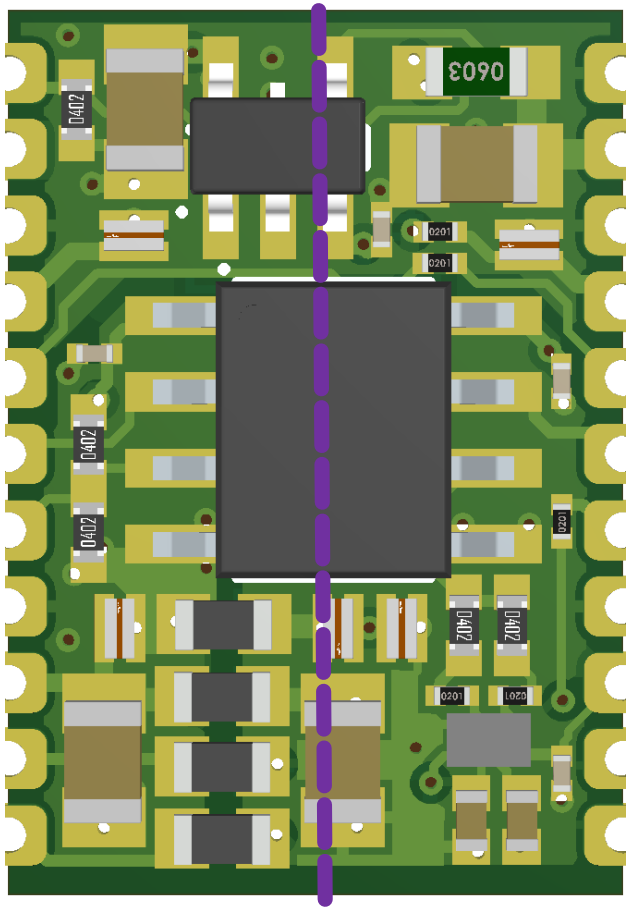
Project: HELIOS-R
LD Pulser - Assembly Sheet

Drawn By: villanif
Checked By: *

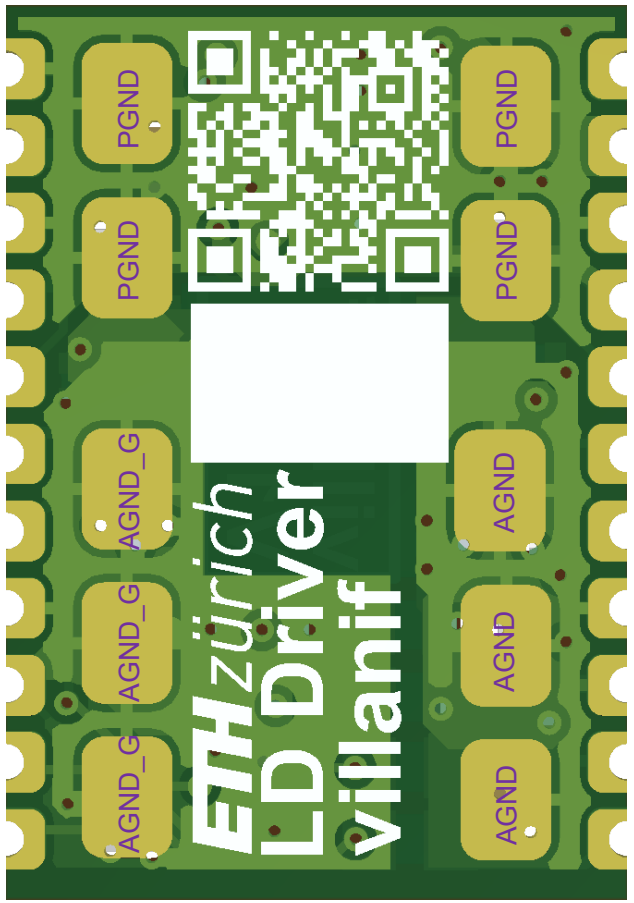
File: PULSER_ASM.PCBDwf

Sheet: 1 / 1

Realistic View



Realistic View



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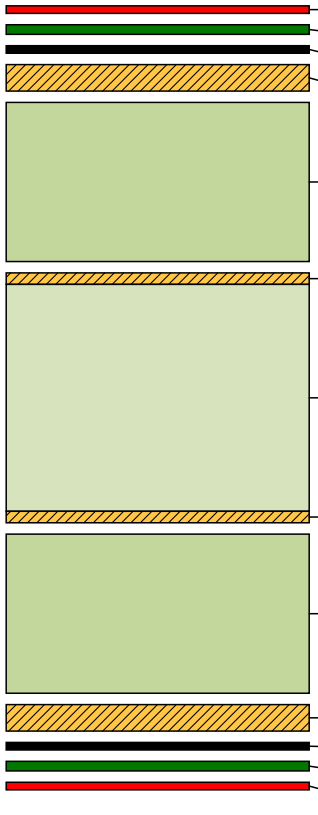
Laboratory: IIS Date: 18/07/2025 15:46 Rev: 1.0 Variation: [No Variations]	Drawn By: villanif Checked By: *
File: PULSER_CON.PCBDwf	Sheet: 1 / 1

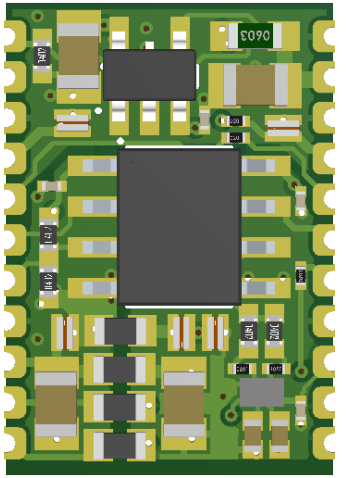
Layer Stack Legend



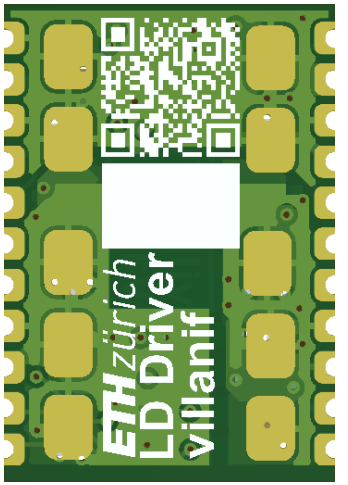
Material	Layer	Thickness	Type	Gerber	Weight
	Top Overlay		Legend	GTO	
Surface Material	Top Solder	0.013mm	Solder Mask	GTS	
Nickel, Gold	Top Surface Finish	0.004mm	Surface Finish		
Copper	**Top Layer**	**0.035mm**	**Signal**	**GTL**	**1oz**
Prepreg		*0.210mm*	*Dielectric*		
Copper	**Layer 1 (GND)**	**0.015mm**	**Signal**	**G1**	**0.5oz**
Core		*0.400mm*	*Dielectric*		
Copper	**Layer 2 (PWR)**	**0.015mm**	**Signal**	**G2**	**0.5oz**
Prepreg		*0.210mm*	*Dielectric*		
Copper	**Bottom Layer**	**0.035mm**	**Signal**	**GBL**	**1oz**
Nickel, Gold	Bottom Surface Finish	0.004mm	Surface Finish		
Surface Material	Bottom Solder	0.013mm	Solder Mask	GBS	
	Bottom Overlay		Legend	GBO	

Total thickness: 0.955mm

Realistic View

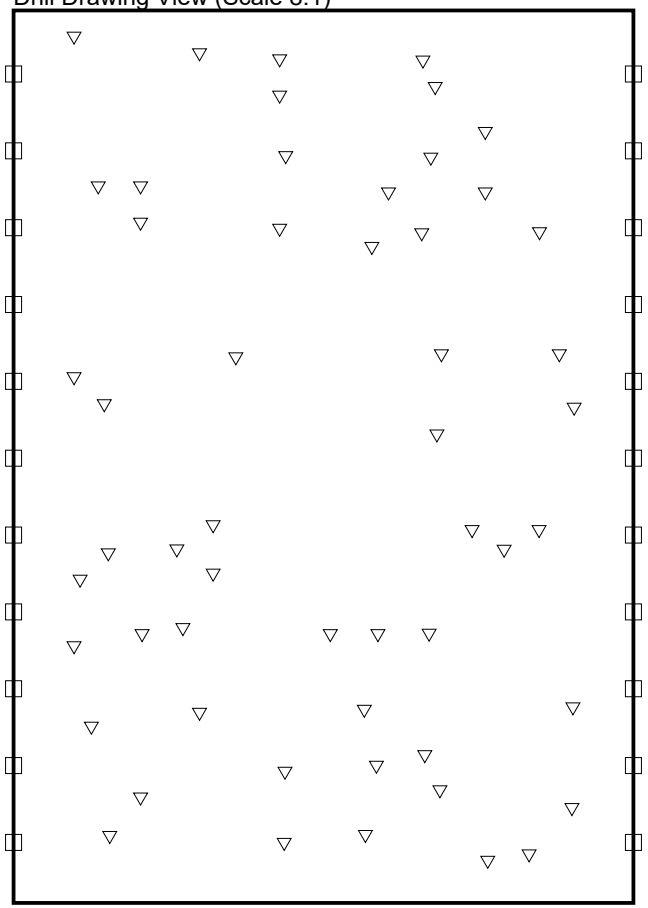


Realistic View



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: HELIOS-R LD Pulser Driver - Manufacturing
Laboratory: IIS Date: 18/07/2025 15:46 Rev: 1.0 Variation: [No Variations]	Drawn By: villanif Checked By: *
File: PULSER_MAN.PCBDwf	Sheet: 1 / 2

Drill Drawing View (Scale 8:1)



Drill Table - top to bottom

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad
▽	54	0.20mm	Plated	Top Layer - Bottom Layer	Via
□	22	0.60mm	Plated	Top Layer - Bottom Layer	Pad
	76 Total				

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Date: 18/07/2025 15:46
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Project: HELIOS-R
LD Pulser Driver - Manufacturing

Drawn By: villanif
Checked By: *

File: PULSER_MAN.PCBDwf