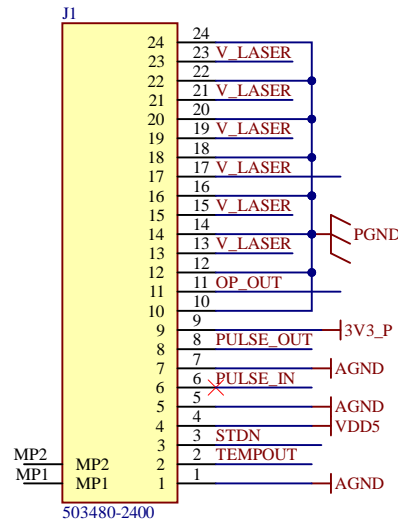
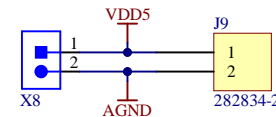
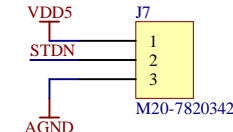
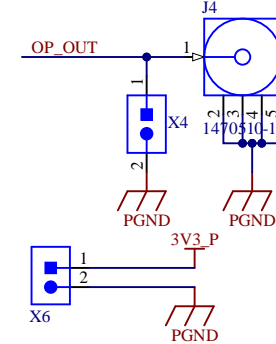
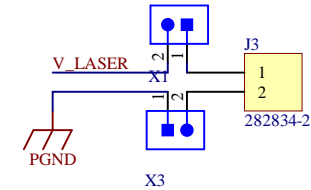
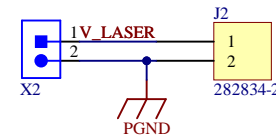
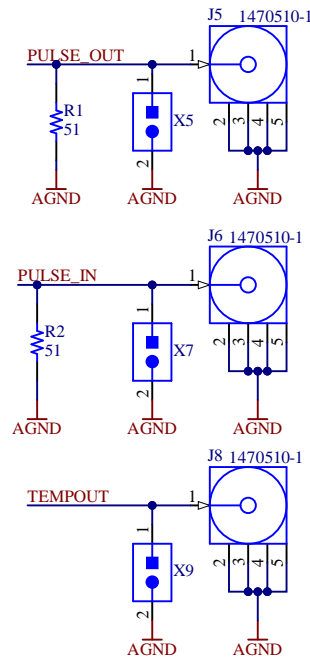


**A** J1 has rating of 500 mA/pin and 50V pin to pin, doublesided connection, 6 parallel V\_LASER connections: 3 A



**A** J1 Is oriented to be placed on the same side as its counterpart on the pulser board. for the right connection all connectors should face up



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Variation: [No Variations]

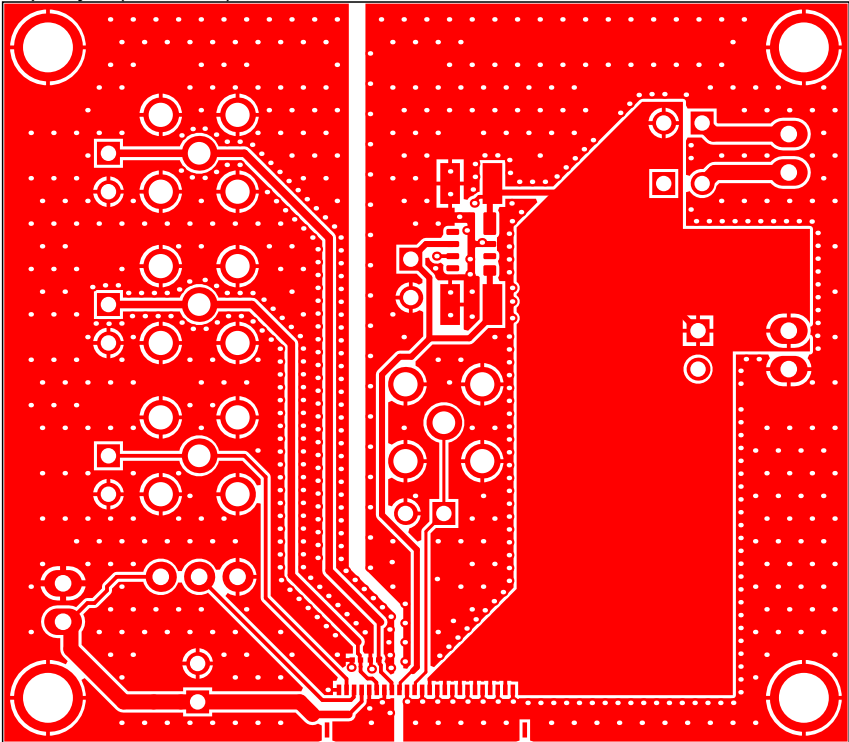
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Project: HELIOS-R  
Pulser Testboard

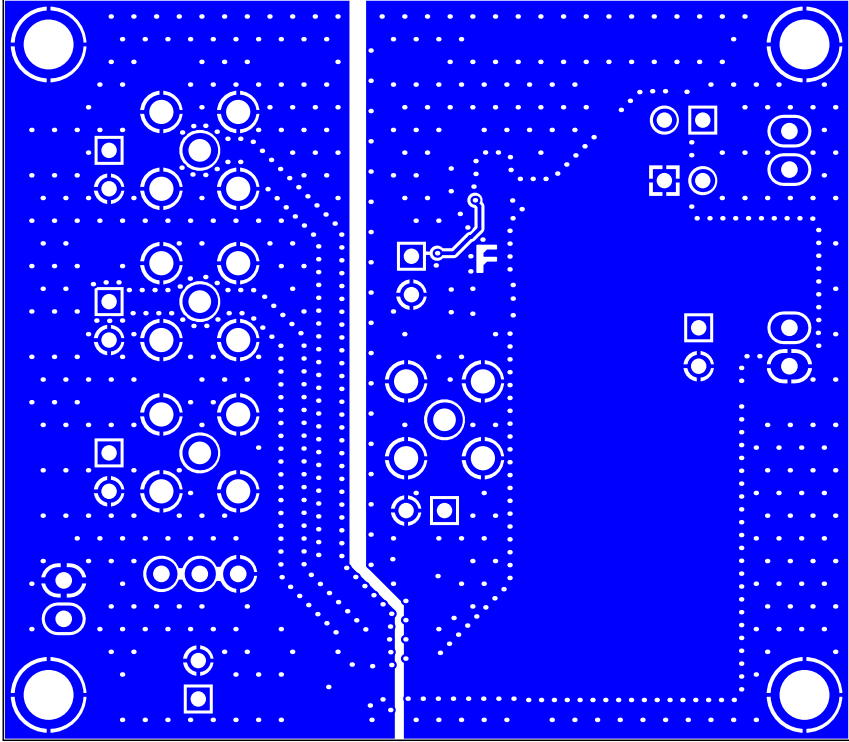
Drawn By: villanif  
Checked By: \*

Sheet: 1 / 1

Top Layer (Scale 2:1)



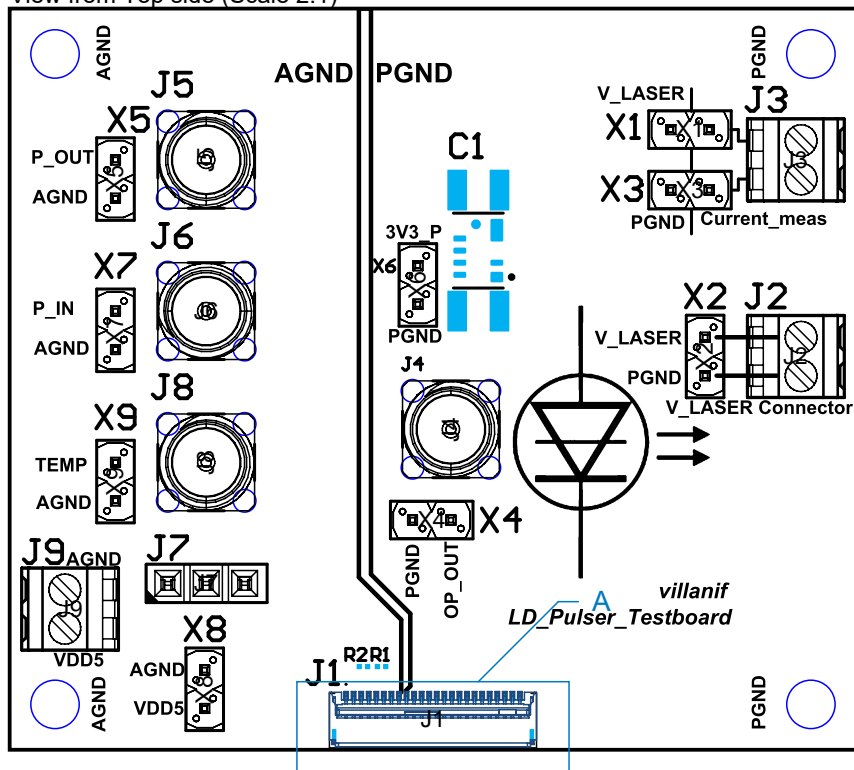
Bottom Layer (Scale 2:1)



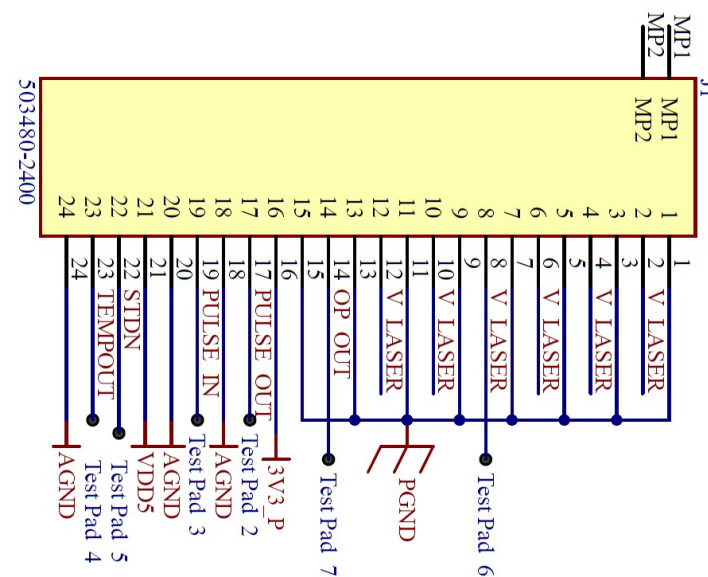
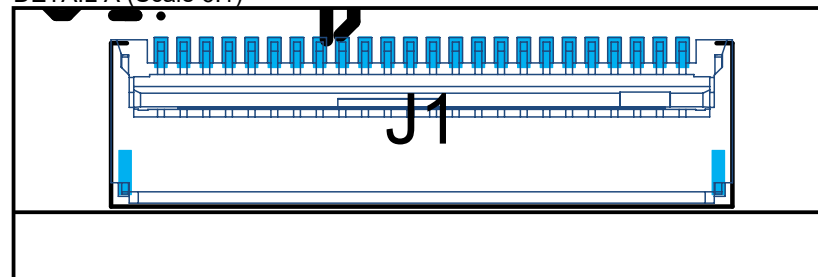
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	LD Pulser - Layout Sheet
	Drawn By:villanif
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	Sheet: 1 / 1



View from Top side (Scale 2:1)



DETAIL A (Scale 6:1)



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	Drawn By: villanif Checked By: *
	Sheet: 1 / 1

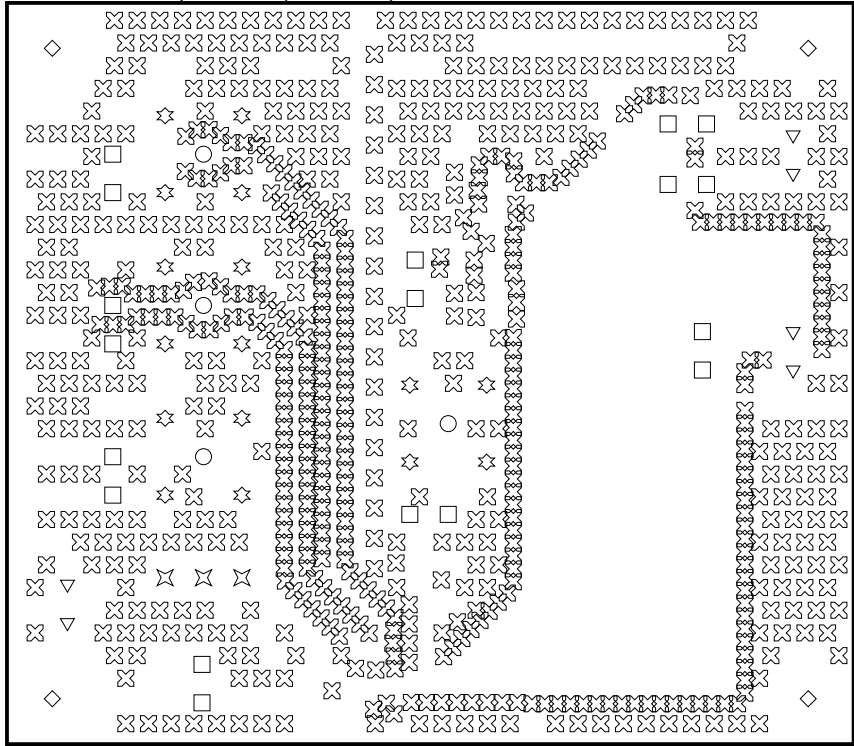
A

B

C

D

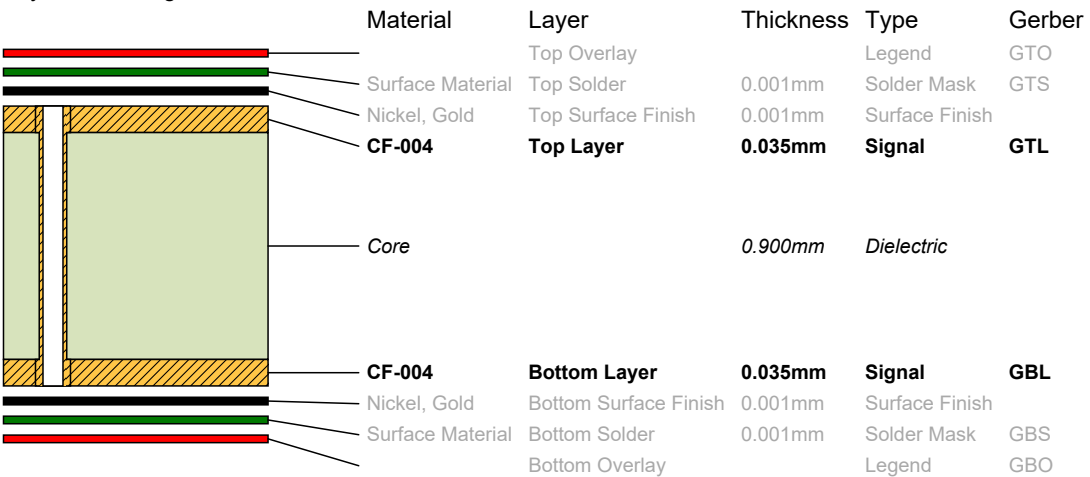
Drill View vias top-bottom (Scale 2:1)



Drill Table - top to bottom

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad
⊠	721	0.30mm	Plated	Top Layer - Bottom Layer	Via
□	18	1.02mm	Plated	Top Layer - Bottom Layer	Pad
▽	6	1.10mm	Plated	Top Layer - Bottom Layer	Pad
✱	3	1.10mm	Plated	Top Layer - Bottom Layer	Pad
○	4	1.50mm	Plated	Top Layer - Bottom Layer	Pad
☆	16	1.60mm	Plated	Top Layer - Bottom Layer	Pad
◇	4	3.30mm	Plated	Top Layer - Bottom Layer	Pad
772 Total					

Layer Stack Legend



Total thickness: 0.974mm

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Variation[No Variations]

File: PULSER\_MAN.PCBDwf

Project: HELIOS-R

LD Pulser - Manufacturing Sheet

Drawn By: villanif

Checked By: \*

Sheet: 1 / 1

A

B

C

D