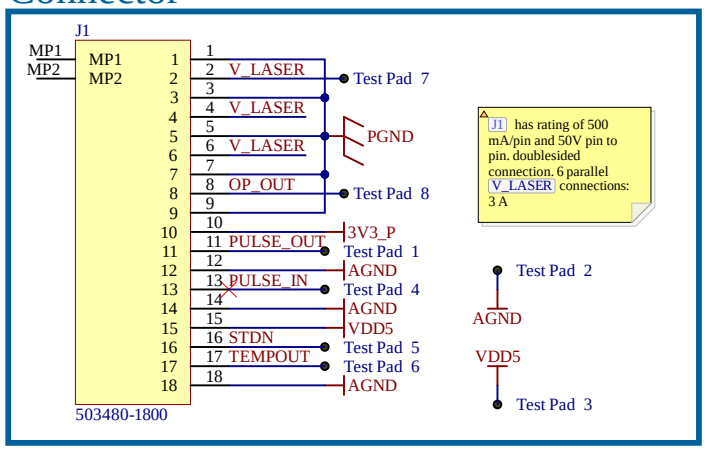
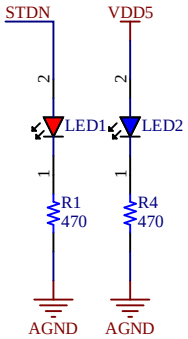
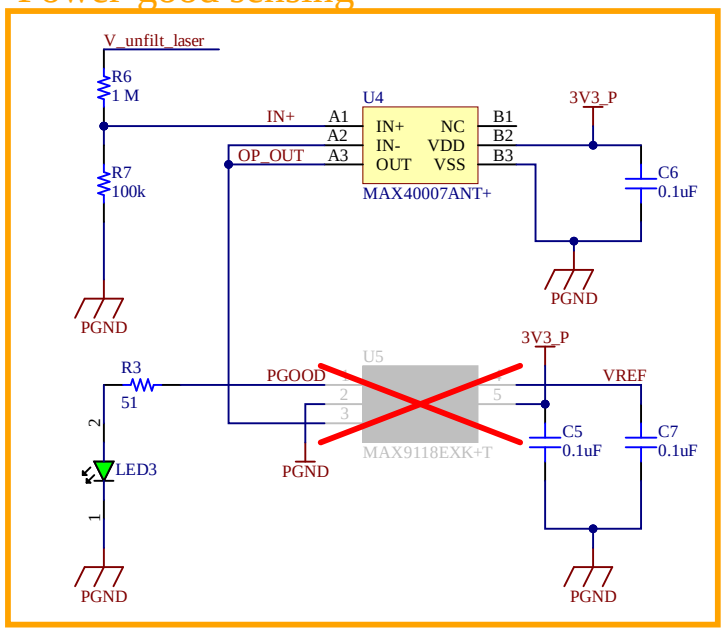
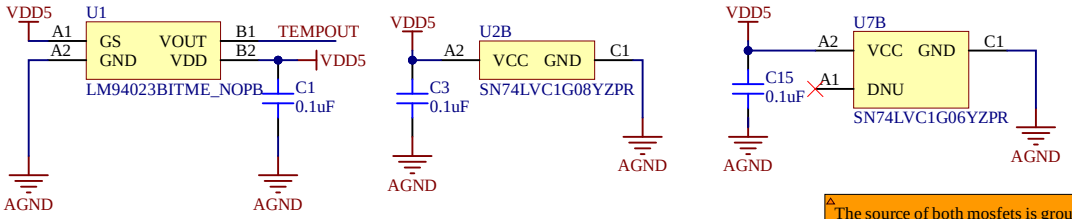
Connector

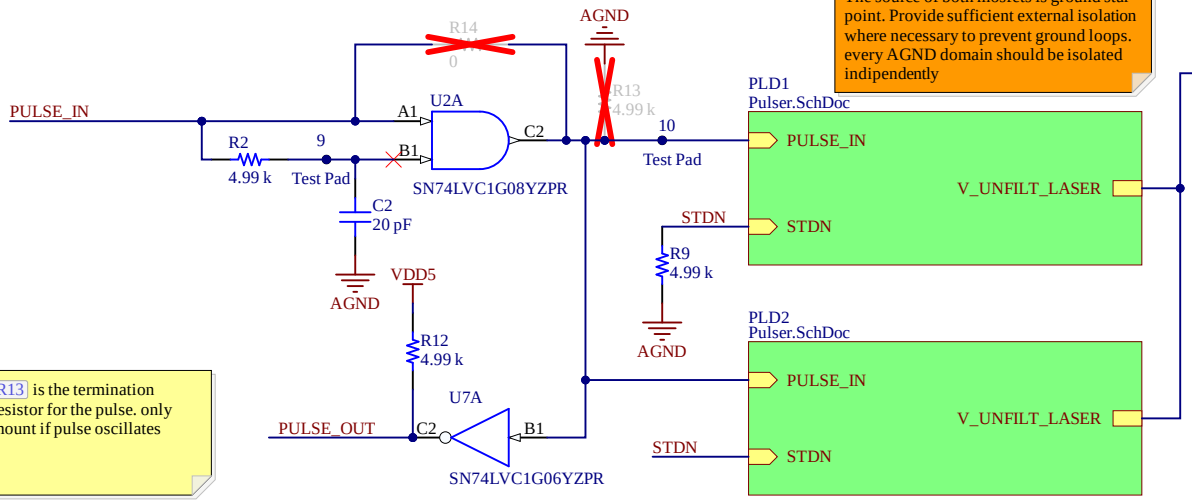


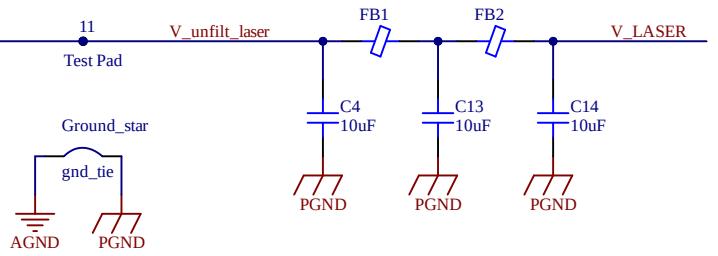


Power-good sensing









ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Laboratory: IIS
Date: 17/07/2025 14:38:57
Rev: 2
Variation: fabrication

Project: HELIOS-R

Pulser Laser Board

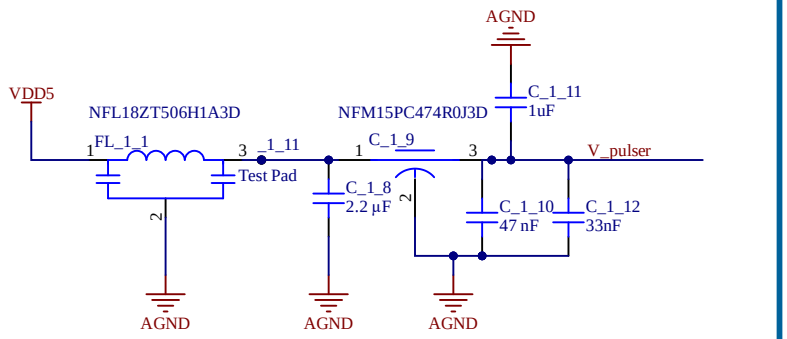
The frontend pcb for the pulser module
Has to be used together with a controller board
Pulses 4 laser modules with 320 A and 20-24 V
Do not pulse longer than 150 ns

Drawn By: villanif
Checked By: liuxian

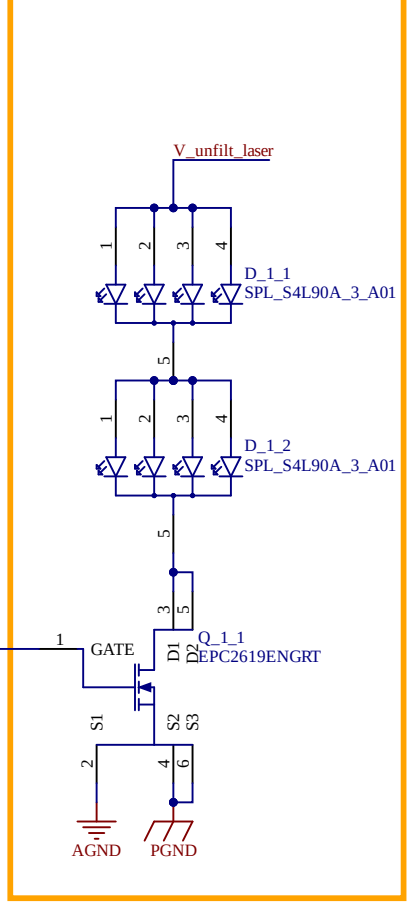
File: main.SchDoc
Sheet: 1 / 2

V_UNFILT_LASER — V_unfilt_laser

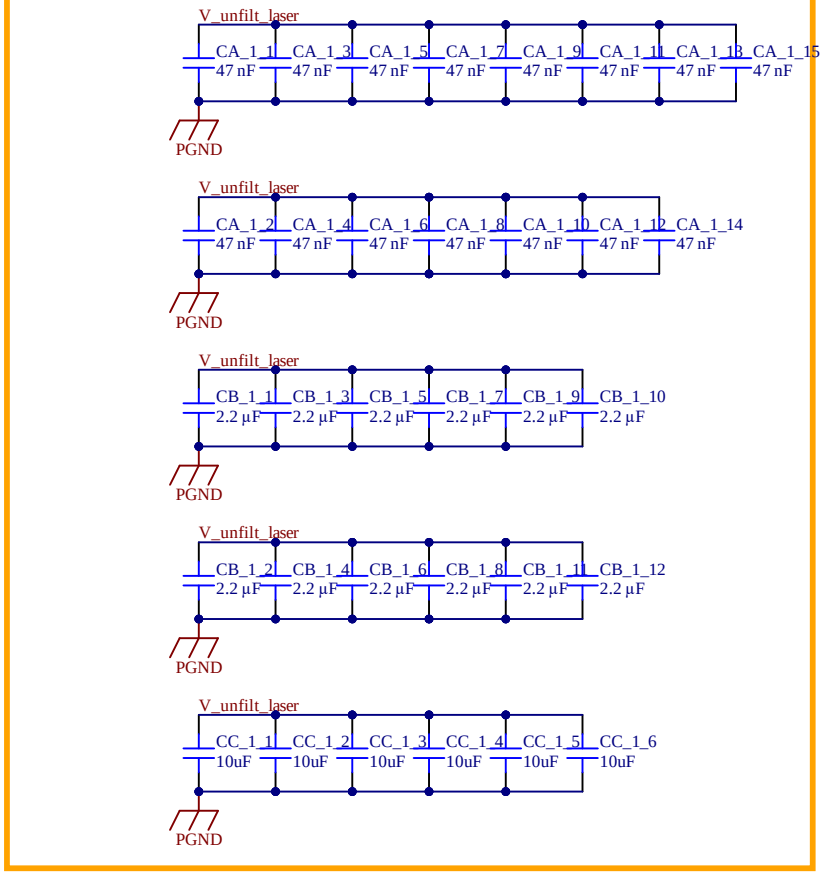
Pulser



Laser Diodes



Capacitor Bank



Mosfet source is ground star point. Provide sufficient external isolation where necessary to prevent ground loops. every AGND domain should be isolated indipendently

ETH
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Date: 17/07/2025 14:38:57
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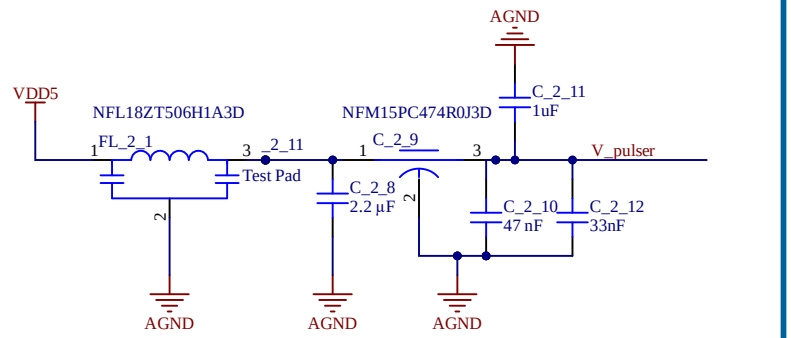
Drawn By: villanif
Checked By: liuxian

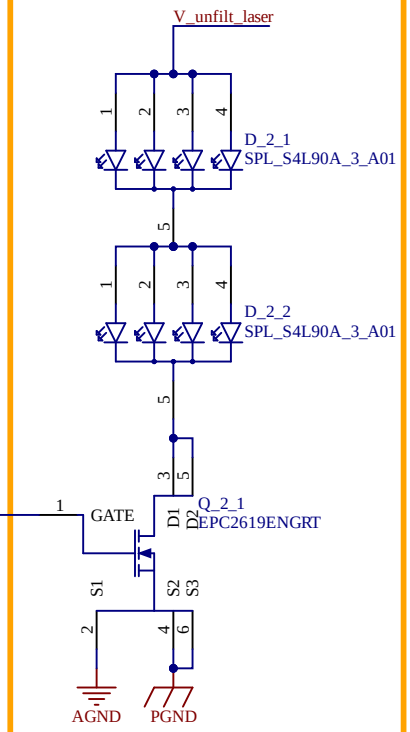
File: Pulser.SchDoc
Sheet: 2 / 2

V_UNFILT_LASER — V_unfilt_laser

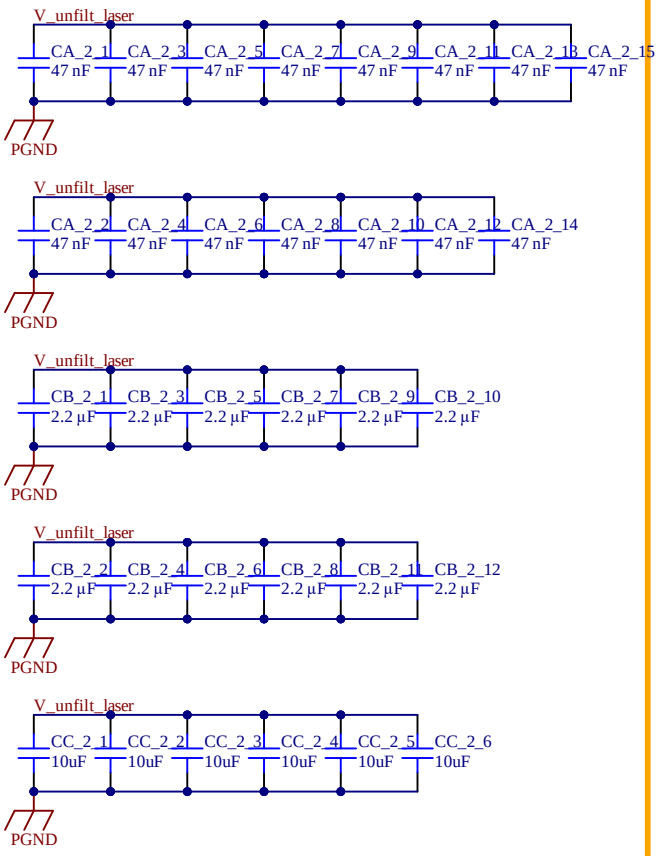
Pulser



Laser Diodes



Capacitor Bank



Mosfet source is ground star point. Provide sufficient external isolation where necessary to prevent ground loops. every AGND domain should be isolated indipendently

ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

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Pulser Laser Board

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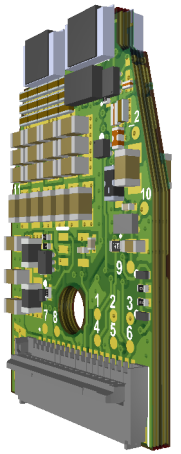
Pulses 4 laser modules with 320 A and 20-24 V
Do not pulse longer than 150 ns

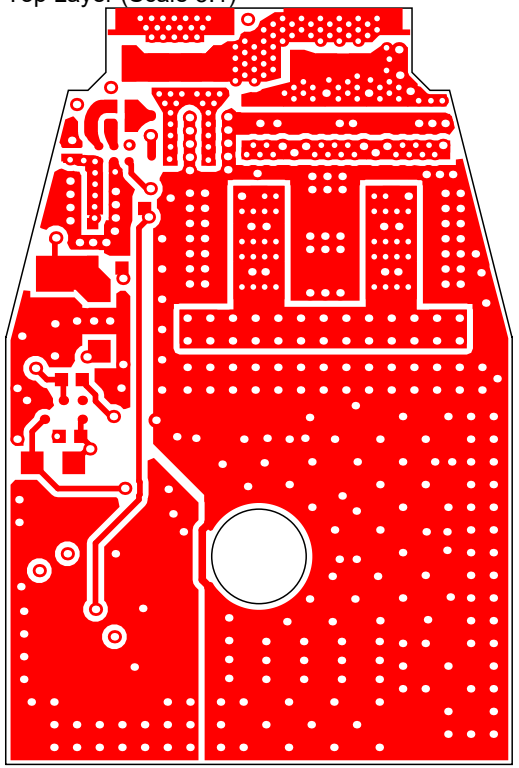
Drawn By: villanif
Checked By: liuxian

File: Pulser.SchDoc
Sheet: 2 / 2

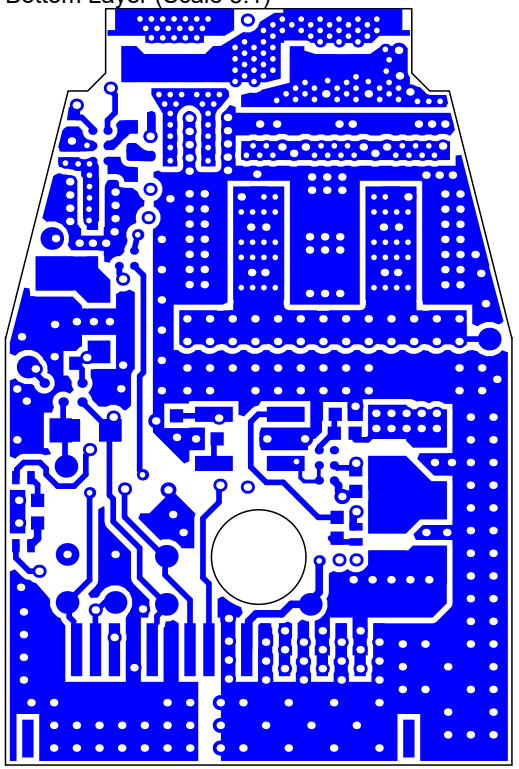
Realistic View



Top Layer (Scale 5:1)



Bottom Layer (Scale 5:1)



ETH
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Swiss Federal Institute of Technology Zurich

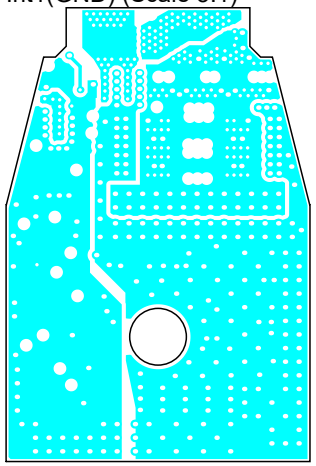
Laboratory: IIS
Date: 17/07/2025 14:39
Rev: 1.0
Variation fabrication

Project: HELIOS-R
LD Pulser - Layout Sheet

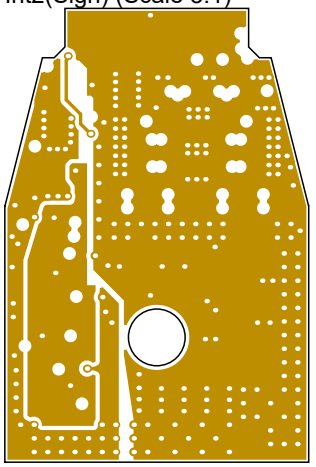
Drawn By: villanif
Checked By: *

File: PULSER_LAY.PCBDwf

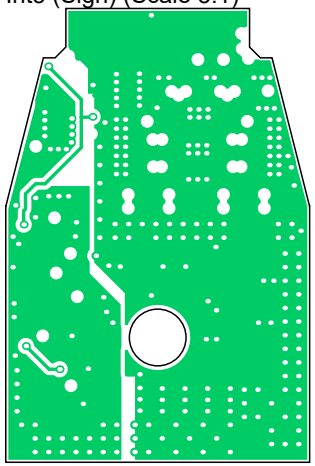
Int1(GND) (Scale 3:1)



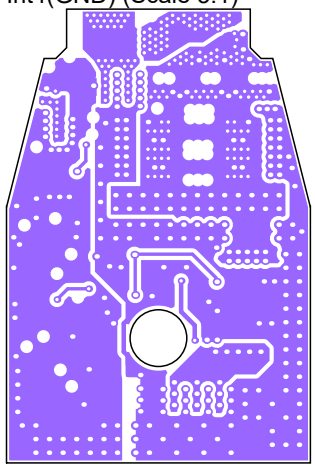
Int2(Sign) (Scale 3:1)



Int3 (Sign) (Scale 3:1)

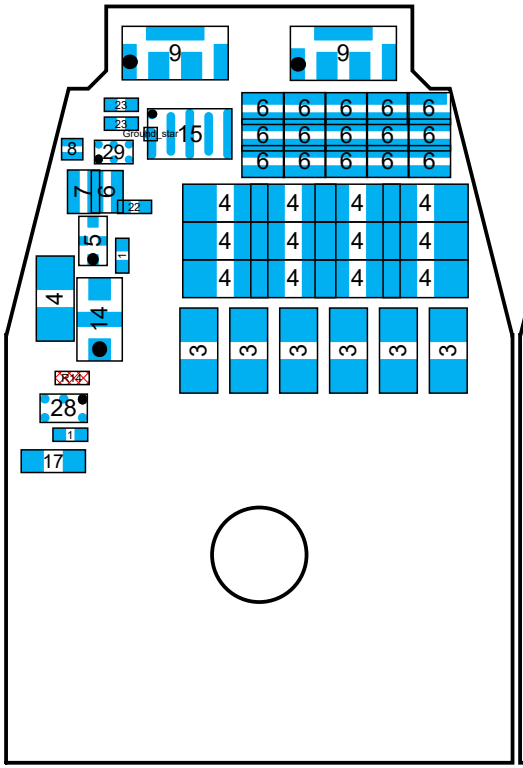


Int4(GND) (Scale 3:1)

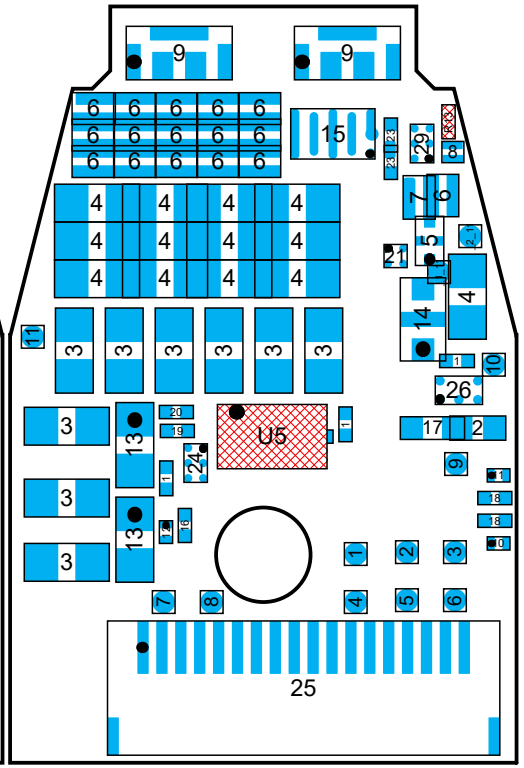


ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: HELIOS-R LD Pulser - Layout Sheet
Laboratory: IIS Date: 17/07/2025 14:39 Rev: 1.0 Variation: fabrication	Drawn By: villanif Checked By: *
File: PULSER_LAY.PCBDwf	Sheet: 2 / 2

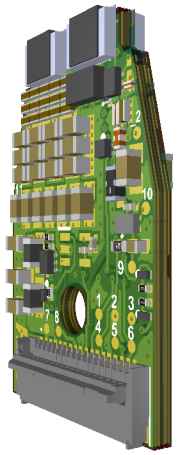
View from Top side (Scale 5:1)



View from Bottom side (Scale 5:1)



Realistic View



Notes:
- Number on assembly view = line # of component (see bom in page 2)
- Pin 1 is indicated by the black dot for each component
- Smallest components: 0201

ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: HELIOS-R LD Pulser - Assembly Sheet
Laboratory: IIS Date: 17/07/2025 14:39 Rev: 1.0 Variation fabrication	Drawn By: villanif Checked By: *
File: PULSER_ASM.PCBDwf	Sheet: 1 / 2

Bill Of Materials

Line #	Designator	Quantity	Description	Manufacturer Part Number 1
1	C1, C3, C5, C6, C7, C15	6	CAP CER 0.1UF 35V X5R 0201	GRM033R6YA104ME14D
2	C2	1	CAP CER 20PF 50V C0G/NP0 0402	GCM1555C1H200FA16D
3	C4, C13, C14, CC_1_1, CC_1_2, CC_1_3, CC_1_4, CC_1_5, CC_1_6, CC_2_1, CC_2_2, CC_2_3, CC_2_4, CC_2_5, CC_2_6	15	CAP CER 10UF 25V X5R 0603	ZRB18AR61E106ME01L
4	C_1_8, C_2_8, CB_1_1, CB_1_2, CB_1_3, CB_1_4, CB_1_5, CB_1_6, CB_1_7, CB_1_8, CB_1_9, CB_1_10, CB_1_11, CB_1_12, CB_2_1, CB_2_2, CB_2_3, CB_2_4, CB_2_5, CB_2_6, CB_2_7, CB_2_8, CB_2_9, CB_2_10, CB_2_11, CB_2_12	26	CAP CER 2.2UF 50V X5R 0603	GRM188R71A225KE15D
5	C_1_9, C_2_9	2	CAP Feed Through, 470 nF, 6.3V, 2A, 3 Pin(s)	NFM15PC474R0J3D
6	C_1_10, C_2_10, CA_1_1, CA_1_2, CA_1_3, CA_1_4, CA_1_5, CA_1_6, CA_1_7, CA_1_8, CA_1_9, CA_1_10, CA_1_11, CA_1_12, CA_1_13, CA_1_14, CA_1_15, CA_2_1, CA_2_2, CA_2_3, CA_2_4, CA_2_5, CA_2_6, CA_2_7, CA_2_8, CA_2_9, CA_2_10, CA_2_11, CA_2_12, CA_2_13, CA_2_14, CA_2_15	32	CAP CER 47 nF, 50V, 20% X7R 0204	CGAEA1X7R1H473M030BC
7	C_1_11, C_2_11	2	CAP LOW L CER 1UF 6.3V X7T 0204	LLL152D70J105ME01D
8	C_1_12, C_2_12	2	CAP LOW L CER 33nF 25V X5R 0102	LLL03TR61E333KE01L
9	D_1_1, D_1_2, D_2_1, D_2_2	4	Diode Laser	SPLS4L90A_3A01
10	LED1	1	Diode LED RED 10 mA @ 1.93 V Iv=40	APG0603SEC-E-TT
11	LED2	1	Diode LED BLUE 10 mA @ 2.9 V Iv=60	APG0603VBC-A1-5MAV
12	LED3	1	Diode LED GREEN 5 mA @ 2.85 V Iv=80(?)	APG0603ZGC-5MAV
13	FB1, FB2	2	FERRITE BEAD 100 OHM 0603 1LN	BLM18SP101SN1D
14	FL_1_1, FL_2_1	2	LC Filter	NFL18ZT506H1A3D
15	Q_1_1, Q_2_1	2	Transistor eGaN	EPC2619ENGRT
16	R3	1	RES SMD 51 OHM 1% 1/20W 0201	ERJ-1GNF51R0C
17	R2, R12	2	RES SMD 4.99KOHM 0.1% 1/16W 0402	ERA-2AEB4991X
18	R1, R4	2	RES SMD 470 OHM 1% 1/20W 0201	ERJ-1GNF4700C
19	R6	1	RES SMD 1MOHM 1% 1/20W 0201	ERJ-U01F1004C
20	R7	1	RES SMD 100 kOHM 0.5% 1/20W 0201	ERJ-1RHD1003C
21	U1	1	IC temperature sensor	LM94023BITME/NOPB
22	R9	1	RES SMD 4.99 kOHM 1% 1/20W 0201	ERJ-1GNF4991C
23	R_1_10, R_1_11, R_2_10, R_2_11	4	RES SMD 2 OHM 1% 1/20W 0201	ERJ-1GNJ2R0C
24	U4	1	Operational Amplifier	MAX40007ANT+T
25	J1	1	Conn FPC 18 POS 0.5mm	503480-1800
26	U2	1	IC Single 2-Input Positive-AND Gate, YZP0005ADAD, LARGE T&R	SN74LVC1G08YZPR
28	U7	1	IC Single Inverter Buffer/Driver With Open-Drain Output, YZP0005ADAD, LARGE T&R	SN74LVC1G06YZPR
29	U_1_6, U_2_6	2	IC Pulser	LMG1020YFFR

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Eidgenössische Technische Hochschule Zürich
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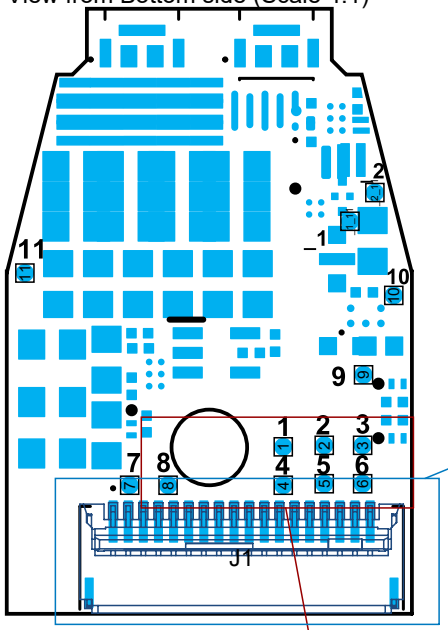
Laboratory: IIS
Date: 17/07/2025 14:39
Rev: 1.0
Variation: fabrication

Project: HELIOS-R
LD Pulser - Assembly Sheet

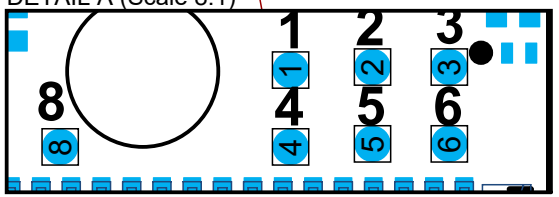
Drawn By: villanif
Checked By: *

File: PULSER_ASM.PCBDwf

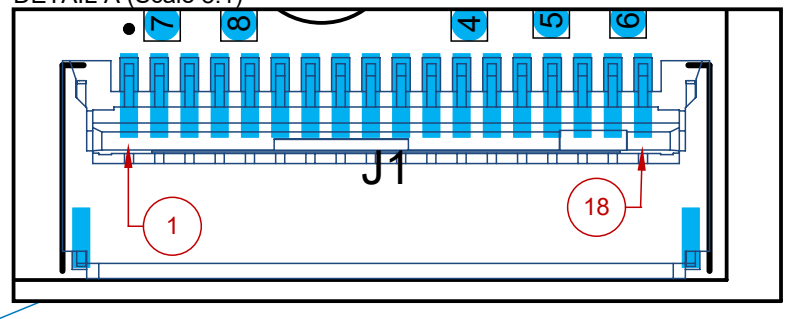
View from Bottom side (Scale 4:1)

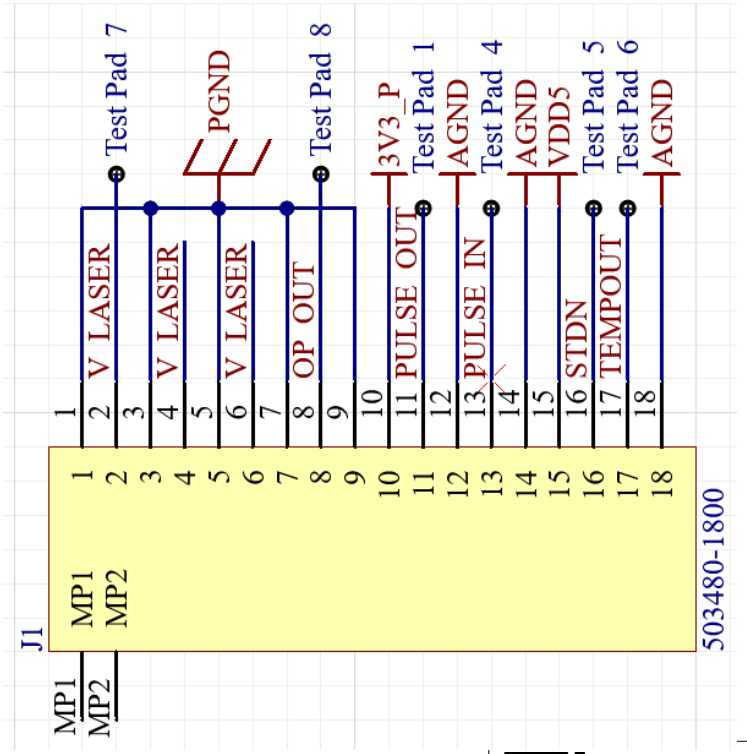


DETAIL A (Scale 8:1)

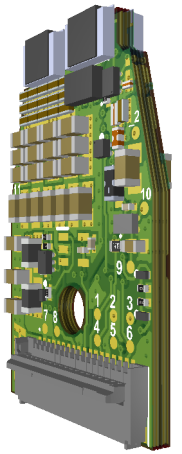


DETAIL A (Scale 8:1)





Realistic View



Table

Test pad designator	Net	GND domain
1	PULSE_OUT	AGND
2	AGND	AGND
3	VDD_5	AGND
4	PULSE_IN	AGND
5	STDN	AGND
6	TEMPOUT	PGND
7	V_LASER	PGND
8	OP_OUT	AGND
9	PULSE_IN - After RC	PGND
10	PGOOD	PGND
11	V_unfilt_laser	AGND
_1	Pulser 1 supply	AGND
_2	Pulser 2 supply	AGND

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Laboratory: IIS
Date: 17/07/2025 14:39
Rev: 1.0
Variation fabrication

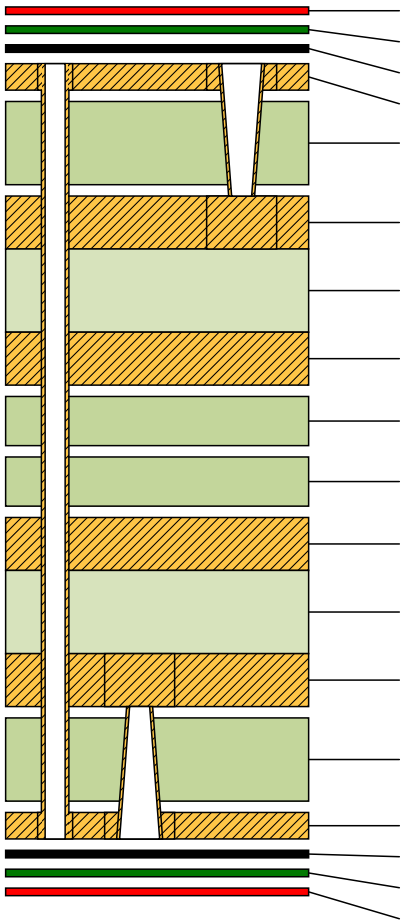
Project: HELIOS-R
LD Pulser - Connector Sheet

Drawn By: villanif
Checked By: *

File: PULSER_CON.PCBDwf

Sheet: 1 / 1

Layer Stack Legend

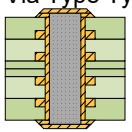


Material	Layer	Thickness	Type	Gerber	Weight
	Top Overlay		Legend	GTO	
Surface Material	Top Solder	0.001mm	Solder Mask	GTS	
Nickel, Gold	Top Surface Finish	0.001mm	Surface Finish		
CF-004	**Top Layer**	**0.035mm**	**Signal**	**GTL**	**1oz**
Prepreg		*0.110mm*	*Dielectric*		
CF-004	**Int1(GND)**	**0.070mm**	**Signal**	**G1**	**2oz**
Core		*0.110mm*	*Dielectric*		
CF-004	**Int2(Sign)**	**0.070mm**	**Signal**	**G2**	**2oz**
Prepreg		*0.065mm*	*Dielectric*		
Prepreg		*0.065mm*	*Dielectric*		
CF-004	**Int3 (Sign)**	**0.070mm**	**Signal**	**G3**	**2oz**
Core		*0.110mm*	*Dielectric*		
CF-004	**Int4(GND)**	**0.070mm**	**Signal**	**G4**	**2oz**
Prepreg		*0.110mm*	*Dielectric*		
CF-004	**Bottom Layer**	**0.035mm**	**Signal**	**GBL**	**1oz**
Nickel, Gold	Bottom Surface Finish	0.001mm	Surface Finish		
Surface Material	Bottom Solder	0.001mm	Solder Mask	GBS	
	Bottom Overlay		Legend	GBO	

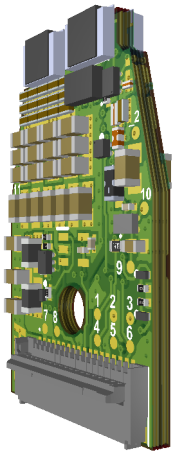
Total thickness: 0.924mm

Through Hole Vias: filled with Resin, Via in Pad, Capped
Microvias: Filled with conductive material, Capped

Via Type Type 7 (Scale 16:1)

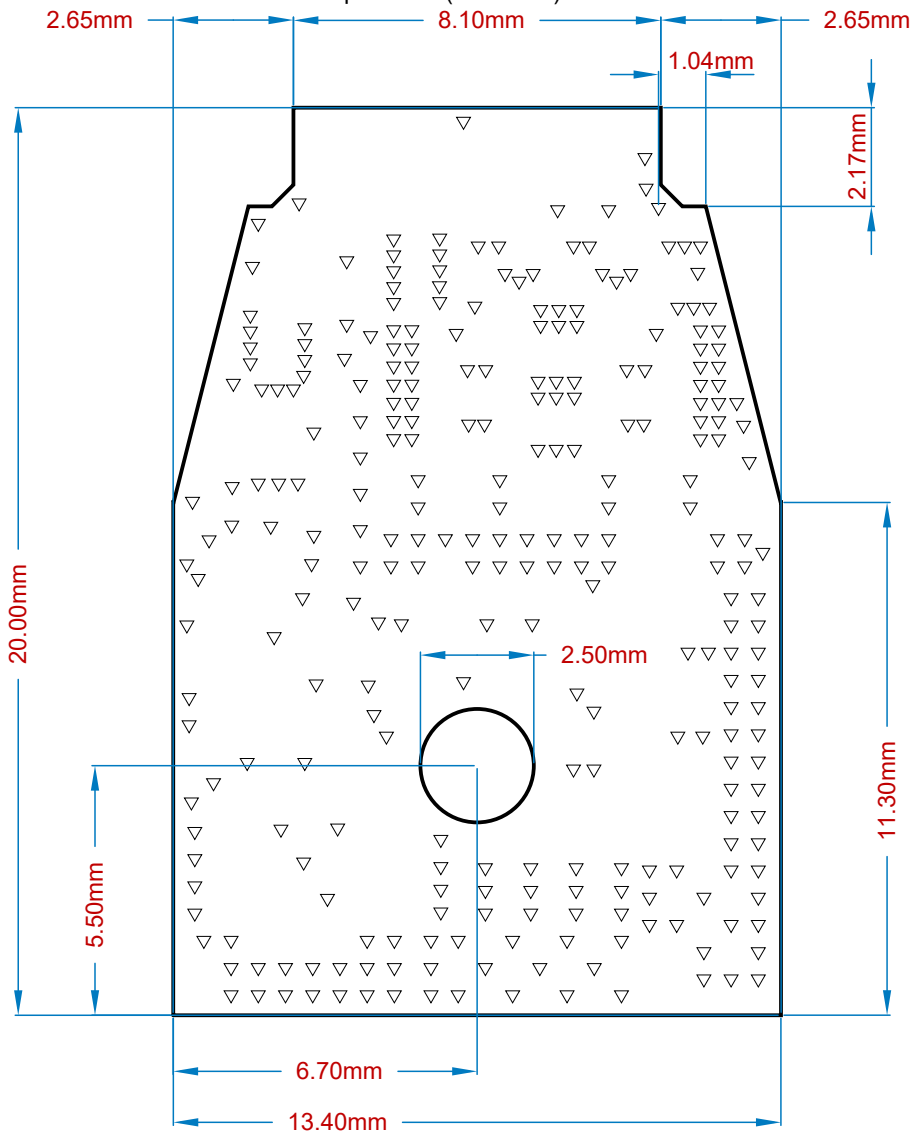


Realistic View



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: HELIOS-R LD Pulser - Manufacturing Sheet
Laboratory: IIS Date: 17/07/2025 14:39 Rev: 1.0 Variation fabrication	Drawn By: villanif Checked By: *
File: PULSER_MAN.PCBDwf	Sheet: 1 / 2

Drill View vias top-bottom (Scale 6:1)



Drill Table - top to bottom

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad
▽	278	0.20mm	Plated	Top Layer - Bottom Layer	Via
	278 Total				

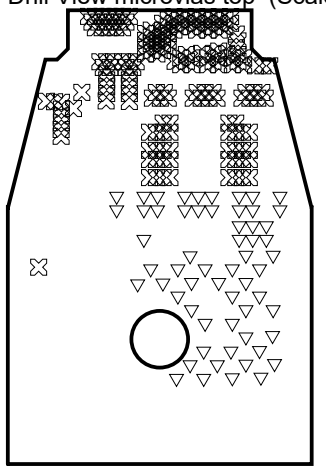
Drill Table - microvias - top layer

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad
⊠	180	0.15mm	Plated	[UVIA] Top Layer - Int1(GND)	Via
▽	59	0.20mm	Plated	[UVIA] Top Layer - Int1(GND)	Via
	239 Total				

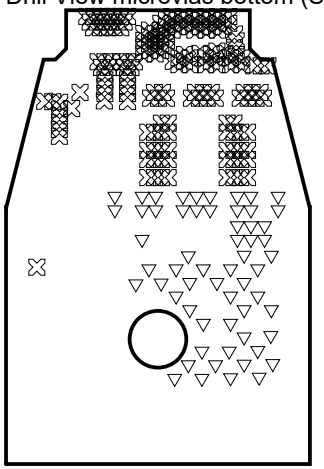
Drill Table - microvias - bottom layer

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad
⊠	182	0.15mm	Plated	[UVIA] Int4(GND) - Bottom Layer	Via
▽	45	0.20mm	Plated	[UVIA] Int4(GND) - Bottom Layer	Via
	227 Total				

Drill View microvias top (Scale 3:1)



Drill View microvias bottom (Scale 3:1)



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich

Laboratory: IIS
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Variation fabrication

Project: HELIOS-R

LD Pulser - Manufacturing Sheet

Drawn By: villanif
Checked By: *

File: PULSER_MAN.PCBDwf