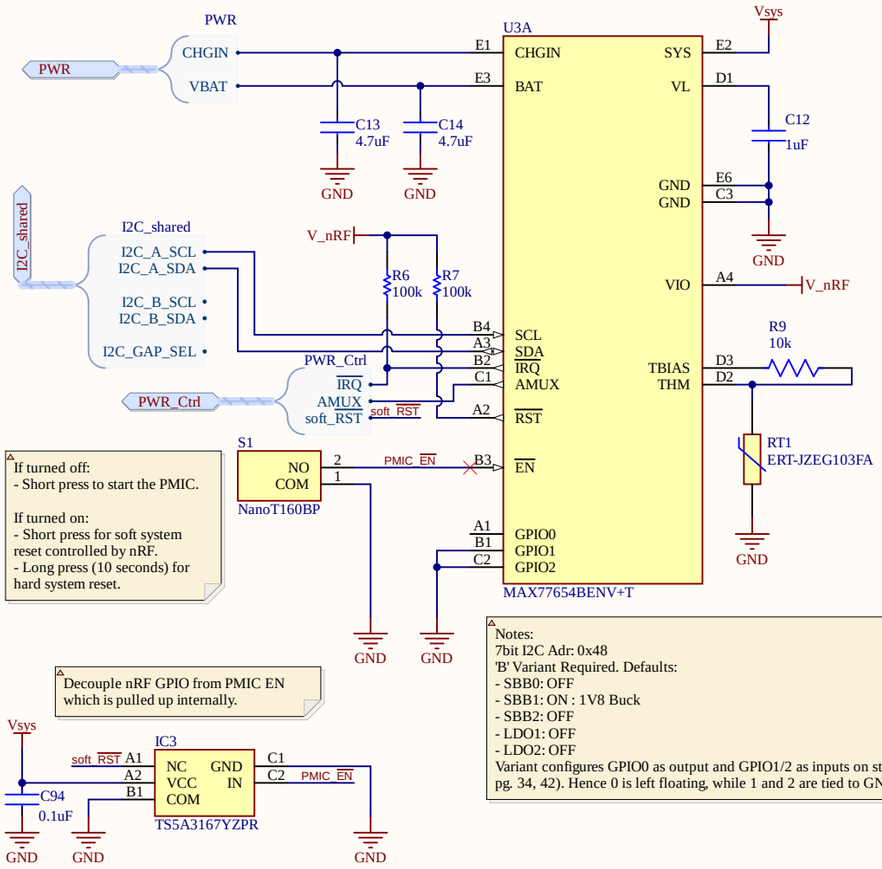
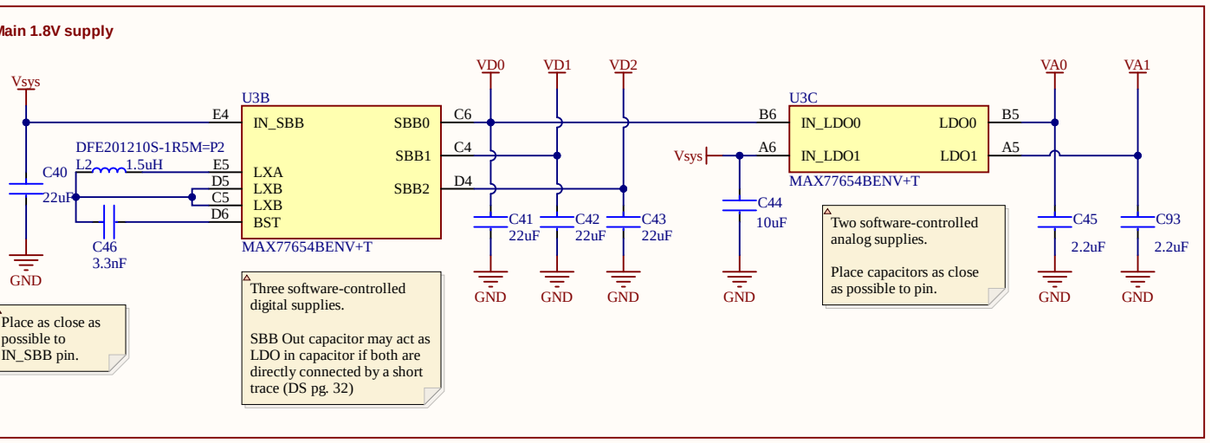
PMIC

VSYS turns on when:
- CHGIN applied, or
- BAT disconnected and then reconnecrec, or
- Short press button S1 (with valid BAT)

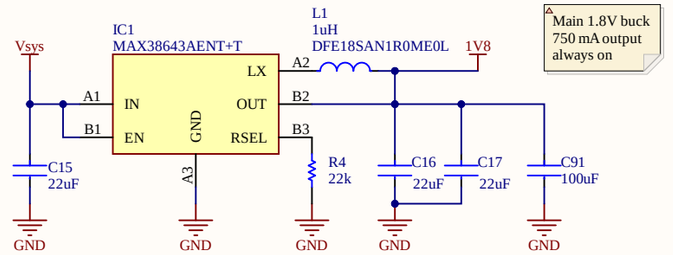
VSYS turns off when:
- factory ship mode (BAT to VSYS switch open), or
- factory ship mode requested through I2C command



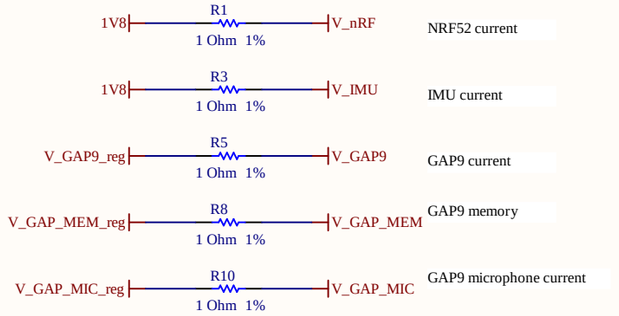
Main 1.8V supply



Main 1.8V supply

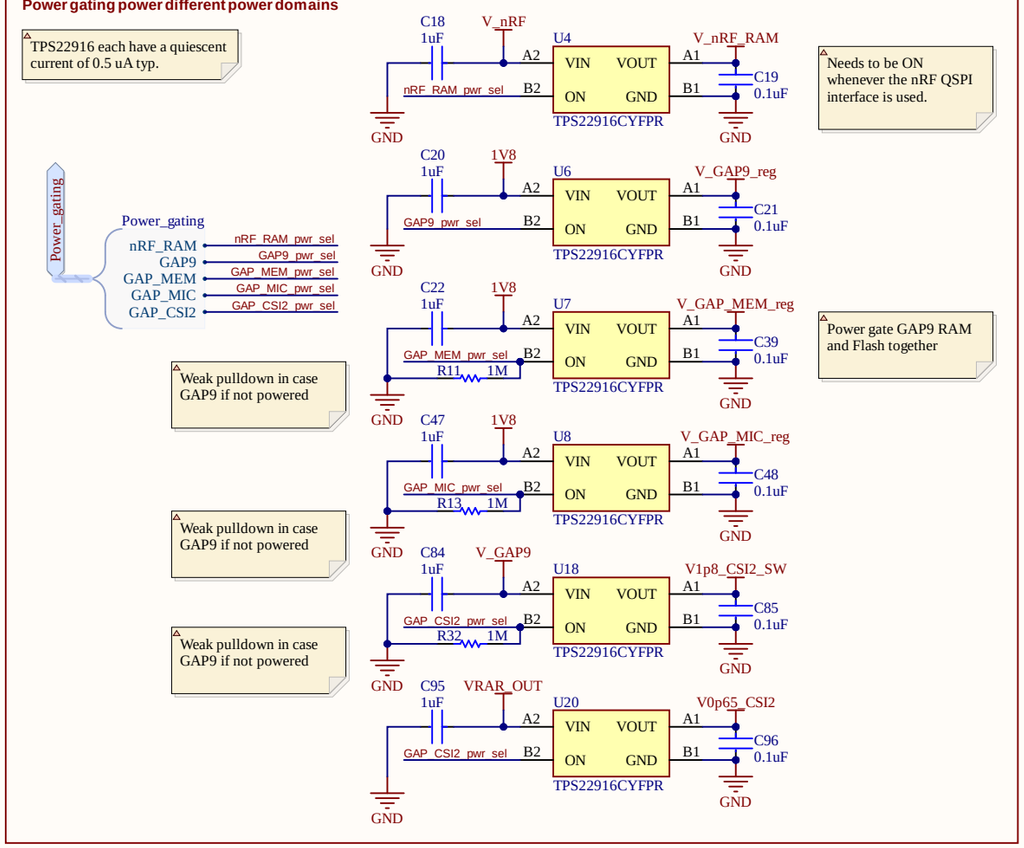


Power measurement shunts



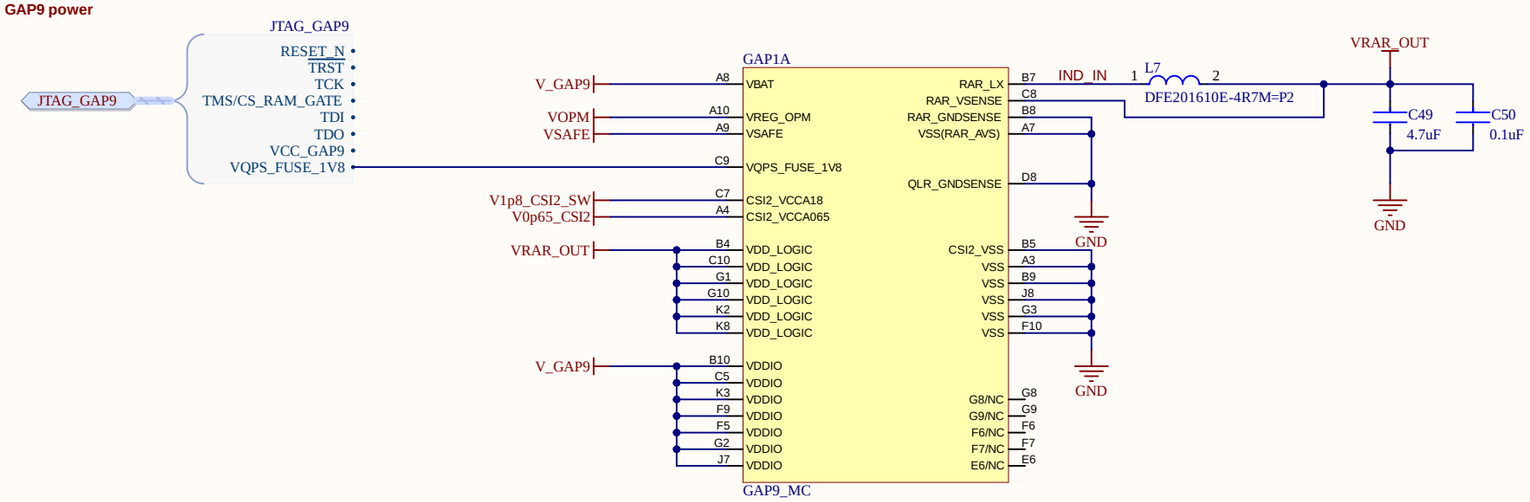
Power gating power different power domains

TPS22916 each have a quiescent current of 0.5 uA typ.

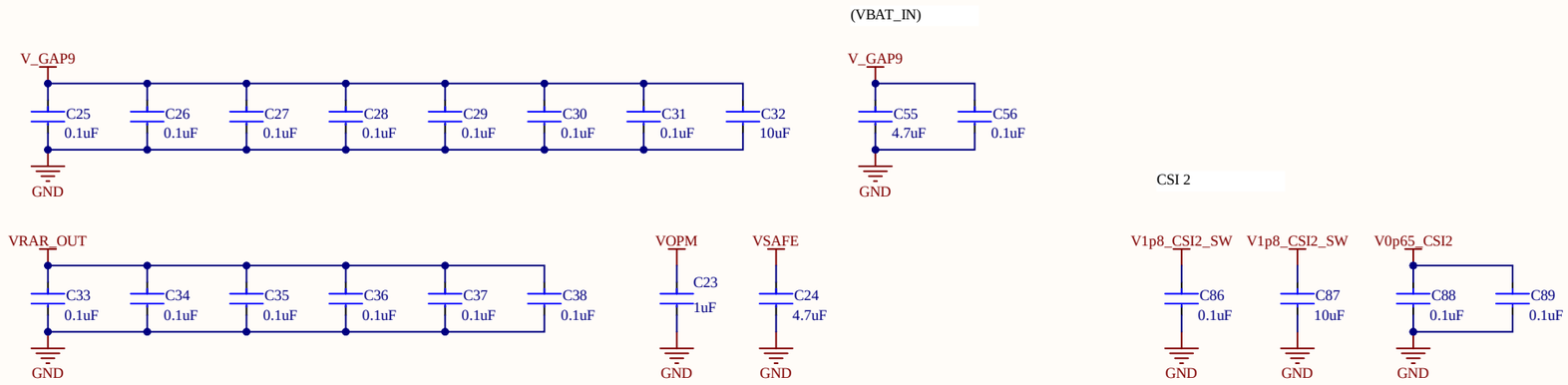


Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich		Project: SENSEI Base Board - Power	
Drawing number: 1 Rev: v1.0	Format: A3	Laboratory: Integrated Systems Laboratory	Sheet: 00_POWER.SchDoc
Date: 23.09.2024 16:16:22		Drawn by: Sebastian Frey	Page 1 of 12
File: H:\Documents\SENSEI\Hardware\sensei-sensor-shield\Hardware\UT_baseBoard\Hardware\01_Mainboard\00_POWER.SchDoc			

GAP9 power



GAP9 bypass CAPs



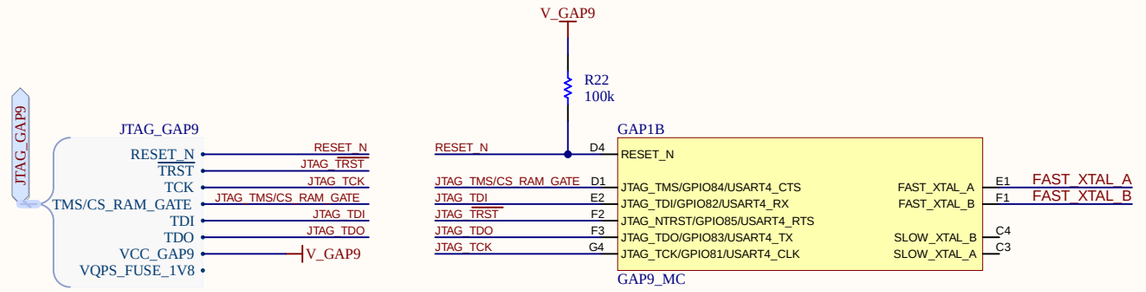
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

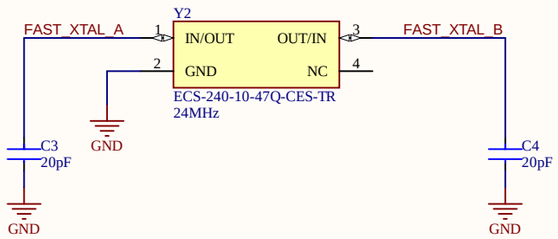
Project: SENSEI Base Board - GAP Power

Drawing number: 2	Rev: v1.0	Format: A3	Laboratory: Integrated Systems Laboratory	Sheet: 01_GAP_POWER.SchDoc	
Date: 23.09.2024 16:16:23			Drawn by: Sebastian Frey	Page 2 of 12	

File: H:\Documents\SENSEI\Hardware\sensei-sensor-shield\Hardware\UT_baseBoard\Hardware\01_Mainboard\01_GAP_POWER.SchDoc

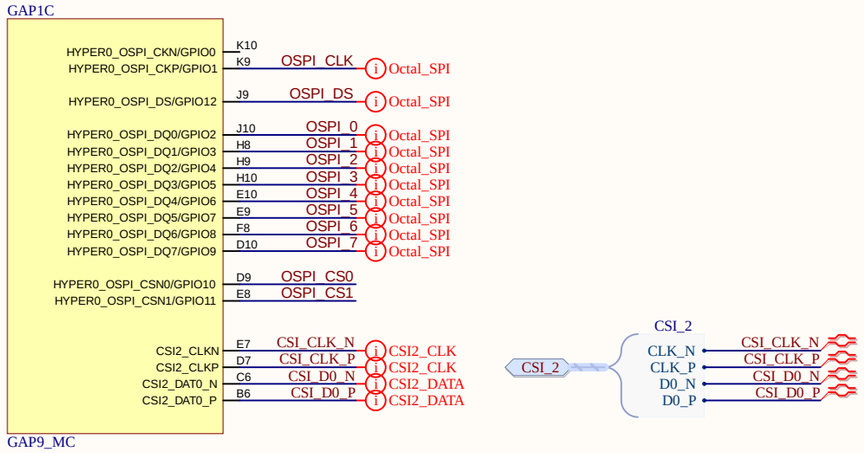
GAP9 JTAG and XTALs



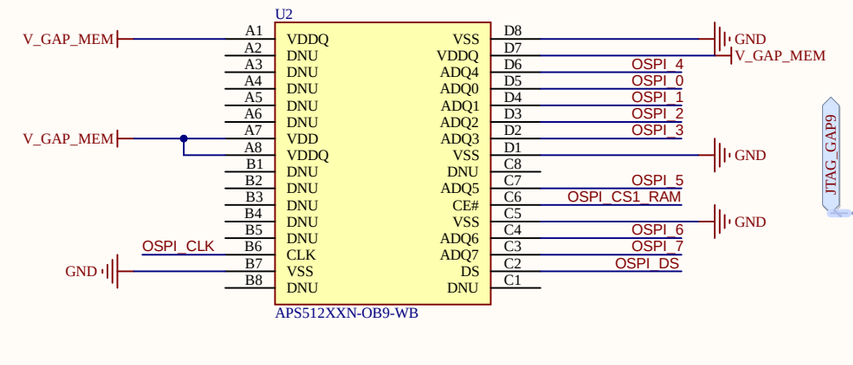


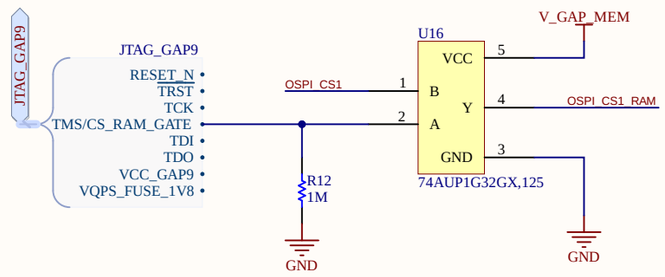
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich			Project: SENSEI Base Board - GAP JTAG & XTAL	
Drawing number: 3	Rev: v1.0	Format: A3	Laboratory: Integrated Systems Laboratory	Sheet: 02_GAP_JTAG_XTALs.SchDoc
Date: 23.09.2024 16:16:23			Drawn by: Sebastian Frey	Page 3 of 12
File: H:\Documents\SENSEI\Hardware\sensei-sensor-shield\Hardware\UT_baseBoard\Hardware\01_Mainboard\02_GAP_JTAG_XTALs.SchDoc				

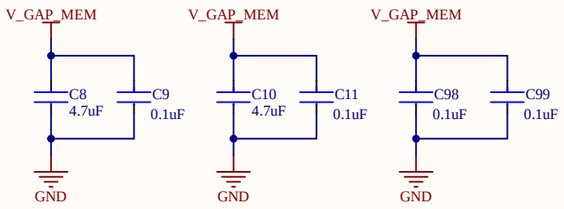
GAP9 memory and camera interface



GAP9 PSRAM







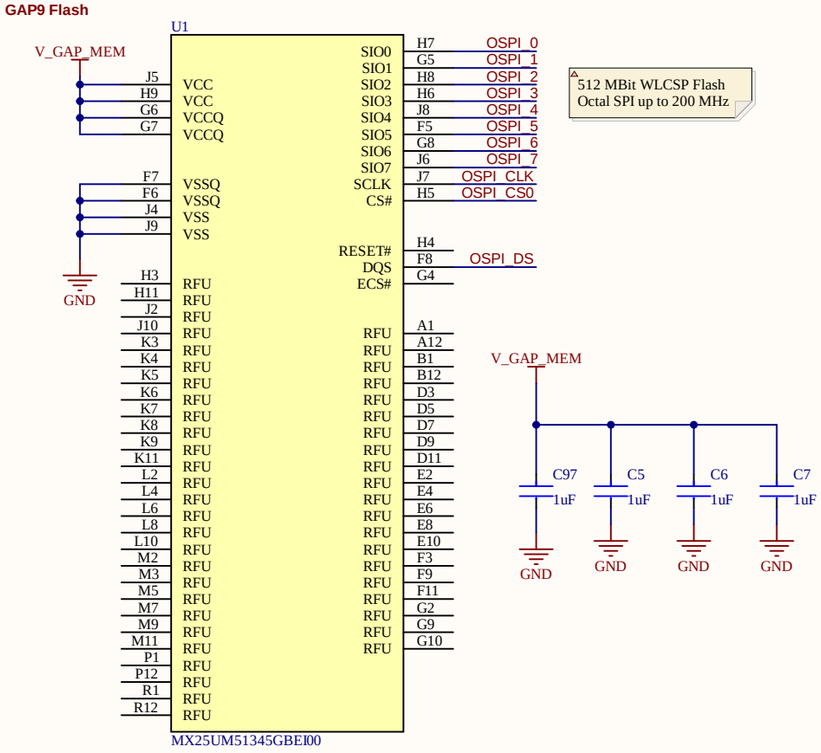
512 MBit WLCSP PSRAM
Octal SPI up to 200 MHz

256 MBit APS256XXN-OBR can be used as a drop-in replacement

OR Gate transmits ChipSelect transparently if JTAG_TMS/CS_RAM_GATE is not driven or is Logic-0.
However if JTAG_TMS/CS_RAM_GATE (from always-on GPIO) is high, then ChipSelct to RAM is forced high.
This is to enable leaving RAM in deep power down (ChipSelect must stay deasserted) while GAP9 goes to Sleep (its ChipSelect output will go low).

This is not needed for the Flash as it exits Deep Power Down only upon reception of suitable OpCode (CS ignored).

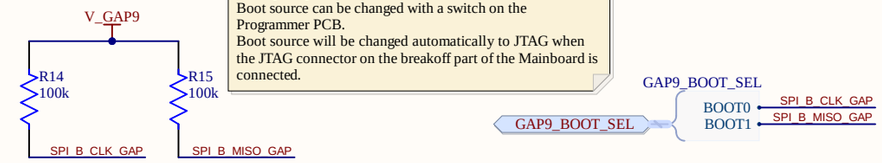
GAP9 Flash



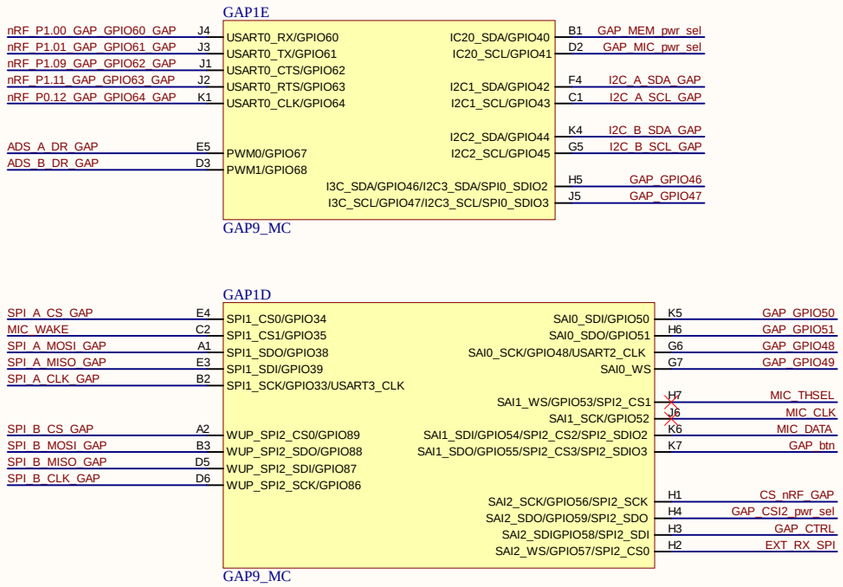
512 MBit WLCSP Flash
Octal SPI up to 200 MHz

ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich			Project: SENSEI Base Board - GAP Memory
Drawing number: 4 Rev: v1.0	Format: A3	Laboratory: Integrated Systems Laboratory	Sheet: 03_GAP_MEM.SchDoc
Date: 23.09.2024 16:16:23		Drawn by: Sebastian Frey	Page 4 of 12
File: H:\Documents\SENSEI\Hardware\sensei-sensor-shield\Hardware\UT_baseBoard\Hardware\01_Mainboard\03_GAP_MEM.SchDoc			

GAP9 boot select

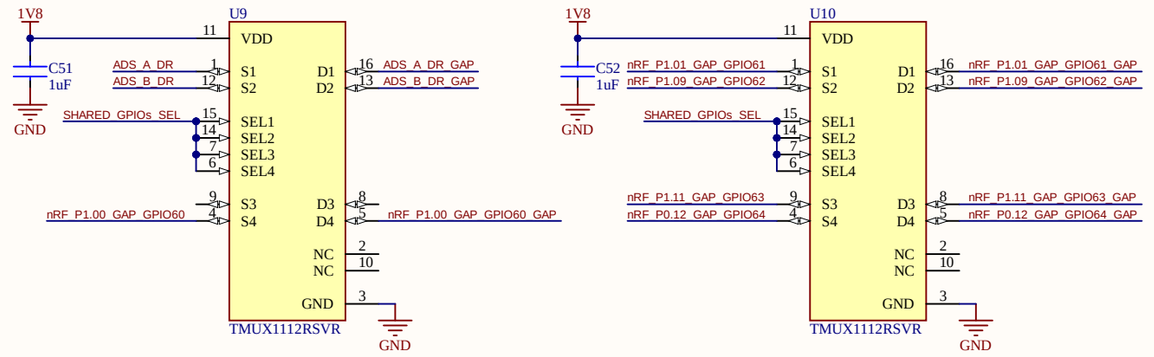


GAP9 GPIOs

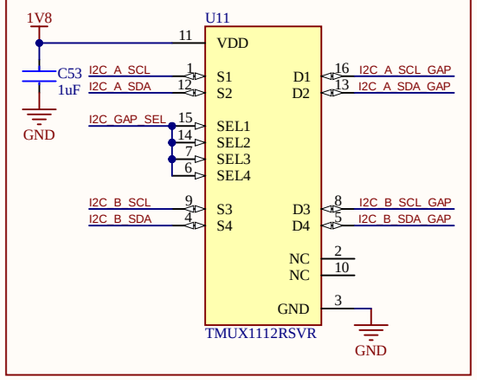


TMUX1112 each have a supply current of 0.001 uA typ.

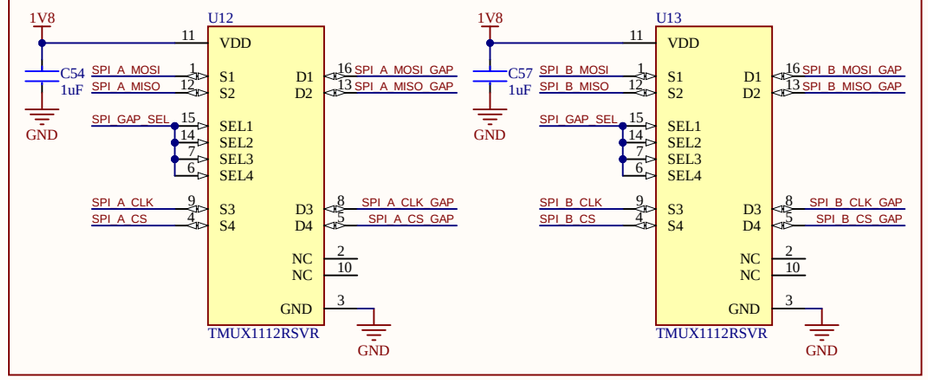
Possibility to isolate GAP9 from shared GPIOs

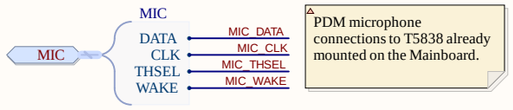


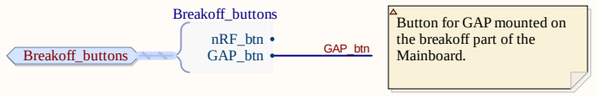
Possibility to isolate GAP9 from shared I2C bus A and B

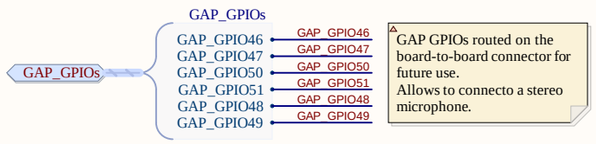


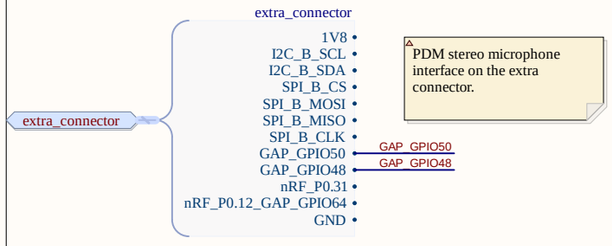
Possibility to isolate GAP9 from shared SPI bus A and B

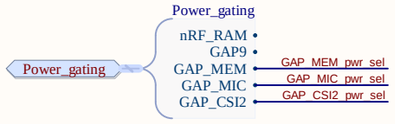


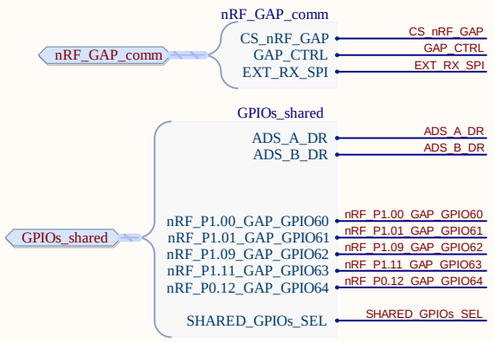


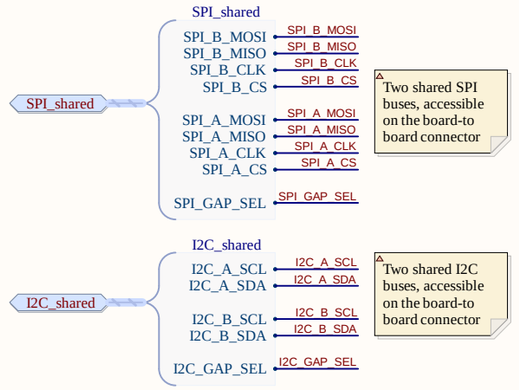












ETH

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

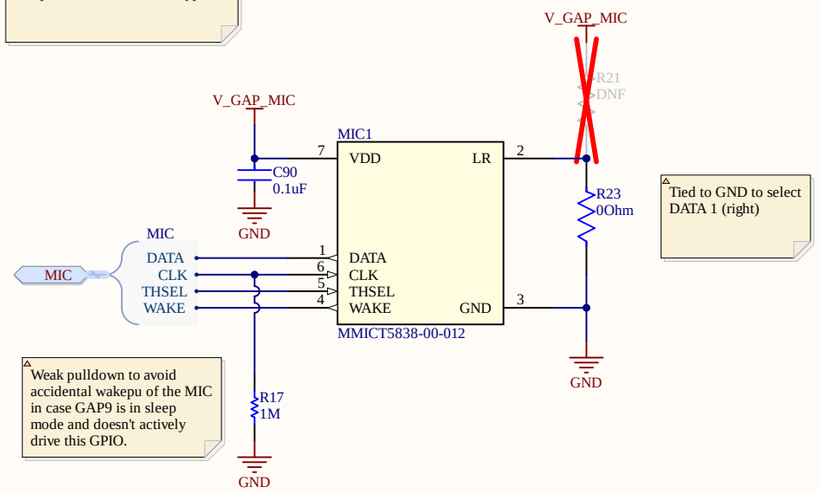
Project:

SENSEI Base Board - GAP GPIO

Drawing number:	5	Rev: v1.0	Format:	Laboratory: Integrated Systems Laboratory	Sheet: 04_GAP_GPIO.SchDoc
Date:	23.09.2024 16:16:23		A3	Drawn by: Sebastian Frey	Page 5 of 12
File:	H:\Documents\SENSEI\Hardware\sensei-sensor-shield\Hardware\UT_baseBoard\Hardware\01_Mainboard\04_GAP_GPIO.SchDoc				

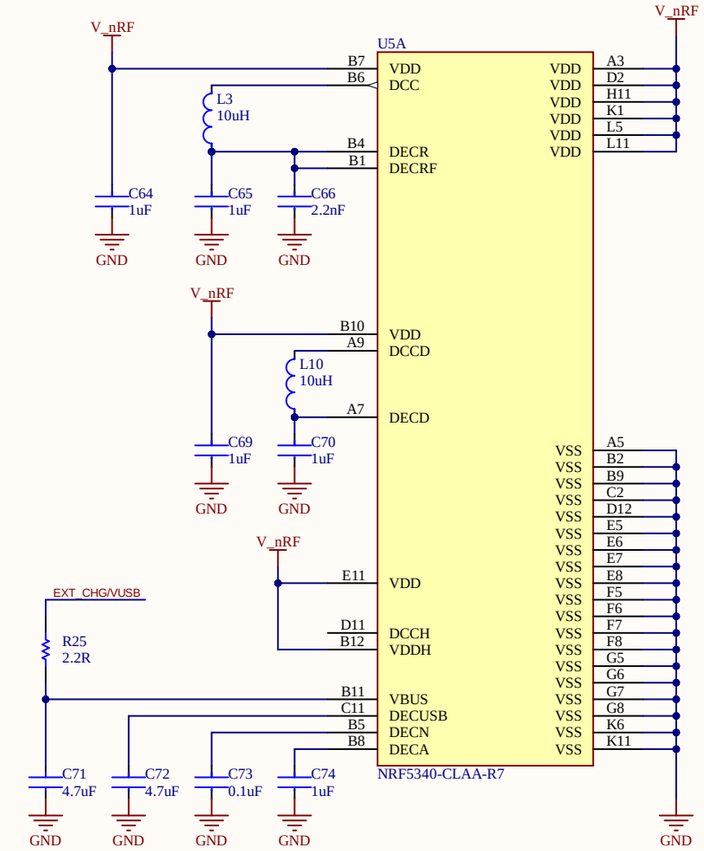
GAP9 PDM microphone

Not power gated.
Sleep mode current: 0.8 uA typ.

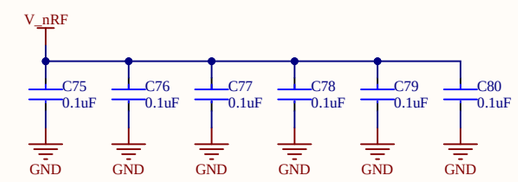


Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich			Project: SENSEI Base Board - GAP MIC	
Drawing number: 6	Rev: v1.0	Format: A3	Laboratory: Integrated Systems Laboratory	Sheet: 05_GAP_MIC.SchDoc
Date: 23.09.2024 16:16:23			Drawn by: Sebastian Frey	Page 6 of 12
File: H:\Documents\SENSEI\Hardware\sensei-sensor-shield\Hardware\UT_baseBoard\Hardware\01_Mainboard\05_GAP_MIC.SchDoc				

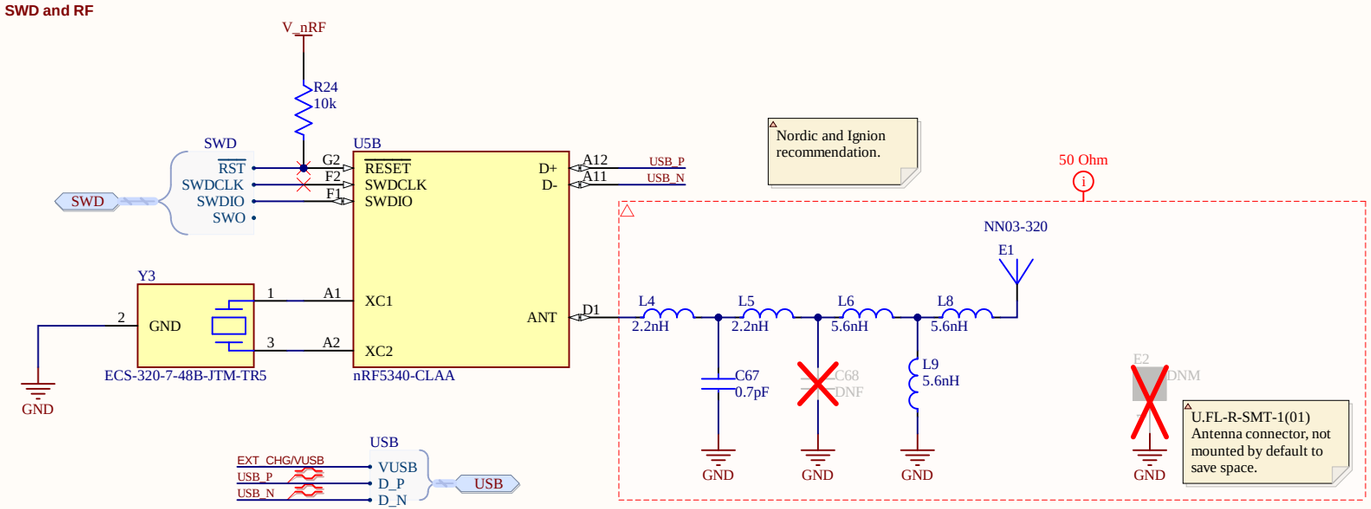
nRF53 power



Bypass CAPs

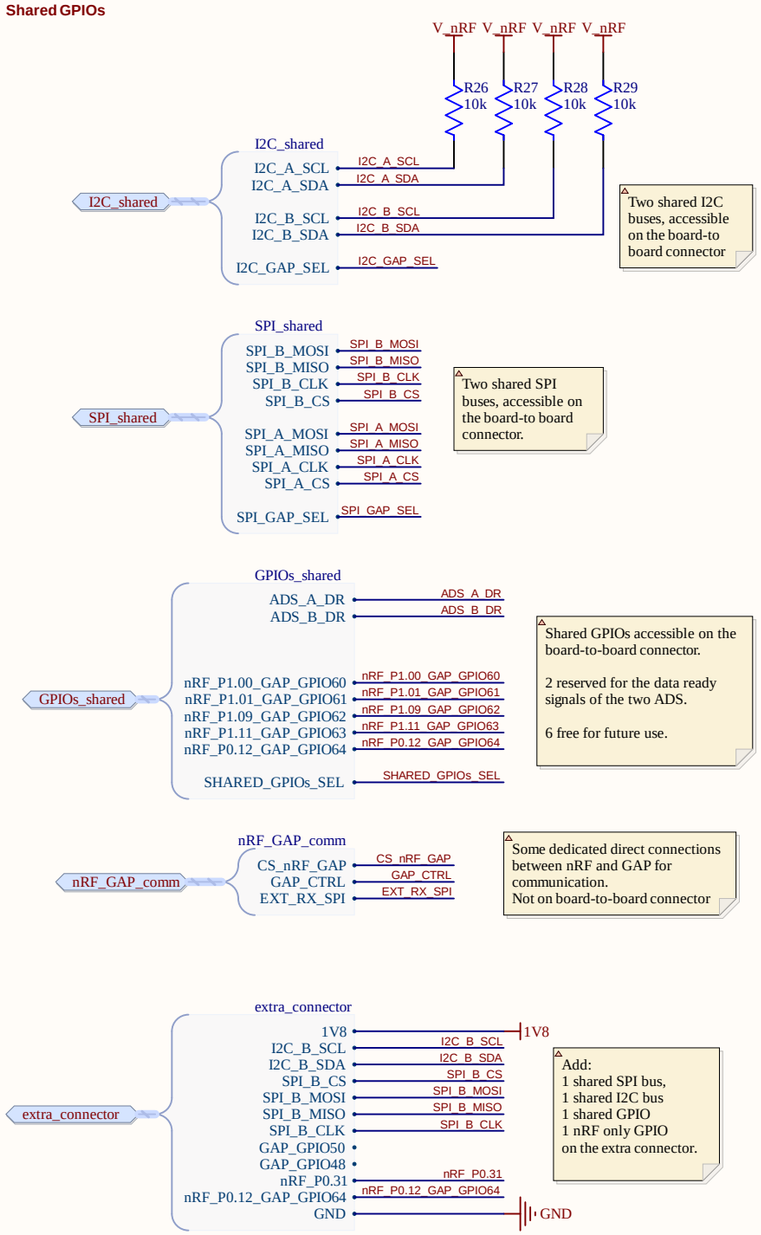


SWD and RF

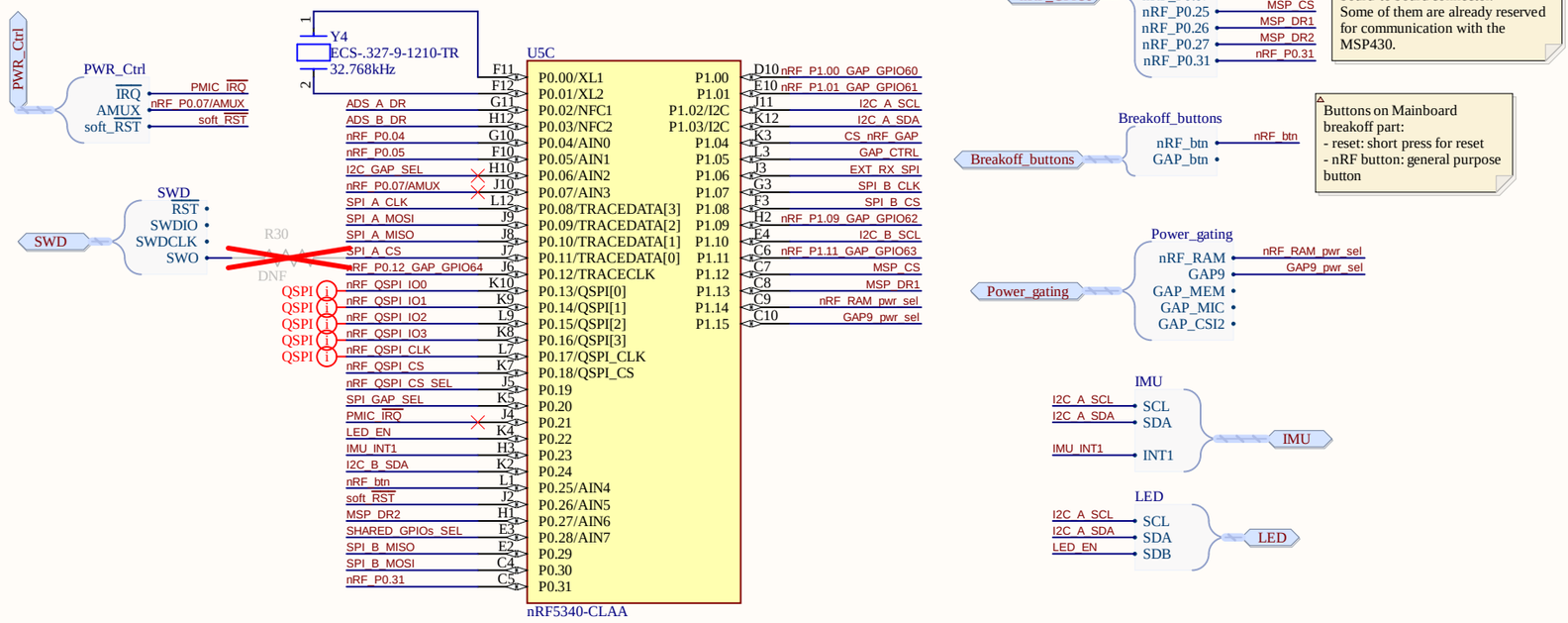


Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: SENSEI Base Board - nRF Power		
Drawing number: 7 Rev: v1.0	Format: A3	Laboratory: Integrated Systems Laboratory	Sheet: 06_nRF_POWER_SWD_RF.SchDoc
Date: 23.09.2024 16:16:23		Drawn by: Sebastian Frey	Page 7 of 12
File: H:\Documents\SENSEI\Hardware\sensei-sensor-shield\Hardware\UT_baseBoard\Hardware\01_Mainboard\06_nRF_POWER_SWD_RF.SchDoc			

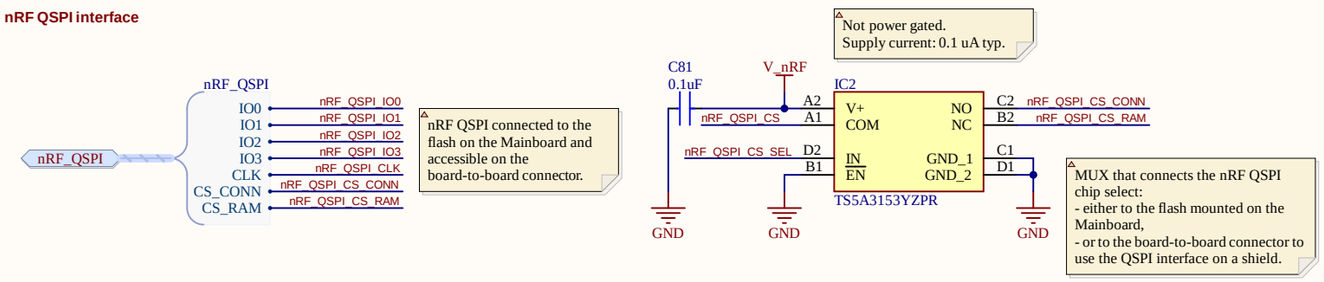
Shared GPIOs



nRF GPIOs

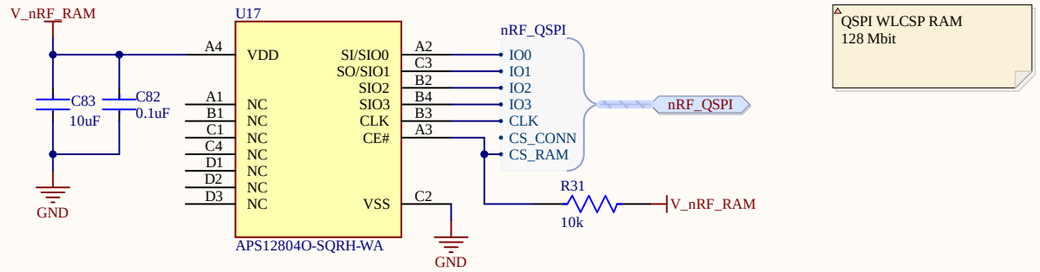


nRF QSPI interface



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich			Project: SENSEI Base Board - nRF GPIO
Drawing number: 8	Rev: v1.0	Format: A3	Laboratory: Integrated Systems Laboratory
Date: 23.09.2024 16:16:23			Drawn by: Sebastian Frey
Sheet: 07_nRF_GPIO.SchDoc			Page 8 of 12
File: H:\Documents\SENSEI\Hardware\sensei-sensor-shield\Hardware\UT_baseBoard\Hardware\01_Mainboard\07_nRF_GPIO.SchDoc			

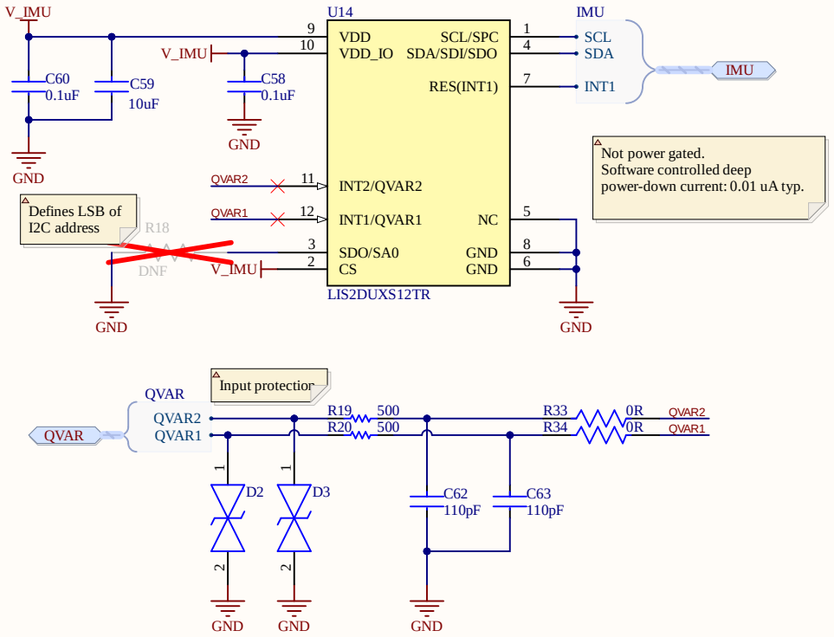
nRF QSPI RAM



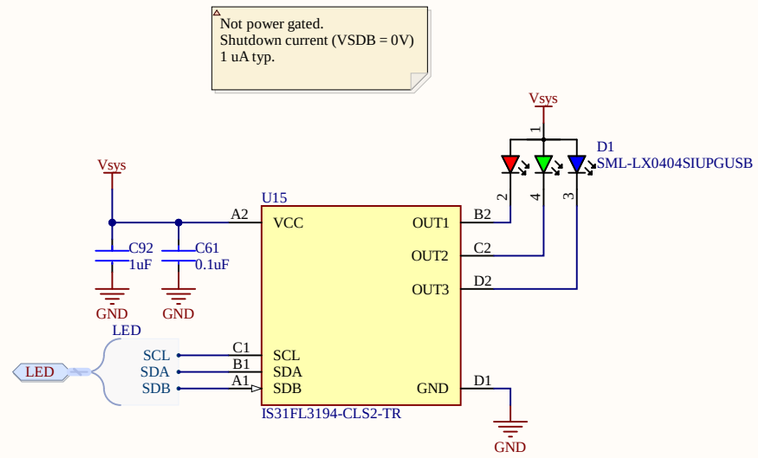
QSPI WLCSP RAM
128 Mbit

Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: SENSEI Base Board - nRF RAM		
Drawing number: 9 Rev: v1.0 Date: 23.09.2024 16:16:23	Format: A3	Laboratory: Integrated Systems Laboratory Drawn by: Sebastian Frey	Sheet: 08_nRF_RAM.SchDoc Page 9 of 12
File: H:\Documents\SENSEI\Hardware\sensei-sensor-shield\Hardware\UT_baseBoard\Hardware\01_Mainboard\08_nRF_RAM.SchDoc			

IMU with QVAR sensing

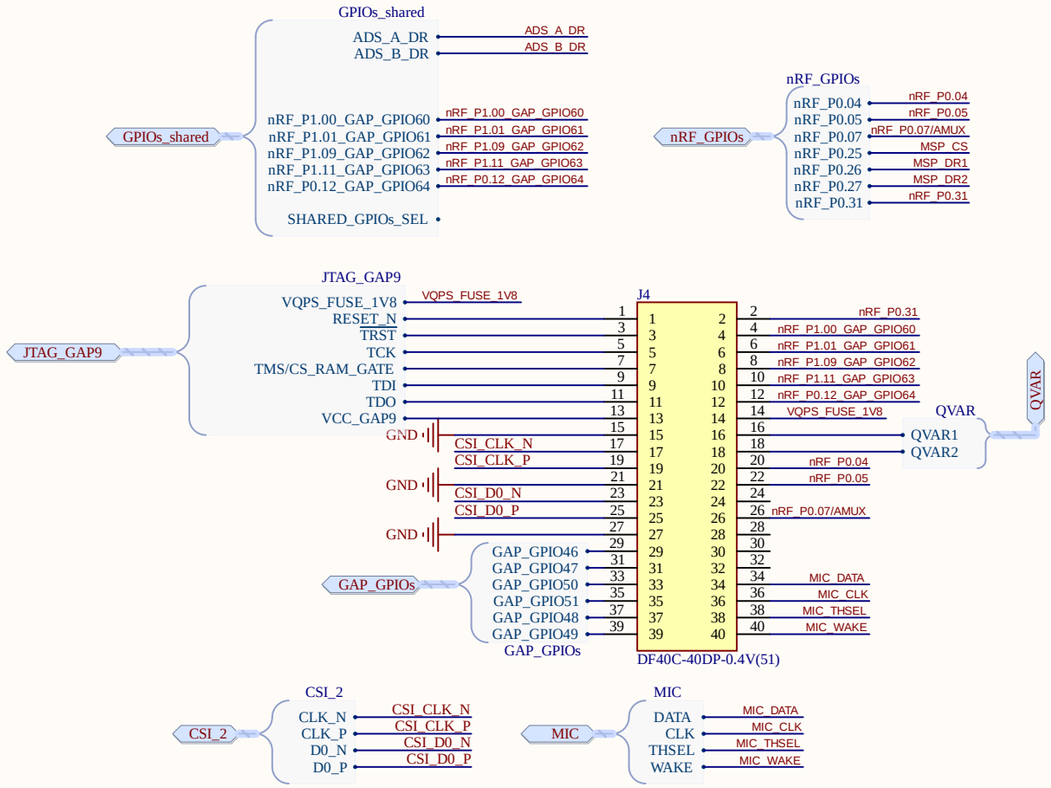


RGB LED



Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: SENSEI Base Board - Shared Peripherals		
Drawing number: 10 Rev: v1.0 Date: 23.09.2024 16:16:23	Format: A3	Laboratory: Integrated Systems Laboratory Drawn by: Sebastian Frey	Sheet: 09_SHARED_PERIPHERAL.SchDoc Page 10 of 12
File: H:\Documents\SENSEI\Hardware\sensei-sensor-shield\Hardware\UT_baseBoard\Hardware\01_Mainboard\09_SHARED_PERIPHERAL.SchDoc			

40-pin board-to-board connector

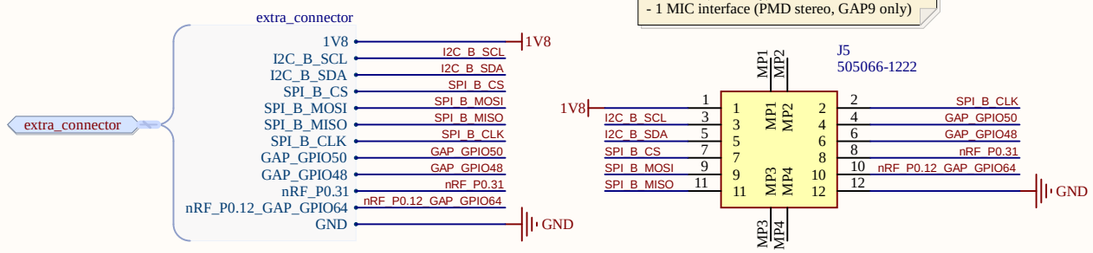


Extra connector

For future flexibility only.
All these GPIOs are also accessible on the other board-to-board connectors.

Extra board-to-board connector (mating height 0.6 mm).
Mate with 505070-1222

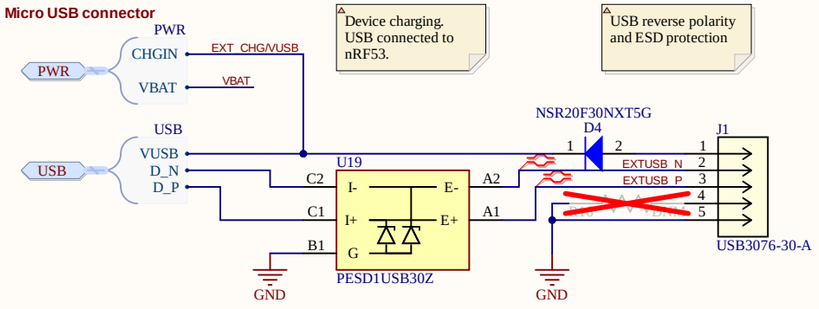
Gives access to:
- 1 I2C bus (shared nRF & GAP)
- 1 SPI bus (shared nRF & GAP)
- 1 GPIO (shared nRF & GAP)
- 1 GPIO (nRF only)
- 1 MIC interface (PMD stereo, GAP9 only)



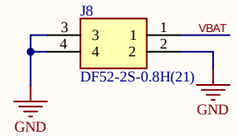
Micro USB connector

Device charging.
USB connected to nRF53.

USB reverse polarity and ESD protection



Battery connector



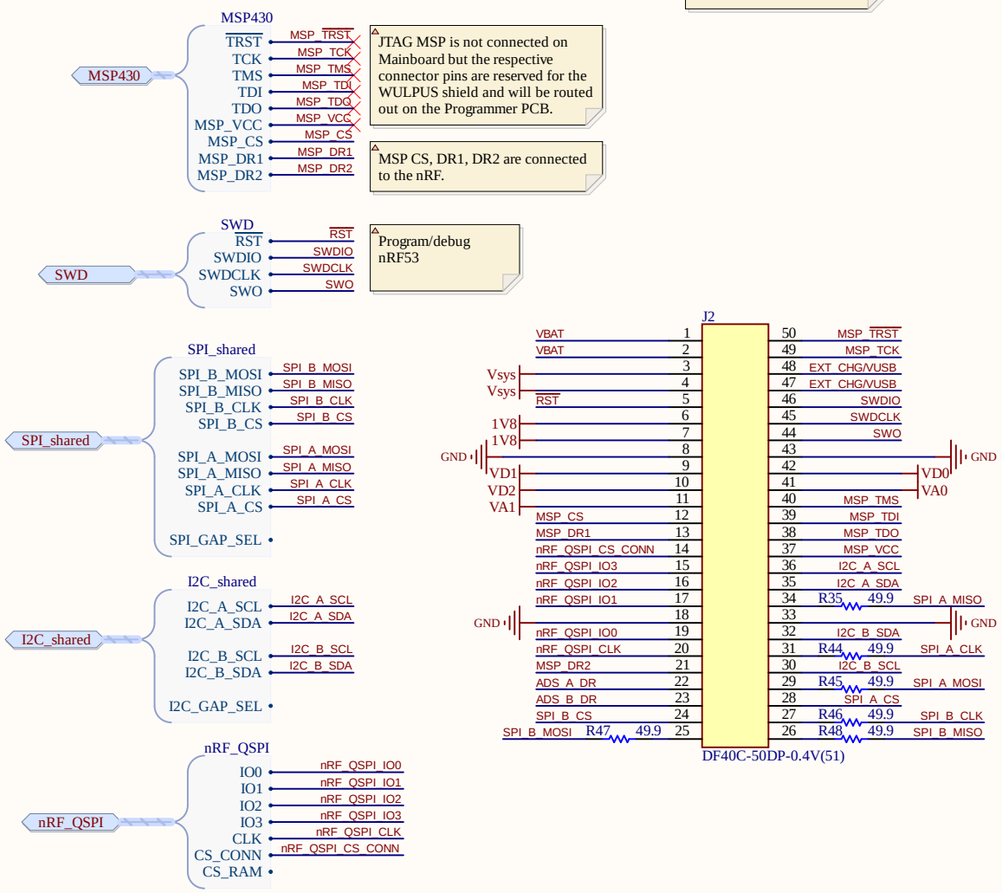
50-pin board-to-board connector

Pin-compatible to VitalCore

JTAG MSP is not connected on Mainboard but the respective connector pins are reserved for the WULPUS shield and will be routed out on the Programmer PCB.

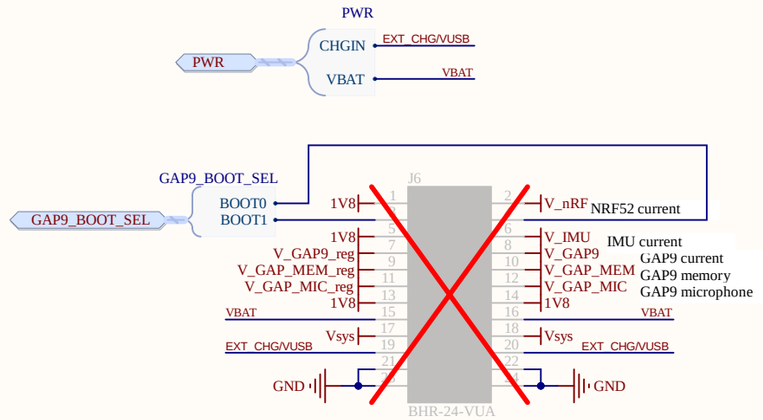
MSP CS, DR1, DR2 are connected to the nRF.

Program/debug nRF53

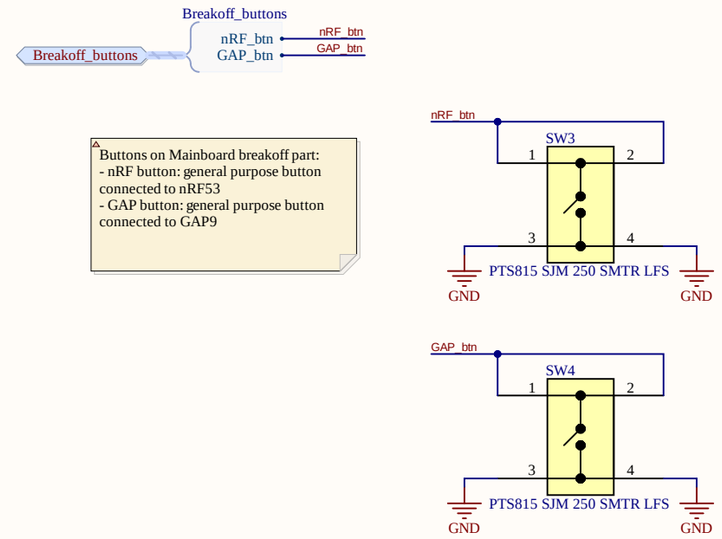


Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich				Project:	SENSEI Base Board - Connectors
Drawing number: 11	Rev: v1.0	Format:	Laboratory: Integrated Systems Laboratory		Sheet: 10_CONNECTOR.SchDoc
Date: 23.09.2024 16:16:23		A3	Drawn by: Sebastian Frey		Page 11 of 12
File: H:\Documents\SENSEI\Hardware\sensei-sensor-shield\Hardware\UT_baseBoard\Hardware\01_Mainboard\10_CONNECTOR.SchDoc					

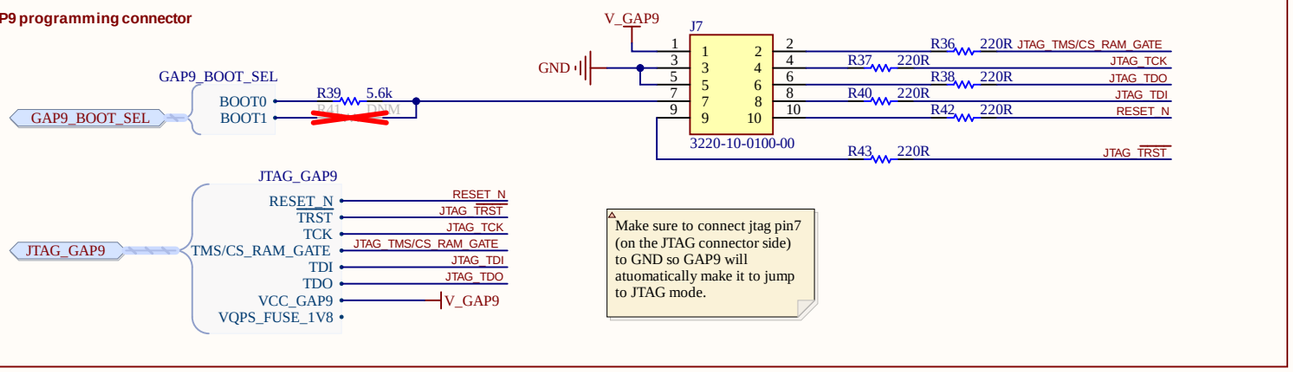
Power measurement pin headers



Buttons



GAP9 programming connector



Fiducial markers

Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich			Project: SENSEI Base Board - Breakoff		
Drawing number: 12	Rev: v1.0	Format: A3	Laboratory: Integrated Systems Laboratory	Sheet: 11_BREAK_OFF.SchDoc	
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