

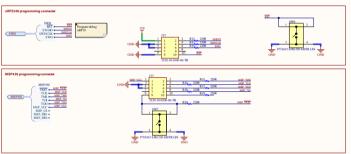


- 0b00=as per eFuse BOOTMODE / 0b01=JTAG / 0b10=HyperFlash / 0b11=eMRAM (for SPI Flash, must use BOOTMODE eFuse)
 They take precedence over eFuse bits BOOTMODE, unless:

- For sub int JTAG LOCK is set, in which case BOOT pins cannot force JTAG boot (but can still force boot from any other source)

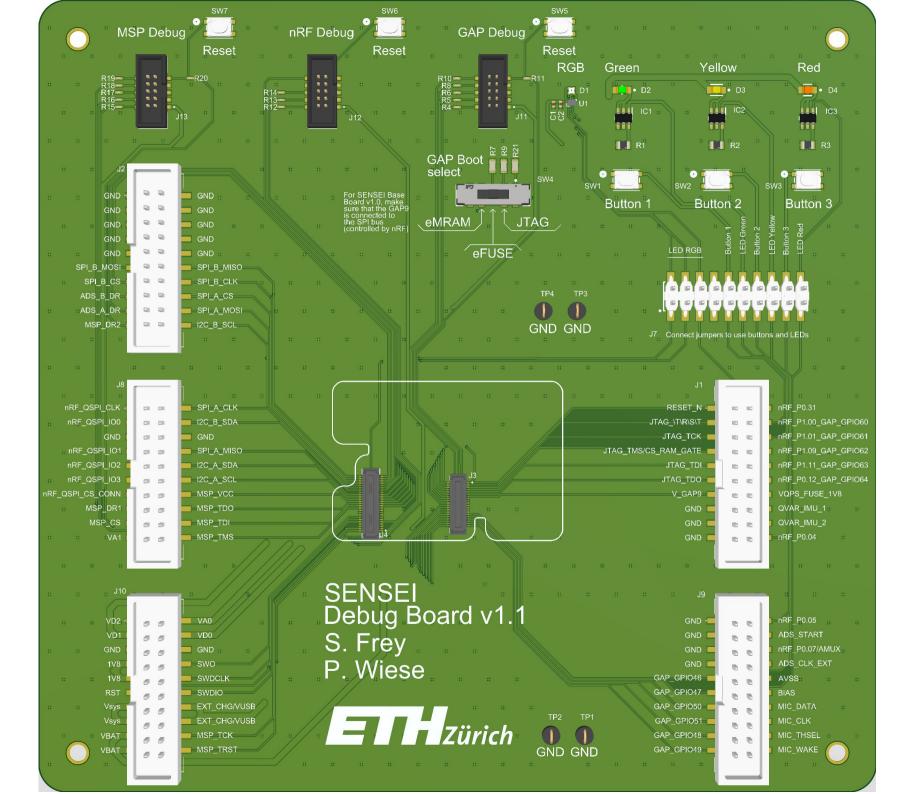
 or, eFuse bit JTAG LOCK is set, in which case BOOT pins cannot force JTAG boot (but can still force boot from any other source)

 or, eFuse bits BOOTMODE0_NOCHECK and/or BOOTMODE1_NOCHECK are set, in which case pins BOOT0 and/or BOOT1 are not examined by boot code and only eFuse BOOTMODE settings are taken into account





ETH		Drawing title							
Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	SENSEI Debug Board								
Drawing number: 1 Rev: vt1	Format	Laboratory: Integrated System Laboratory	Project:	OLgap.	interf	ace SchDoo			
Date: 26.09.2024 11:25:45	A2	Drawn by: Sebastian Frey	Page	1	of				
File H\Documents\SENSEI\Hardware\sensei-debug-pcb\Hardware\SENSEI_Debug-Board\OI_gap_interbuStrDoc									



Comment	Description	Designator	Quantity	Resistance	Capacitance	Tolerance
	Cap Ceramic 1uF 10V	<i>g</i>				
CL05A105KP5NNNC		C1	1		1uF	10%
	+85°C Paper T/R					
CL05A104KA5NNNC	Cap Ceramic 100nF					
		C2	1		0.1uF	10%
	0402 +85°C Paper T/R					
SML-LX0404SIUPGUSB	SML-LX0404SIUPGUSB RGB LED	D1	1			
LTST-C170GKT	LED GREEN CLEAR SMD	D2	1			
LTST-C170YKT	LED YELLOW CLEAR SMD	D3	1			
LTST-C170EKT		D4	1			
NCR421UX		IC1, IC2, IC3	3			
3020-20-0300-00	Connector	J1, J2, J8, J9, J10	5			
	40 Position 0.4mm	. , . , , . ,				
	Pitch Dual Row					
DE 10110 (0.0) 1050 0 111(51)	Vertical Surface					
DF40HC(3.0)-40DS-0.4V(51)	Mount (SMT) Pin	J3	l 1			
	Socket, 3.0mm					
	Stacking Height					
DF40HC(3.0)-50DS-0.4V(51)	50 Position 0.4mm					
	Pitch Dual Row					
	Vertical Surface					
	Mount (SMT) Pin	J4	1			
	Socket, 3.0mm					
	Stacking Height					
	0.025" SQ Post					
	Header, Surface					
TSM-110-01-T-DV	Mount, Vertical, -55					
	to 105 degC, 2.54 mm	J7	1			
	Pitch, 20-Pin, Male,					
	RoHS					
3220-10-0300-00-TR	Connector	J11, J12, J13	3			
	50 Position 0.4mm					
	Pitch Dual Row					
DF40C-40DP-0.4V(51)	Vertical Surface	J14	1			
(,,	Mount (SMT)					
	Receptacle					
	50 Position 0.4mm					
	Pitch Dual Row					
DF40C-50DP-0.4V(51)	Vertical Surface	J15	1			
	Mount (SMT)					
	Receptacle,					
RR1220Q-680-D	68Ω ±0.5% 0.1W					
	1/10W Chip Resistor	R1, R2, R3	,	68R		0.5%
	0805 (2012 Metric)	IN 1, INZ, INS]	OOK		0.070
	Thin Film					
CRCW0201220RFKED		R4, R5, R6, R8, R10,				
		R11, R12, R13, R14,	15			
		R15, R16, R17, R18,				
		R19, R20				
RK73B1JTTD562J		R7, R9, R21		5.6k		
PTS815 SJM 250 SMTR LFS		SW1, SW2, SW3, SW5,	6			
1 130 13 331VI 230 31VI II LI 3	Available	SW6, SW7	ļ			
JS203011JCQN	SWITCH SLIDE DP3T	SW4	1			
	300MA 6V		<u>'</u>			
TP THT		TP1, TP2, TP3, TP4	4			
	LED Driver with					
	Programmable					
IS31FL3194-CLS2-TR	Pattern Sequencing 3-	U1	1			
	Channel 40mA 8-Pin					
	WCSP T/R					