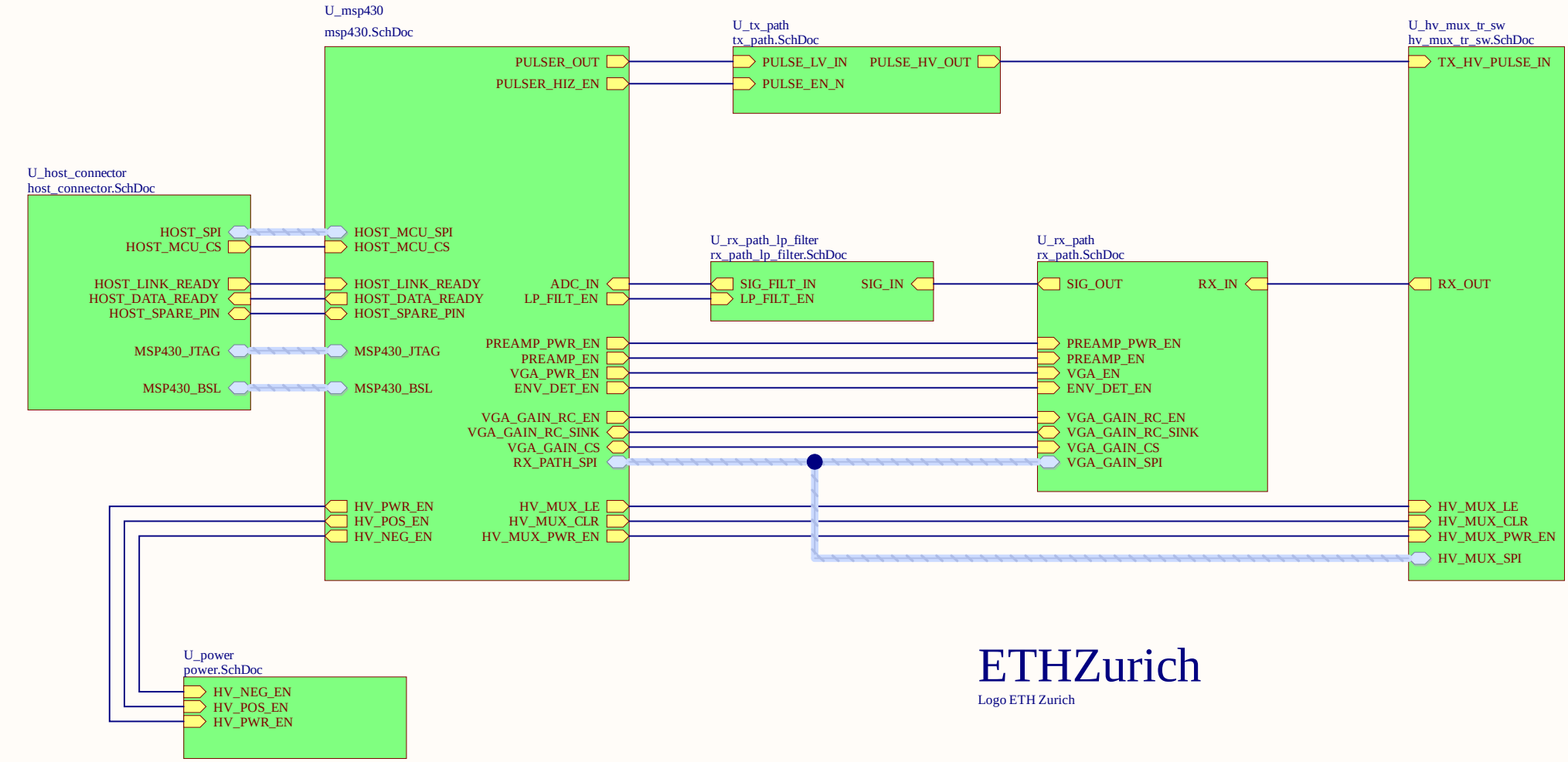


ETHZurich

Logo ETH Zurich

TP8 GND

TP9 GND

Mounting Hole M1

Mounting Hole M2

Mounting Hole M3

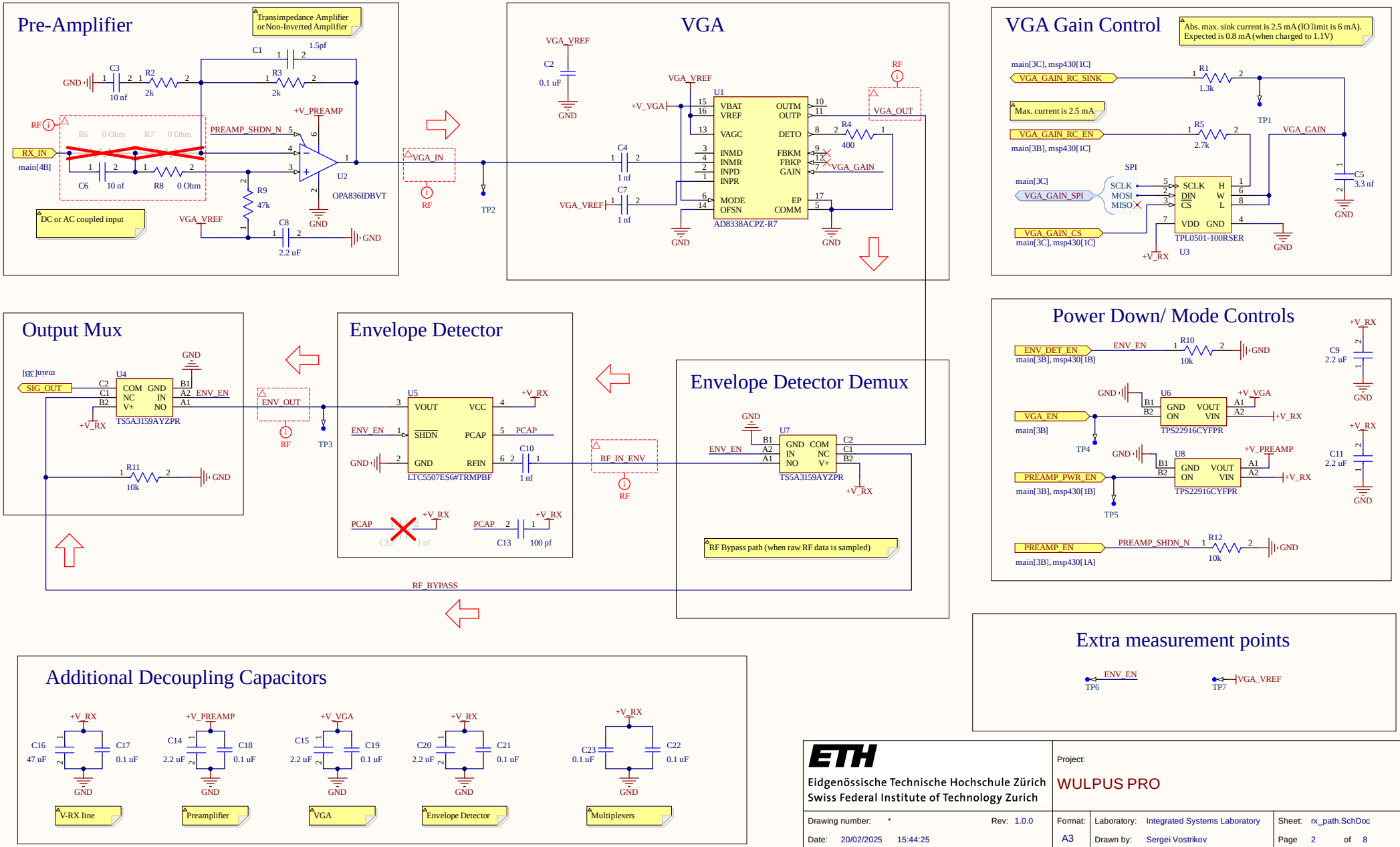
Mounting Hole M4

ETH

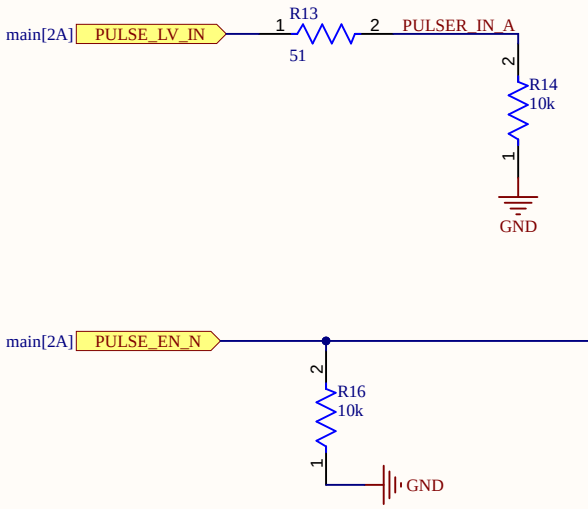
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: WULPUS PRO

Drawing number: *	Rev: 1.0.0	Format: A4 Q	Laboratory: Integrated Systems Laboratory	Sheet: main.SchDoc	
Date: 20/02/2025 15:44:25			Drawn by: Sergei Vostrikov	Page 1	of 8
File: C:\Users\serge\Documents\repos\wulpus_pro\hw\wulpus_pro_acq_pcb_dev_board\main.SchDoc					


Pre-Amplifier
Transimpedance Amplifier or Non-Inverted Amplifier
C1 1.5pf
C3 10 nf
R2 2k
R3 2k
GND
RF
RX_IN
main[4B]
R6 0 Ohm
R7 0 Ohm
C6 10 nf
R8 0 Ohm
PREAMP_SHDN_N
+V_PREAMP
U2
OPA836IDBVT
R9 47k
C8 2.2 uF
VGA_REF
DC or AC coupled input
VGA_IN
TP2
VGA
VGA_VREF
C2 0.1 uF
U1
+V_VGA
VGA_OUT
R4 400
C4 1 nf
C7 1 nf
VGA_GAIN
AD8338ACPZ-R7
VGA Gain Control
Abs. max. sink current is 2.5 mA (IO limit is 6 mA). Expected is 0.8 mA (when charged to 1.1V)
main[3C], msp430[1C]
VGA_GAIN_RC_SINK
R1 1.3k
Max. current is 2.5 mA
TP1
VGA_GAIN_RC_EN
main[3B], msp430[1C]
R5 2.7k
C5 3.3 nf
SPI
main[3C]
VGA_GAIN_SPI
SCLK
MOSI
MISO
VGA_GAIN_CS
main[3C], msp430[1C]
TPL0501-100RSER
U3
+V_RX
Output Mux
SIG_OUT
main[3B]
U4
TS5A3159AYZPR
ENV_EN
ENV_OUT
R11 10k
Envelope Detector
U5
LTC5507ES6#TRMPBF
PCAP
C10 1 nf
C12 1 nf
C13 100 pf
RF_IN_ENV
Envelope Detector Demux
U7
TS5A3159AYZPR
RF Bypass path (when raw RF data is sampled)
RF_BYPASS
Power Down/ Mode Controls
ENV_DET_EN
main[3B], msp430[1B]
R10 10k
C9 2.2 uF
VGA_EN
U6
TPS22916CYFPR
TP4
PREAMP_PWR_EN
U8
C11 2.2 uF
TP5
PREAMP_EN
main[3B], msp430[1A]
PREAMP_SHDN_N
R12 10k
Extra measurement points
TP6
TP7
Additional Decoupling Capacitors
C16 47 uF
C17 0.1 uF
C14 2.2 uF
C18 0.1 uF
C15 2.2 uF
C19 0.1 uF
C20 2.2 uF
C21 0.1 uF
C23 0.1 uF
C22 0.1 uF
V-RX line
Preamplifier
VGA
Envelope Detector
Multiplexers
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
Project:
WULPUS PRO
Drawing number: *
Rev: 1.0.0
Format: A3
Laboratory: Integrated Systems Laboratory
Sheet: rx_path.SchDoc
Date: 20/02/2025 15:44:25
Drawn by: Sergei Vostrikov
Page 2 of 8
File: C:\Users\serge\Documents\repos\wulpus_pro\hw\wulpus_pro_acq_pcb_dev_board\rx_path.SchDoc

Input Matching

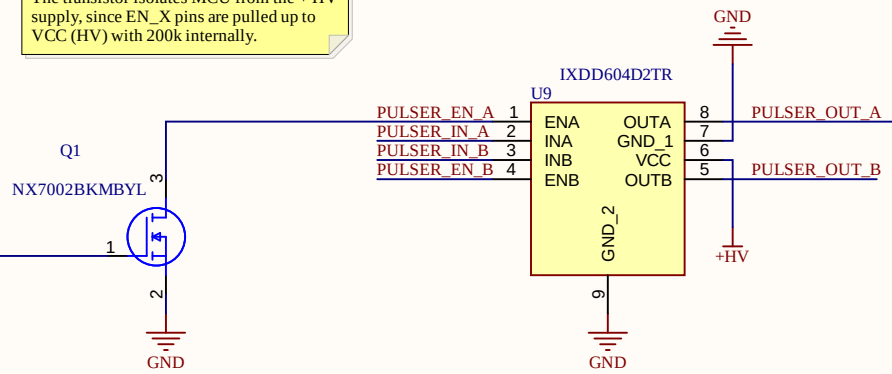


PULSE_EN_N drives EN pin through a transistor. It should be pulled to ground by default (enable state of the pulser)

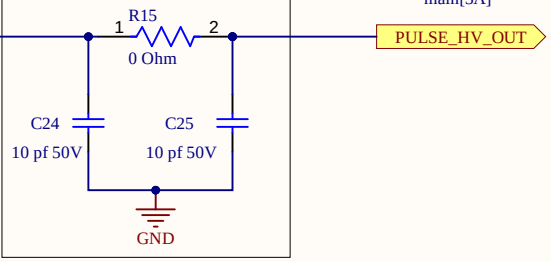
PULSE_IN delivers square pulses 0-3.3V with the maximum frequency up to 10 MHz. It should be driven low if the PULSE_IN output is in high-Z state.

The transistor isolates MCU from the + HV supply, since EN_X pins are pulled up to VCC (HV) with 200k internally.

Pulser IXDD604D2TR has a max source resistance of 2.5 Ohm with typical rise time of 9 ns and fall time of 8 ns. Maximum source current is 9 A. Power supply current <1 uA from VCC.



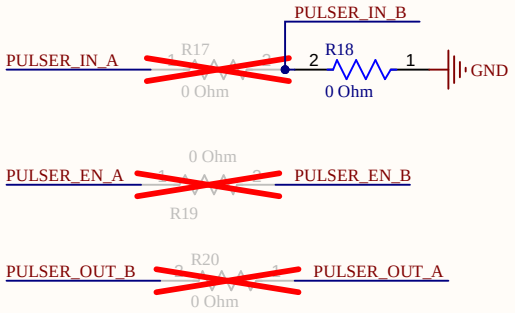
Optional Filter



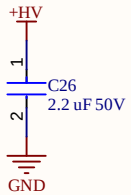
The second pulser channel (optional)

To connect the channel B, shorten pulser outputs PULSER_OUT_B and PULSER_OUT_A. Moreover, remove resistor that pulls PULSER_IN_B to ground and connect this line to PULSER_IN_A. Connect PULSER_EN_A to PULSER_EN_B

When using a single pulser channel A, disconnect all three signals (IN, EN and OUT) between channels A and B. Moreover, pull PULSER_IN_B to ground for the lowest power consumption.



Decoupling Capacitors

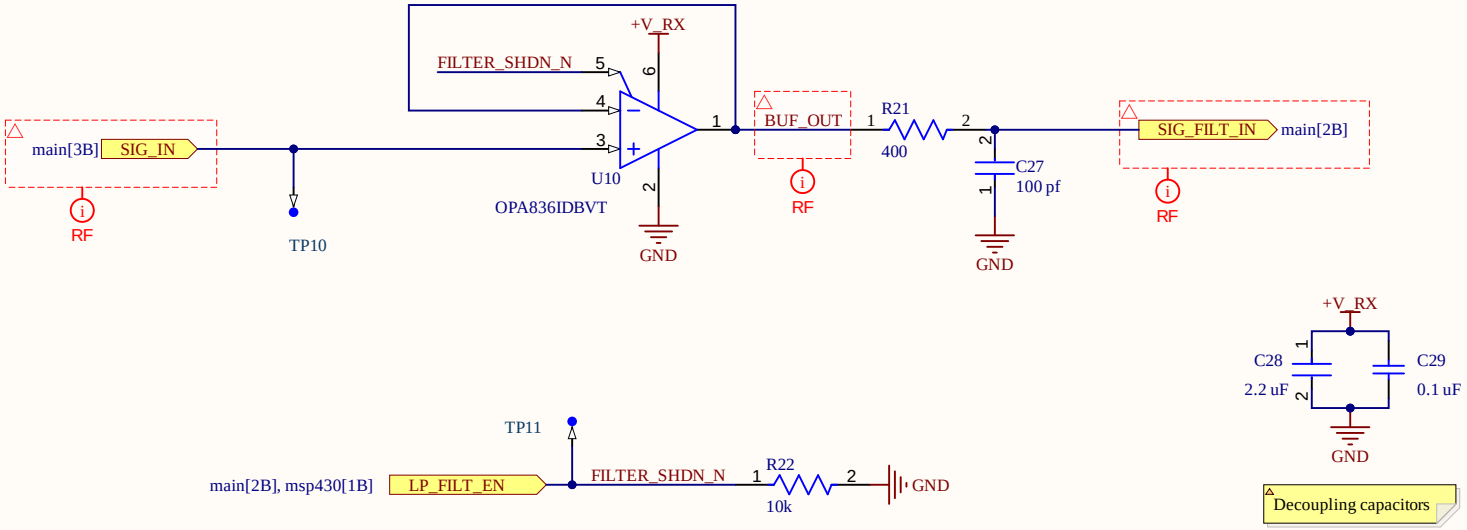


Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

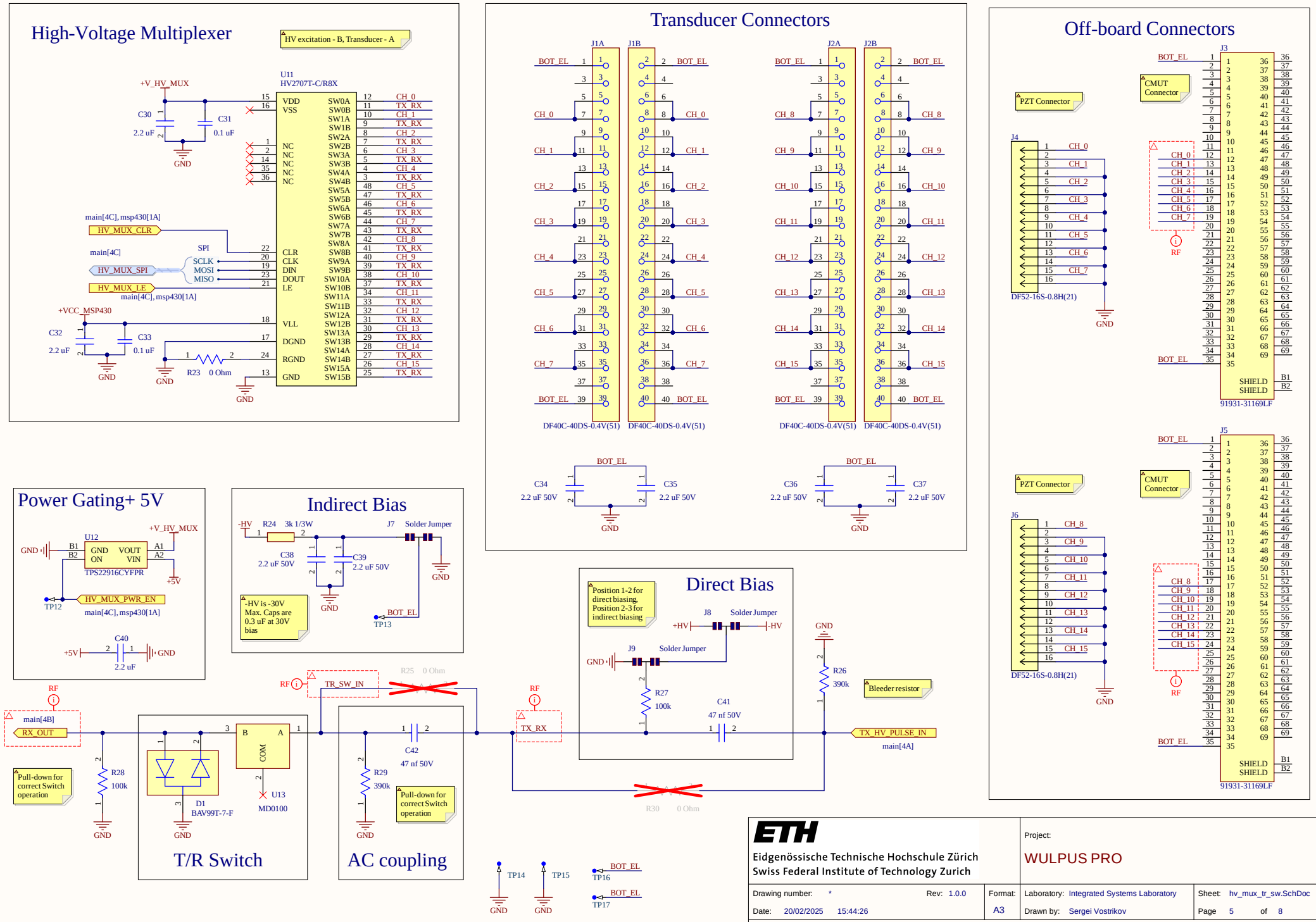
Project: WULPUS PRO

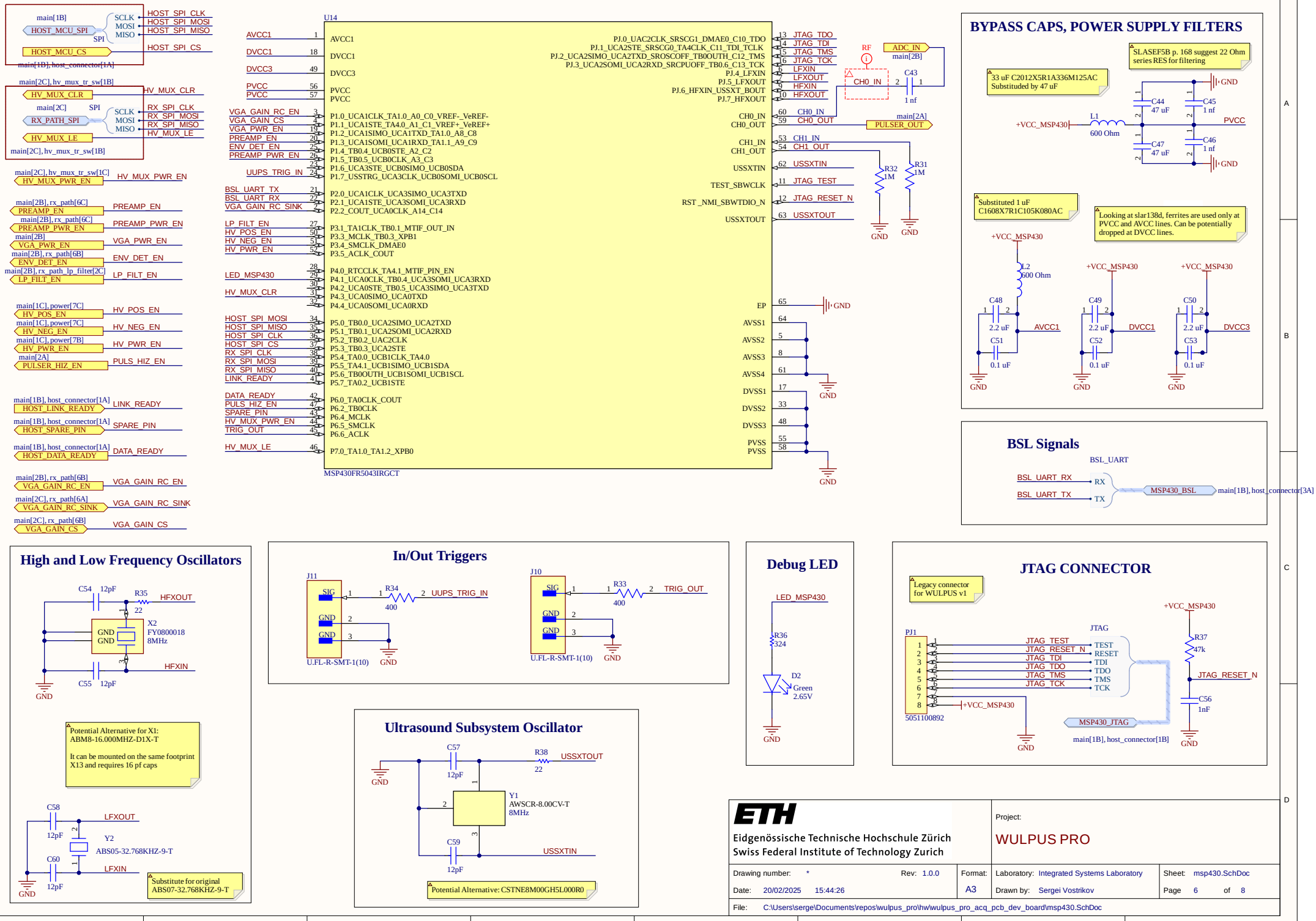
Drawing number: * Rev: 1.0.0	Format: A4 Q	Laboratory: Integrated Systems Laboratory	Sheet: tx_path.SchDoc
Date: 20/02/2025 15:44:25		Drawn by: Sergei Vostrikov	Page 3 of 8
File: C:\Users\serge\Documents\repos\wulpus_pro\hw\wulpus_pro_acq_pcb_dev_board\tx_path.SchDoc			

Output Buffer + Low Pass Filter (4 MHz cutoff)



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: WULPUS PRO		
Drawing number: * Rev: 1.0.0	Format: A4 Q	Laboratory: Integrated Systems Laboratory	Sheet: rx_path_lp_filter.SchDoc
Date: 20/02/2025 15:44:26		Drawn by: Sergei Vostrikov	Page 4 of 8
File: C:\Users\serge\Documents\repos\wulpus_pro\hw\wulpus_pro_acq_pcb_dev_board\rx_path_lp_filter.SchDoc			


High-Voltage Multiplexer
HV excitation - B, Transducer - A
U11
HV2707T-C/R8X
+V_HV_MUX
C30
2.2 uF
C31
0.1 uF
GND
main[4C], msp430[1A]
HV_MUX_CLR
main[4C]
SPI
SCLK
MOSI
MISO
HV_MUX_SPI
HV_MUX_LE
main[4C], msp430[1A]
+VCC_MSP430
C32
2.2 uF
C33
0.1 uF
R23
0 Ohm
Transducer Connectors
J1A
J1B
J2A
J2B
DF40C-40DS-0.4V(51)
C34
2.2 uF 50V
C35
2.2 uF 50V
C36
2.2 uF 50V
C37
2.2 uF 50V
Off-board Connectors
J3
J4
J5
J6
PZT Connector
CMUT Connector
DF52-16S-0.8H(21)
91931-31169LF
RF
Power Gating+ 5V
U12
TPS22916CYFPR
HV_MUX_PWR_EN
TP12
C40
2.2 uF
+5V
Indirect Bias
R24
3k 1/3W
J7
Solder Jumper
C38
2.2 uF 50V
C39
2.2 uF 50V
-HV is -30V
Max. Caps are
0.3 uF at 30V
bias
TP13
Direct Bias
Position 1-2 for
direct biasing,
Position 2-3 for
indirect biasing
J8
J9
R27
100k
C41
47 nf 50V
R26
390k
Bleeder resistor
TX_HV_PULSE_IN
main[4A]
TR_SW_IN
R25
0 Ohm
R30
0 Ohm
main[4B]
RX_OUT
TX_RX
R28
100k
Pull-down for
correct Switch
operation
D1
BAV99T-7-F
U13
MD0100
T/R Switch
C42
47 nf 50V
R29
390k
AC coupling
TP14
TP15
TP16
TP17
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
Project:
WULPUS PRO
Drawing number: *
Rev: 1.0.0
Format: A3
Laboratory: Integrated Systems Laboratory
Sheet: hv_mux_tr_sw.SchDoc
Date: 20/02/2025 15:44:26
Drawn by: Sergei Vostrikov
Page 5 of 8
File: C:\Users\serge\Documents\repos\wulpus_pro\hw\wulpus_pro_acq_pcb_dev_board\hv_mux_tr_sw.SchDoc


main[1B]
HOST_MCU_SPI
SCLK
MOSI
MISO
SPI
HOST_MCU_CS
HOST_SPI_CLK
HOST_SPI_MOSI
HOST_SPI_MISO
HOST_SPI_CS
main[1B], host_connector[1A]
main[2C], hv_mux_tr_sw[1B]
HV_MUX_CLR
main[2C]
RX_PATH_SPI
HV_MUX_LE
RX_SPI_CLK
RX_SPI_MOSI
RX_SPI_MISO
HV_MUX_LE
main[2C], hv_mux_tr_sw[1C]
HV_MUX_PWR_EN
main[2B], rx_path[6C]
PREAMP_EN
PREAMP_PWR_EN
main[2B]
VGA_PWR_EN
main[2B], rx_path[6B]
ENV_DET_EN
main[2B], rx_path_lp_filter[2C]
LP_FILT_EN
main[1C], power[7C]
HV_POS_EN
HV_NEG_EN
main[1C], power[7B]
HV_PWR_EN
main[2A]
PULSER_HIZ_EN
PULS_HIZ_EN
main[1B], host_connector[1A]
HOST_LINK_READY
LINK_READY
HOST_SPARE_PIN
SPARE_PIN
HOST_DATA_READY
DATA_READY
main[2B], rx_path[6B]
VGA_GAIN_RC_EN
main[2C], rx_path[6A]
VGA_GAIN_RC_SINK
main[2C], rx_path[6B]
VGA_GAIN_CS
U14
AVCC1
DVCC1
DVCC3
PVCC
VGA_GAIN_RC_EN
VGA_GAIN_CS
VGA_PWR_EN
PREAMP_EN
ENV_DET_EN
PREAMP_PWR_EN
UUPS_TRIG_IN
BSL_UART_TX
BSL_UART_RX
VGA_GAIN_RC_SINK
LP_FILT_EN
HV_POS_EN
HV_NEG_EN
HV_PWR_EN
LED_MSP430
HV_MUX_CLR
HOST_SPI_MOSI
HOST_SPI_MISO
HOST_SPI_CLK
HOST_SPI_CS
RX_SPI_CLK
RX_SPI_MOSI
RX_SPI_MISO
LINK_READY
DATA_READY
PULS_HIZ_EN
HV_MUX_PWR_EN
SPARE_PIN
TRIG_OUT
HV_MUX_LE
P1.0_UCA1CLK_TA1.0_A0_C0_VREF-_VeREF-
P1.1_UCA1STE_TA4.0_A1_C1_VREF+_VeREF+
P1.2_UCA1SIMO_UCA1TXD_TA1.0_A8_C8
P1.3_UCA1SOMI_UCA1RXD_TA1.1_A9_C9
P1.4_TB0.4_UCB0STE_A2_C2
P1.5_TB0.5_UCB0CLK_A3_C3
P1.6_UCA3STE_UCB0SIMO_UCB0SDA
P1.7_USSTRG_UCA3CLK_UCB0SOMI_UCB0SCL
P2.0_UCA1CLK_UCA3SIMO_UCA3TXD
P2.1_UCA1STE_UCA3SOMI_UCA3RXD
P2.2_COUT_UCA0CLK_A14_C14
P3.1_TA1CLK_TB0.1_MTIF_OUT_IN
P3.3_MCLK_TB0.3_XPB1
P3.4_SMCLK_DMAE0
P3.5_ACLK_COUT
P4.0_RTCCLK_TA4.1_MTIF_PIN_EN
P4.1_UCA0CLK_TB0.4_UCA3SOMI_UCA3RXD
P4.2_UCA0STE_TB0.5_UCA3SIMO_UCA3TXD
P4.3_UCA0SIMO_UCA0TXD
P4.4_UCA0SOMI_UCA0RXD
P5.0_TB0.0_UCA2SIMO_UCA2TXD
P5.1_TB0.1_UCA2SOMI_UCA2RXD
P5.2_TB0.2_UAC2CLK
P5.3_TB0.3_UCA2STE
P5.4_TA0.0_UCB1CLK_TA4.0
P5.5_TA4.1_UCB1SIMO_UCB1SDA
P5.6_TB0OUTH_UCB1SOMI_UCB1SCL
P5.7_TA0.2_UCB1STE
P6.0_TA0CLK_COUT
P6.2_TB0CLK
P6.4_MCLK
P6.5_SMCLK
P6.6_ACLK
P7.0_TA1.0_TA1.2_XPB0
MSP430FR5043IRGCT
PJ.0_UAC2CLK_SRSCG1_DMAE0_C10_TDO
PJ.1_UCA2STE_SRSCG0_TA4CLK_C11_TDI_TCLK
PJ.2_UCA2SIMO_UCA2TXD_SROSCOFF_TB0OUTH_C12_TMS
PJ.3_UCA2SOMI_UCA2RXD_SRCPUOFF_TB0.6_C13_TCK
PJ.4_LFXIN
PJ.5_LFXOUT
PJ.6_HFXIN_USSXT_BOUT
PJ.7_HFXOUT
CH0_IN
CH0_OUT
CH1_IN
CH1_OUT
USSXTIN
TEST_SBWCLK
RST _NMI_SBWTDIO_N
USSXTOUT
JTAG_TDO
JTAG_TDI
JTAG_TMS
JTAG_TCK
LFXIN
LFXOUT
HFXIN
HFXOUT
CH1_IN
CH1_OUT
USSXTIN
JTAG_TEST
JTAG_RESET_N
USSXTOUT
EP
AVSS1
AVSS2
AVSS3
AVSS4
DVSS1
DVSS2
DVSS3
PVSS
PVSS
GND
RF
ADC_IN
main[2B]
CH0_IN
C43
1 nf
CH0_IN
CH0_OUT
main[2A]
PULSER_OUT
R32
1M
R31
1M
BYPASS CAPS, POWER SUPPLY FILTERS
SLASEF5B p. 168 suggest 22 Ohm series RES for filtering
33 uF C2012X5R1A336M125AC
Substituted by 47 uF
+VCC_MSP430
L1
600 Ohm
C44
47 uF
C45
1 nf
C47
47 uF
C46
1 nf
PVCC
GND
Substituted 1 uF
C1608X7R1C105K080AC
Looking at slar138d, ferrites are used only at PVCC and AVCC lines. Can be potentially dropped at DVCC lines.
L2
600 Ohm
C48
2.2 uF
C51
0.1 uF
AVCC1
C49
2.2 uF
C52
0.1 uF
DVCC1
C50
2.2 uF
C53
0.1 uF
DVCC3
BSL Signals
BSL_UART
BSL_UART_RX
BSL_UART_TX
RX
TX
MSP430_BSL
main[1B], host_connector[3A]
High and Low Frequency Oscillators
C54
12pF
R35
22
HFXOUT
X2
FY0800018
8MHz
HFXIN
C55
12pF
Potential Alternative for X1:
ABM8-16.000MHZ-D1X-T
It can be mounted on the same footprint X13 and requires 16 pf caps
C58
12pF
LFXOUT
Y2
ABS05-32.768KHZ-9-T
C60
12pF
LFXIN
Substitute for original ABS07-32.768KHZ-9-T
In/Out Triggers
J11
SIG
GND
R34
400
UUPS_TRIG_IN
U.FL-R-SMT-1(10)
J10
R33
400
TRIG_OUT
Debug LED
LED_MSP430
R36
324
D2
Green
2.65V
JTAG CONNECTOR
Legacy connector for WULPUS v1
PJ1
5051100892
JTAG_TEST
JTAG_RESET_N
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
JTAG
TEST
RESET
TDI
TDO
TMS
TCK
R37
47k
C56
1nF
MSP430_JTAG
main[1B], host_connector[1B]
Ultrasound Subsystem Oscillator
C57
12pF
R38
22
USSXTOUT
Y1
AWSCR-8.00CV-T
8MHz
C59
12pF
USSXTIN
Potential Alternative: CSTNE8M00GH5L000R0
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
Project:
WULPUS PRO
Drawing number: *
Rev: 1.0.0
Format: A3
Laboratory: Integrated Systems Laboratory
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Date: 20/02/2025 15:44:26
Drawn by: Sergei Vostrikov
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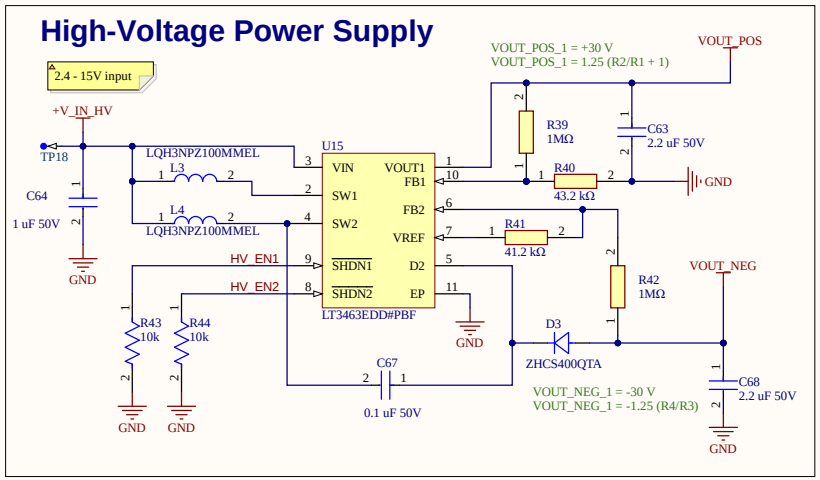
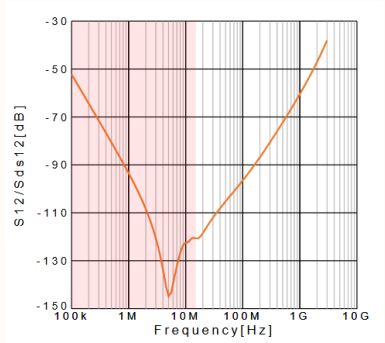
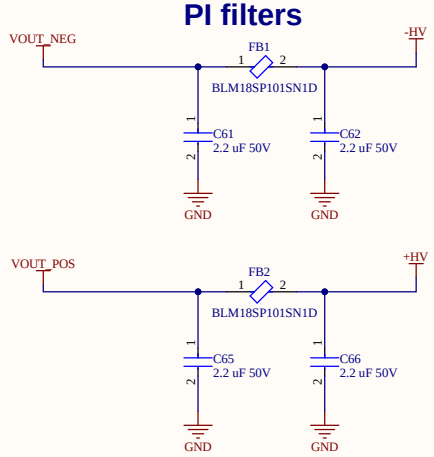
File: C:\Users\serge\Documents\repos\wulpus_pro\hw\wulpus_pro_acq_pcb_dev_board\msp430.SchDoc

High-Voltage Power Supply

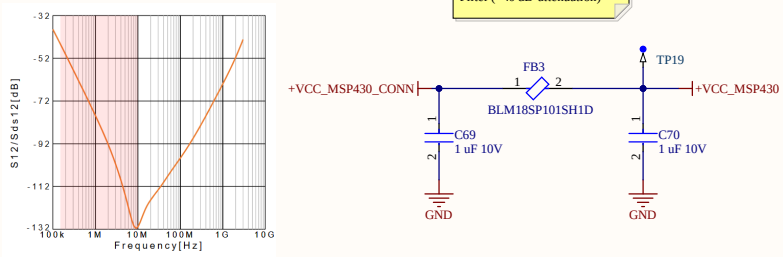


PI filters

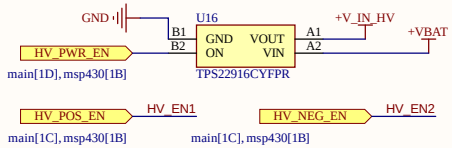




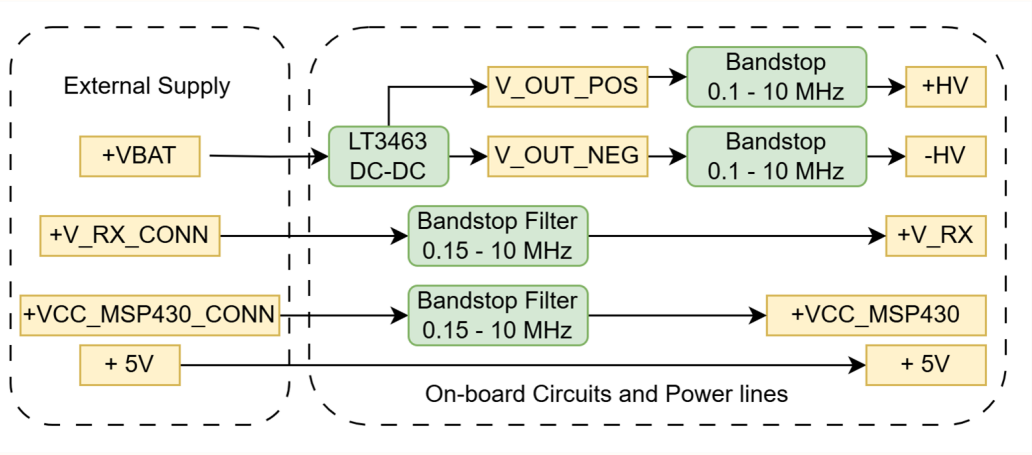
Input Filter for MCU voltage



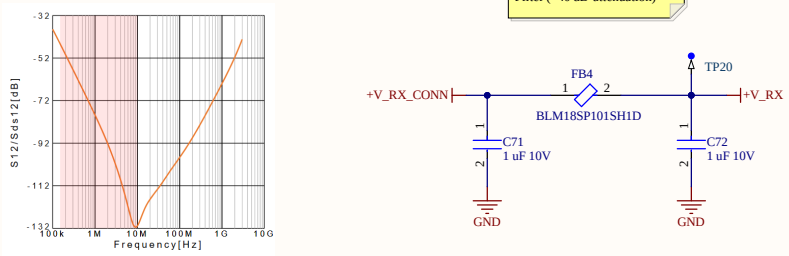
Power Switch



Power Tree (No Load Switches)



Input Filter for RX path



Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: WULPUS PRO

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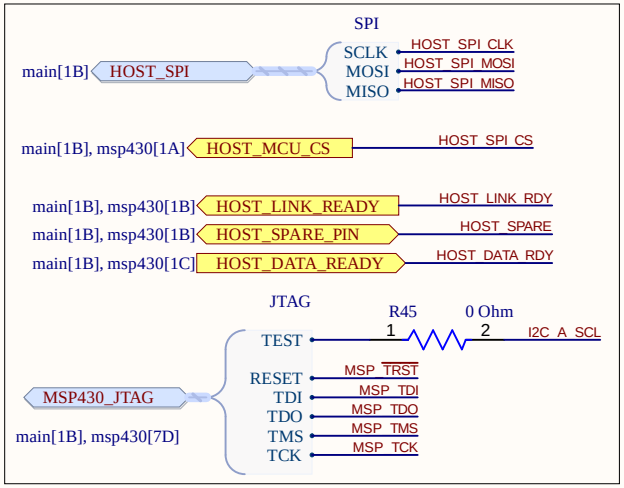

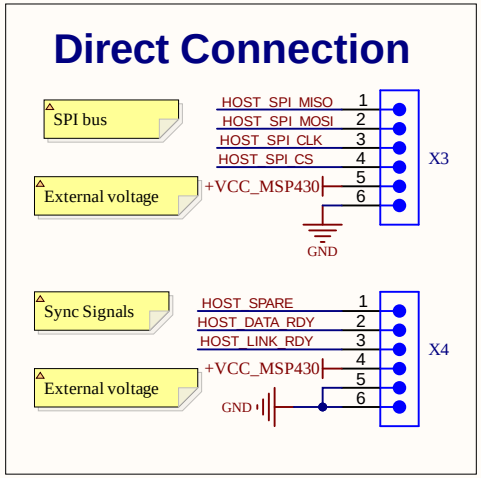

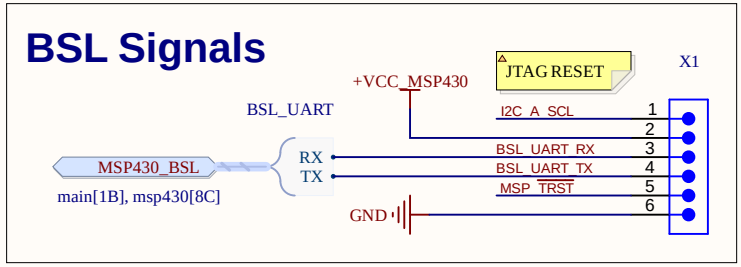

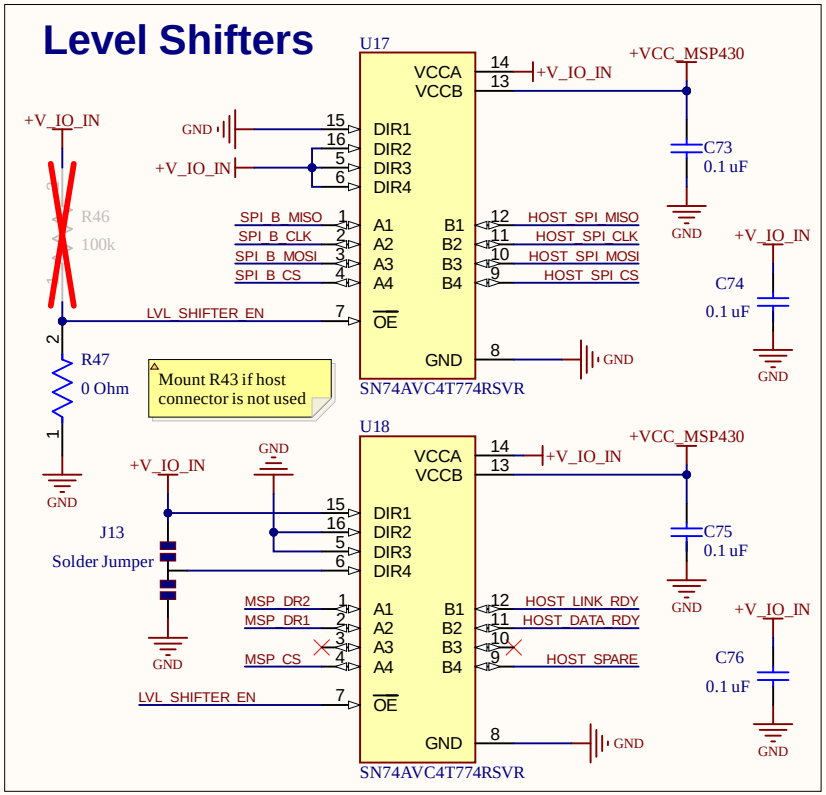

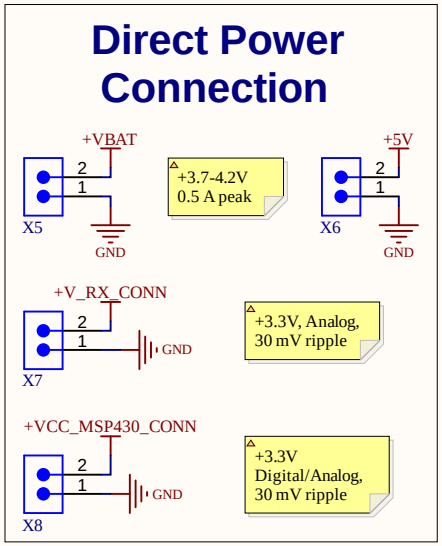

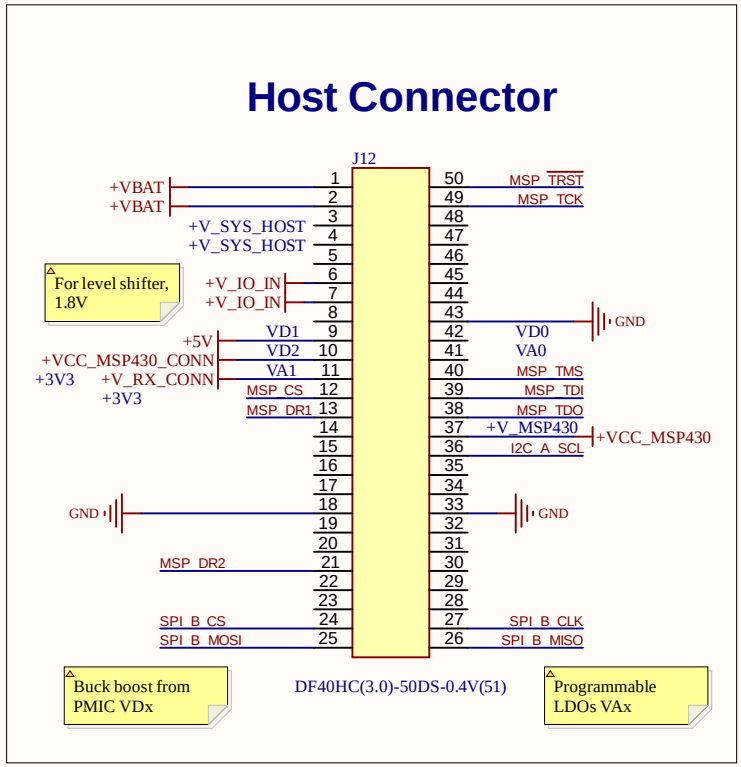

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