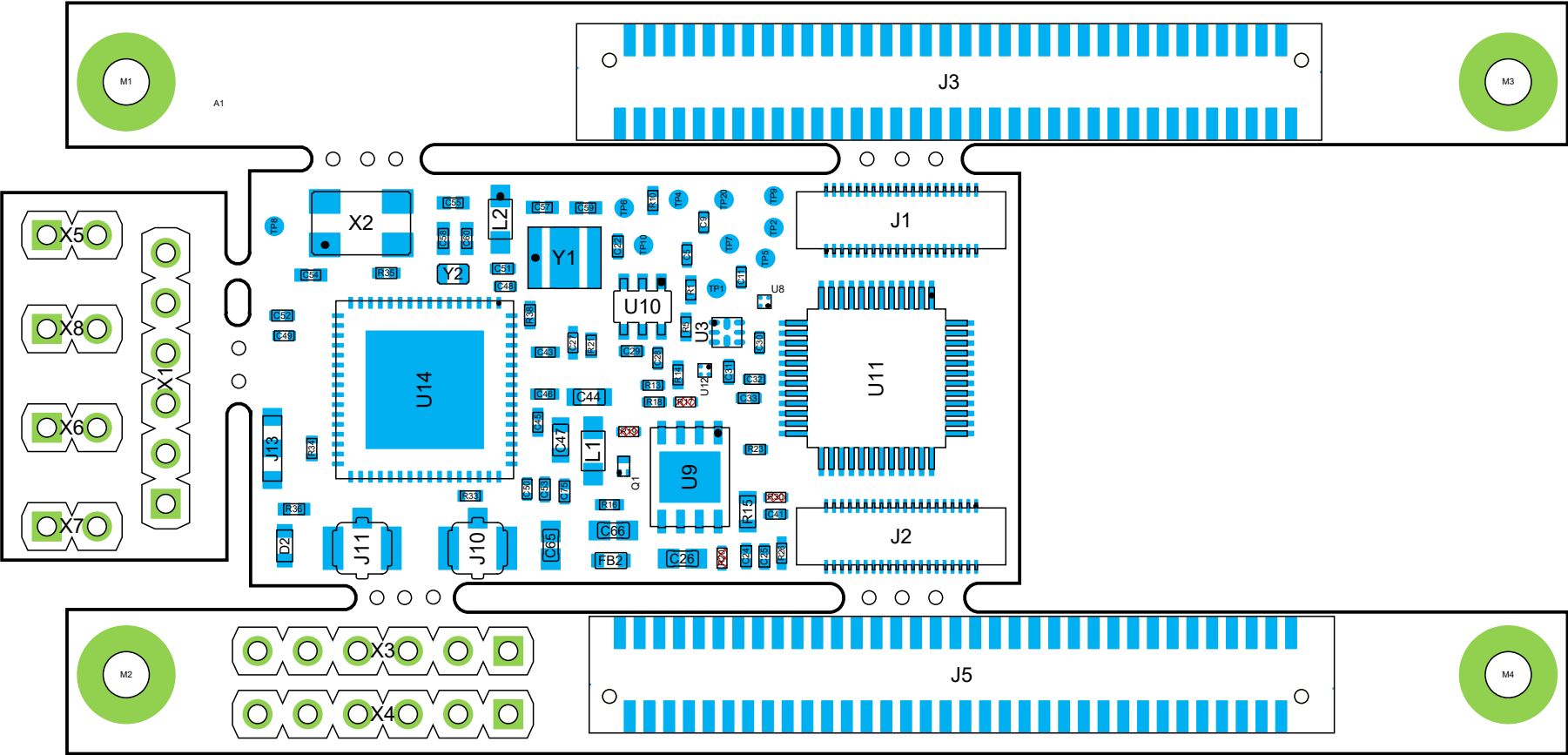


View from Top side (Scale 3:1)



Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project:

WULPUS PRO Assembly Drawing

Drawing number: *

Rev: v1.0.0

Format: Laboratory: IIS

Sheet: wulpus_pro_acq.PCBDwf

Date: 20/02/2025 15:49

Drawn by: Sergei Vostrikov

Page: 1 of 1

File: C:\Users\serge\Documents\repos\wulpus_pro\hw\wulpus_pro_acq_pcb_dev_board\wulpus_pro_acq.PCBDwf

A



C

D

A

B

C

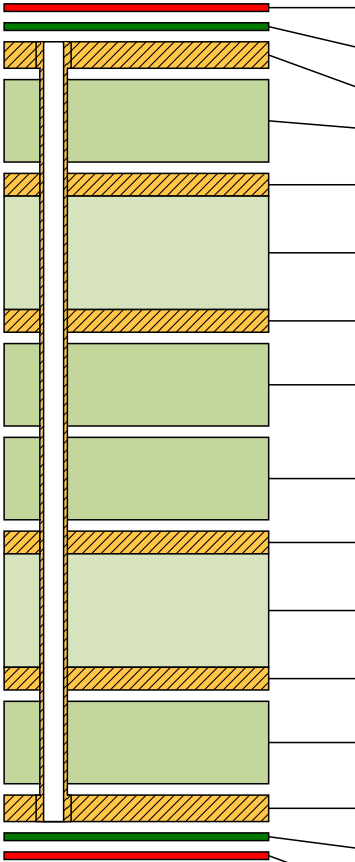

D

1


2

3

4

1		2		3		4		
Layer Stack Legend								
A		Material	Layer	Thickness	Dielectric Material	Type	Gerber	
			Top Overlay				Legend	GTO
		Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask	GTS	
		Copper	Top Layer	0.04mm		Signal	GTL	
		Prepreg		0.11mm	PP-2116	Dielectric		
		CF-004	Layer 2	0.03mm		Signal	G1	
		Core		0.15mm	Core-009	Dielectric		
		CF-004	Layer 3	0.03mm		Signal	G2	
		Prepreg		0.11mm	PP-2116	Dielectric		
		Prepreg		0.11mm	PP-2116	Dielectric		
B		CF-004	Layer 4	0.03mm		Signal	G3	
	Core		0.15mm	Core-009	Dielectric			
	CF-004	Layer 5	0.03mm		Signal	G4		
	Prepreg		0.11mm	PP-2116	Dielectric			
	Copper	Bottom Layer	0.04mm		Signal	GBL		
	Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask	GBS		
		Bottom Overlay			Legend	GBO		
	Total thickness: 0.95mm							
	C							
D	JLCPCB stack up: JLC061011-2116A							
					Project:			
	Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich				WULPUS PRO Assembly Drawing			
	Drawing number: *		Rev: v1.0.0		Format:	Laboratory: IIS	Sheet: wulpus_pro_acq.PCBDw	
	Date: 20/02/2025 15:49		A4 Q		Drawn by: Sergei Vostrikov		Page =sheetofsheettotal	
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JLCPCB stack up: JLC061011-2116A

 Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: WULPUS PRO Assembly Drawing			
Drawing number: *	Rev: v1.0.0	Format: A4 Q	Laboratory: IIS	Sheet: wulpus_pro_acq.PCBDwf
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