

Bitcraze Workshop: PULP Introduction

Lorenzo Lamberti, Hanna Müller, Vlad Niculescu, Manuele Rusci, Daniele Palossi



















Team

Lorenzo





Hanna



ETH zürich

Vlad



ETH zürich

Manuele







Daniele







- Lorenzo Lamberti
- Hanna Müller
- Vlad Niculescu
- Dr. Manuele Rusci
- Dr. Daniele Palossi

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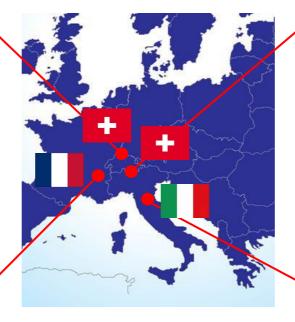
D. Palossi 16.04.2021

Team affiliations

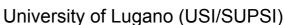
THzürich



Polytechnic of Zürich (ETHZ)











Greenwaves Tech. in Grenoble (GWT)



University of Bologna (UniBO)





We are looking for outstanding Ph.D. candidates: https://www.supsi.ch/home en/supsi/lavora-con-noi/2021-02-24-bando816.html





Agenda

	Topic	Time	Description	Speaker
Overview	PULP introduction	15'	Parallel Ultra-low Power (PULP) overview	Daniele
	GAP8 architecture	10'	System-on-Chip hardware architecture	Manuele
	Al-deck	15'	Printed circuit board overview & GAP8 SDK	Hanna
	Break	15'		
Hands-on	Basic programming	10'	JTAG programming & 'Hello World' example	Hanna
	Image manipulation	10'	Image acquisition, parallel image filter	Hanna
	Firmware integration	15'	App-layer integration, UART communication	Vlad
	Video streaming	20'	Basic Wi-Fi streaming, JPEG image compression	Lorenzo
	Conclusion	5'	Final remarks	Daniele





Parallel Ultra-low Power (PULP)

- The PULP project started in 2013
- Collaboration between the University of Bologna and ETH Zürich
 - Large team, about 60 people, not all are working on PULP
- Academic/Research goals:
 - Create a compute platform used for research (e.g., autonomous nano-drones) by the PULP and other groups in Europe and in the World
 - Push energy efficiency of IoT computing systems as much as possible (we target research on low-power MCUs)
 - Open-source approach
- We wanted to start with a clean slate, no need to remain compatible with legacy systems, no dependency with any commercial IP
- We started with **OpenRISC** and around mid-2016 we moved to **RISC-V** ISA:
 - Larger community, more momentum



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PULP ecosystem

RISC-V Cores

RI5CY Micro Zero Ariane riscy 32b 32b 64b

We have developed several optimized RISC-V cores







Only processing cores are not ETHZürich

PULP ecosystem

RISC-V Cores RI5CY Ariane Micro Zero riscy riscy 32b 32b 32b 64b

Peripherals		Interconnect	
JTAG	SPI	Logarithmic interconnect	
UART	I2S	APB – Peripheral Bus	
DMA	GPIO	AXI4 – Interconnect	

HWCE (convolution)

enough, we need more

HWCrypt (crypto)

PULPO (1st order opt)

Accelerators

Neurostream (ML)

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All these components are platforms combined into

PULP ecosystem

Peripherals RISC-V Cores JTAG SPI Ariane **RI5CY** Micro Zero riscy riscy 125 **UART** 32b 32b 32b 64b **DMA GPIO**

Interconnect Logarithmic interconnect APB - Peripheral Bus AXI4 – Interconnect

Platforms



Single Core

PULPino

PULPissimo

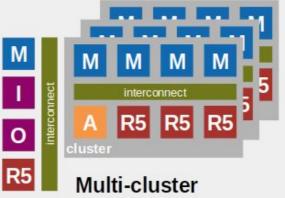






Multi-core

- **Fulmine**
- Mr. Wolf



Hero

IOT

Accelerators

HWCE (convolution) Neurostream (ML)

HWCrypt (crypto)

PULPO (1st order opt)



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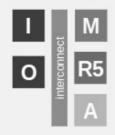
All these components are platforms ETHZürich combined into

PULP ecosystem

RISC-V Cores RI5CY Micro Zero Ariane riscy 32b 32b 32b 64b

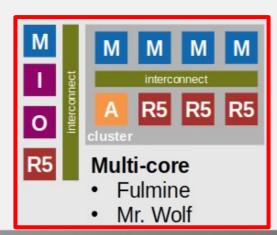
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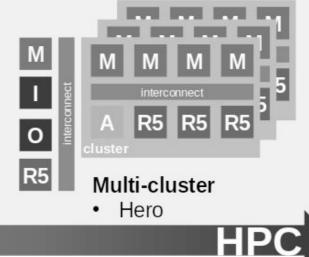
Platforms



Single Core

- PULPino
- PULPissimo





IOT

Accelerators

HWCE (convolution) Neurostream (ML)

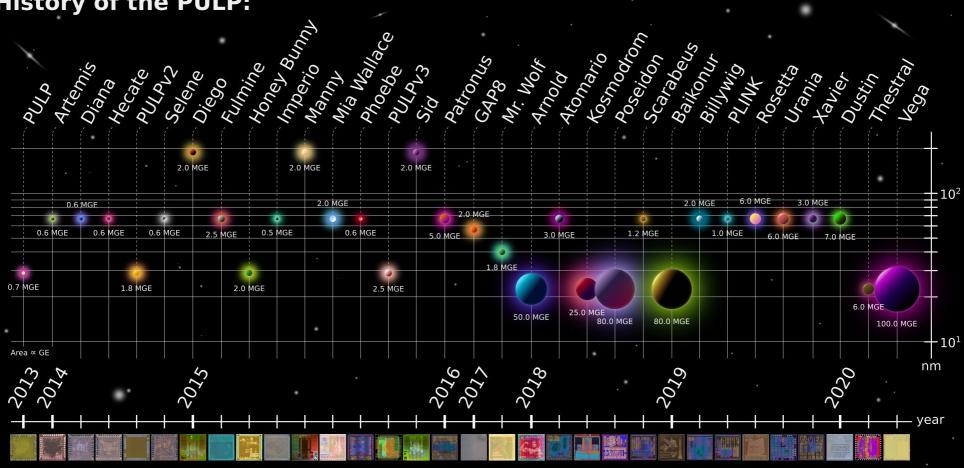
HWCrypt (crypto)

PULPO (1st order opt)



PULP Silicon Prototypes







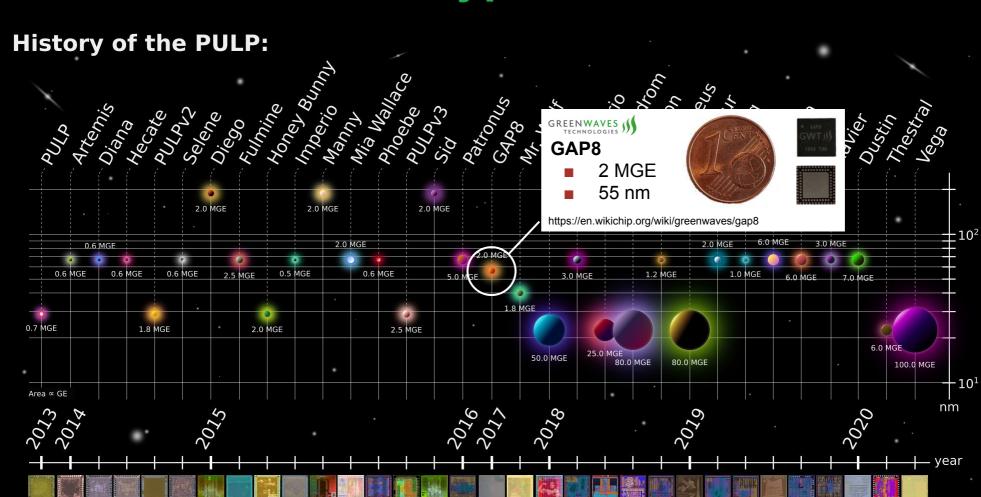
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http://asic.ethz.ch/applications/Pulp.html

Credit: Daniele Palossi

-THZürich

PULP Silicon Prototypes





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http://asic.ethz.ch/applications/Pulp.html

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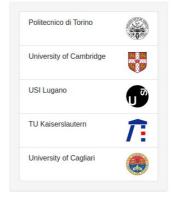


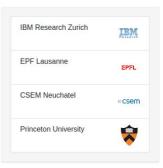
Who uses PULP?

Industrial users:



Direct research collaborators:







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users we are Academic aware of:

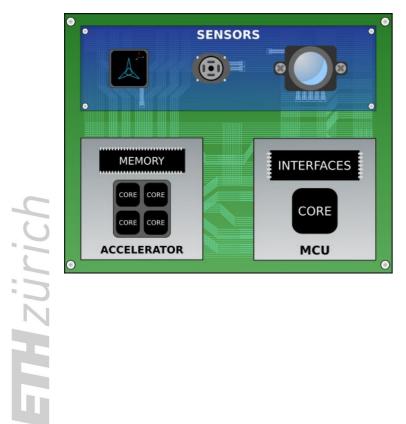
Università di Genova Stanford University M UC Los Angeles İstanbul Teknik Üniversitesi UC San Diego Columbia University \Rightarrow TU Darmstadt LIRMM Montpelie RWTH Aachen Universität Bremen University of Stuttgart Hongik University Seou UFRN Rio Grande do Norte IIT Kharagpur 働 TU Münich ТШП FORTH Hellas Chalmers Göteborg FAU Erlangen-Nürnberg 0 NTNU Trondheim Kyoto University Tecnologico de Costa Rica TEC IDSIA Manno SVNIT Surat





The PULP-Shield

ULP heterogeneous model [1]



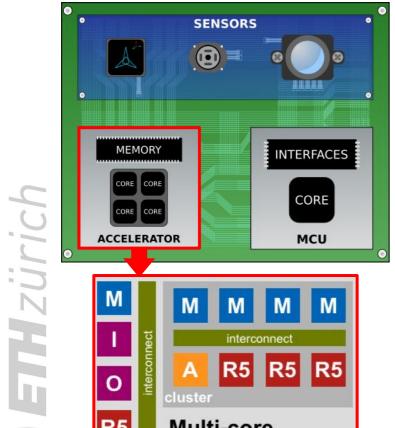


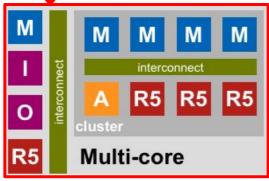




The PULP-Shield

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[1] F. Conti, D. Palossi, A. Marongiu, D. Rossi, and L. Benini. "Enabling the heterogeneous accelerator model on ultra-low power microcontroller platforms." IEEE DATE, 2016.



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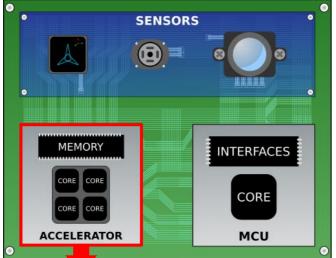


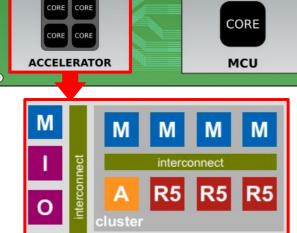
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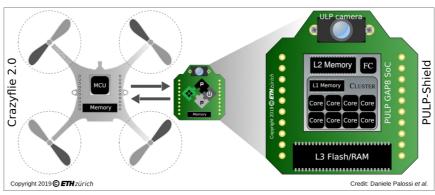


PULP-Shield [2]





Multi-core









- $\sim 5 g 30x28 mm$
- PULP GAP8 SoC
- Off-chip DRAM/Flash
- QVGA ULP Camera
- Open source hardware





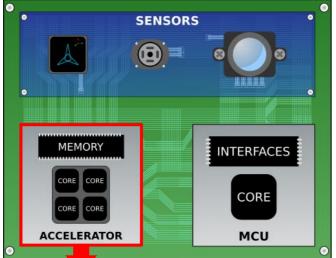
[1] F. Conti, D. Palossi, A. Marongiu, D. Rossi, and L. Benini. "Enabling the heterogeneous accelerator model on ultra-low power microcontroller platforms." IEEE DATE, 2016. [2] D. Palossi, F. Conti, and L. Benini "An open source and open hardware deep learning-powered visual navigation engine for autonomous nano-UAVs." IEEE DCOSS, 2019.

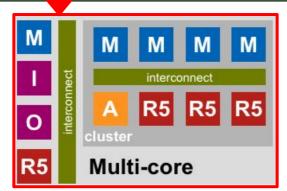




The PULP-Shield

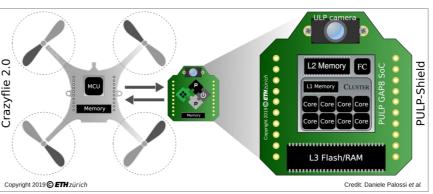
ULP heterogeneous model [1]







PULP-Shield [2]

















 $\sim 5 \text{ g} - 30 \text{x} 28 \text{ mm}$

PULP GAP8 SoC





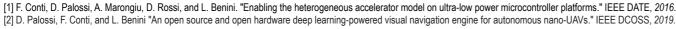




- $\sim 8 \text{ g} 40 \text{x} 28 \text{ mm}$
- PULP GAP8 SoC
- 8/64 MB DRAM/Flash
- QVGA ULP Camera
- WiFi module



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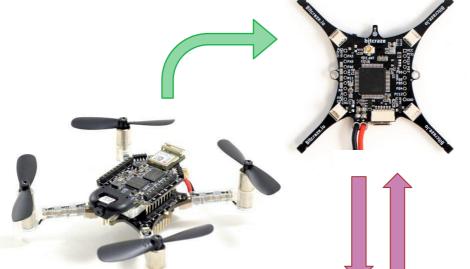


The Al-Deck

Crazyflie (STM32)

Al-Deck (GAP8)

Crazyflie + Al-Deck



Radio: Nordic BTLE



nRF51 2.4GHz

Data rate: 0,25/1/2 Mbit/s

UART Link

Data rate: 1 Mbit/s

Radio: NINA Wi-Fi

Wifi

NINA-W102 2.4 GHz Data rate: 6-54 Mbit/s

Radio dongle



Wi-Fi card

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The Al-Deck

Crazyflie (STM32)

Radio: **Nordic BTLE**



nRF51 2.4GHz

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UART Link

Radio: **NINA Wi-Fi**

Wi Fi

NINA-W102 2.4 GHz Data rate: 6-54 Mbit/s Radio dongle



Wi-Fi card

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Crazyflie + Al-Deck

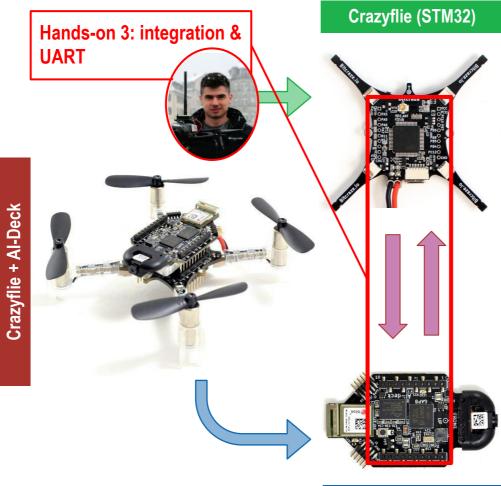
Hands-on 1-2: GAP8 programming & camera

Al-Deck (GAP8)

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The Al-Deck



Al-Deck (GAP8)

Radio: Nordic BTLE



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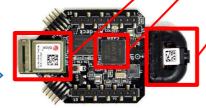
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Wi Fi



Wi-Fi card

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Crazyflie + Al-Deck

Radio dongle

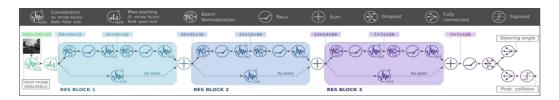
Hands-on 4: Wi-Fi image streaming

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Al-based applications (not in this workshop)

PULP-Dronet:



Task:	Lane detection / Obstacle avoidance	
CNN:	41 MMAC/frame	
Onboard:	6fps@45mW / 18fps@272mW	
Device:	PULP-Shield (GAP8)	
arXiv.org	https://arxiv.org/abs/1805.01831	







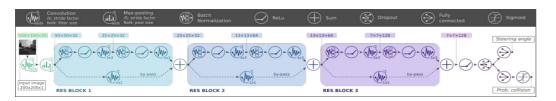
https://www.youtube.com/watc h?v=JKY03NV3C2s





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PULP-Dronet v2 for the Al-Deck coming soon on GitHub

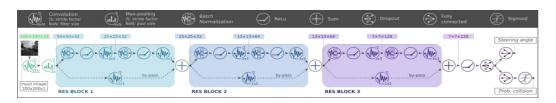






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PULP-Frontnet:

① PULP-Frontnet 160×32 ② PULP-Frontnet 160×16 ③ PULP-Frontnet 80×32	/S Convolution /S: stride factor N×N N×N: filter size	/S Max-pooling /S: stride factor N×N N×N: pool size	Batch Normalization	ReLu Dropot	ut Fully Connected Linear
② 160×96×1 ② 80×48×16	① 40×24×32 ② 40×24×16 ③ 20×12×32 ② 10×6×32) - (///) - (////) - (//-) - (① 10×6×64 ② 10×6×32 ③ 5×3×64	⊕ 5×3×128 ⊕ 5×3×64 ⊕ 3×2×128	0 1920
Input image	BLOCK 1		BLOCK 2	вьоск з	

Task:	Human pose estimation	
CNN:	14 / 4.3 / 4 MMAC/frame	
Onboard:	48fps@20mW / 135fps@86mW	
Device: Al-Deck (GAP8)		
arXiv.org https://arxiv.org/abs/2103.10873		









PULP-Dronet v2 for the Al-Deck coming soon on GitHub



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