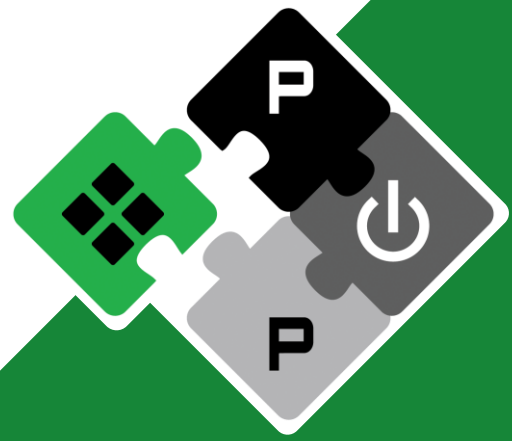
ETH zürich ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA

CachePool: Many-core cluster of customizable, lightweight scalar-vector PEs for irregular L2 data-plane workloads

Integrated Systems Laboratory (ETH Zürich)

Zexin Fu, Diyou Shen zexifu, dishen@iis.ee.ethz.ch

Alessandro Vanelli-Coralli avanelli@iis.ee.ethz.ch
Luca Benini lbenini@iis.ee.ethz.ch



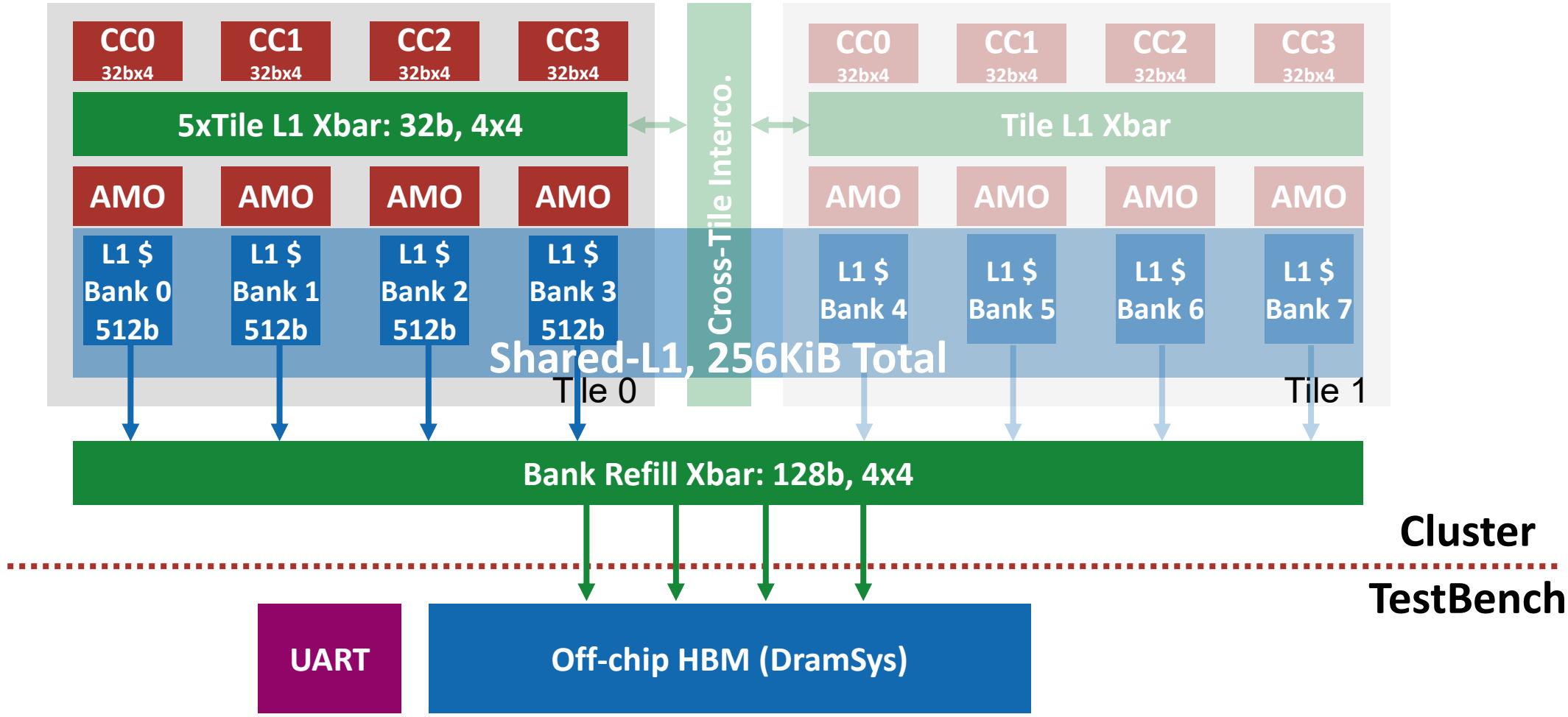
@pulp_platform

pulp-platform.org

youtube.com/pulp_platform

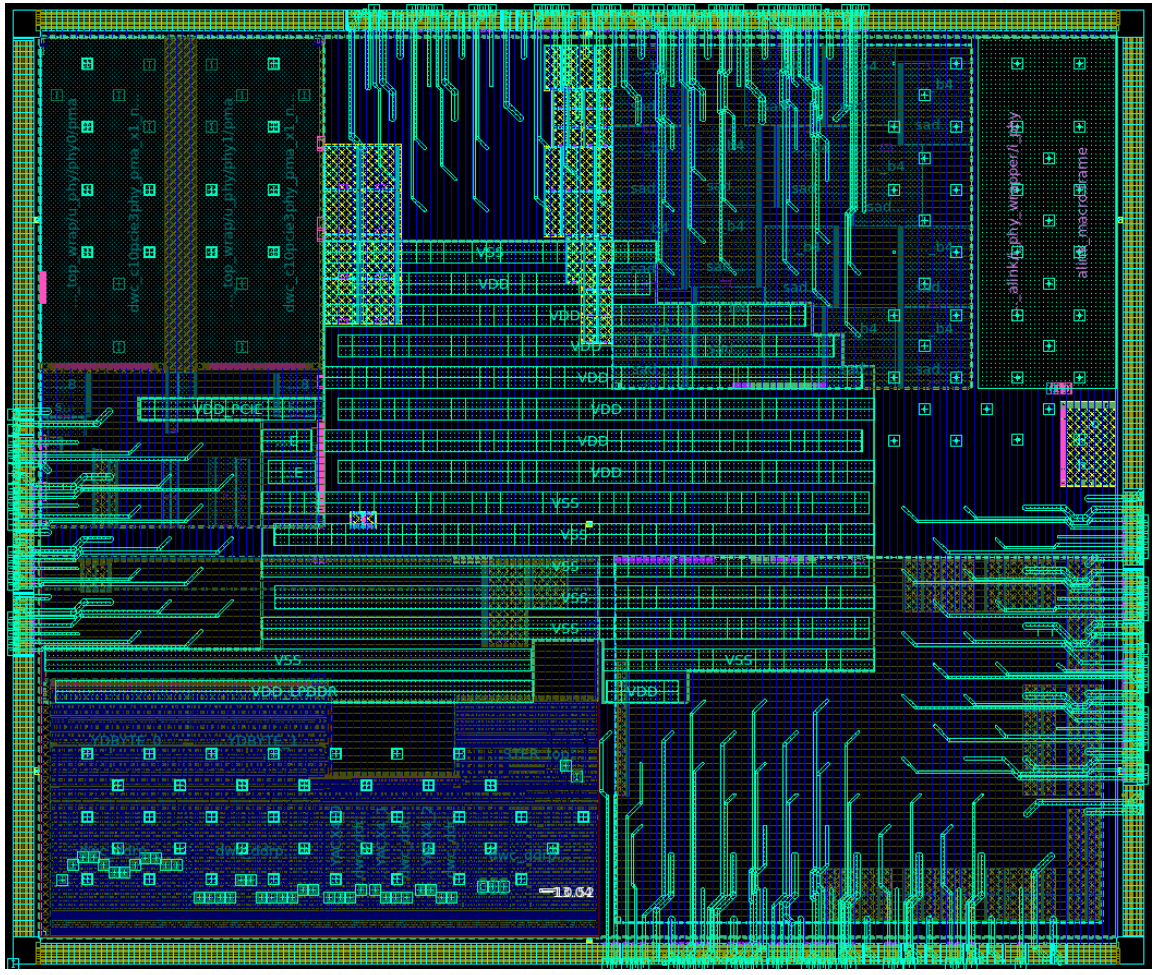
PULP Platform
Open Source Hardware, the way it should be!

Hardware Development



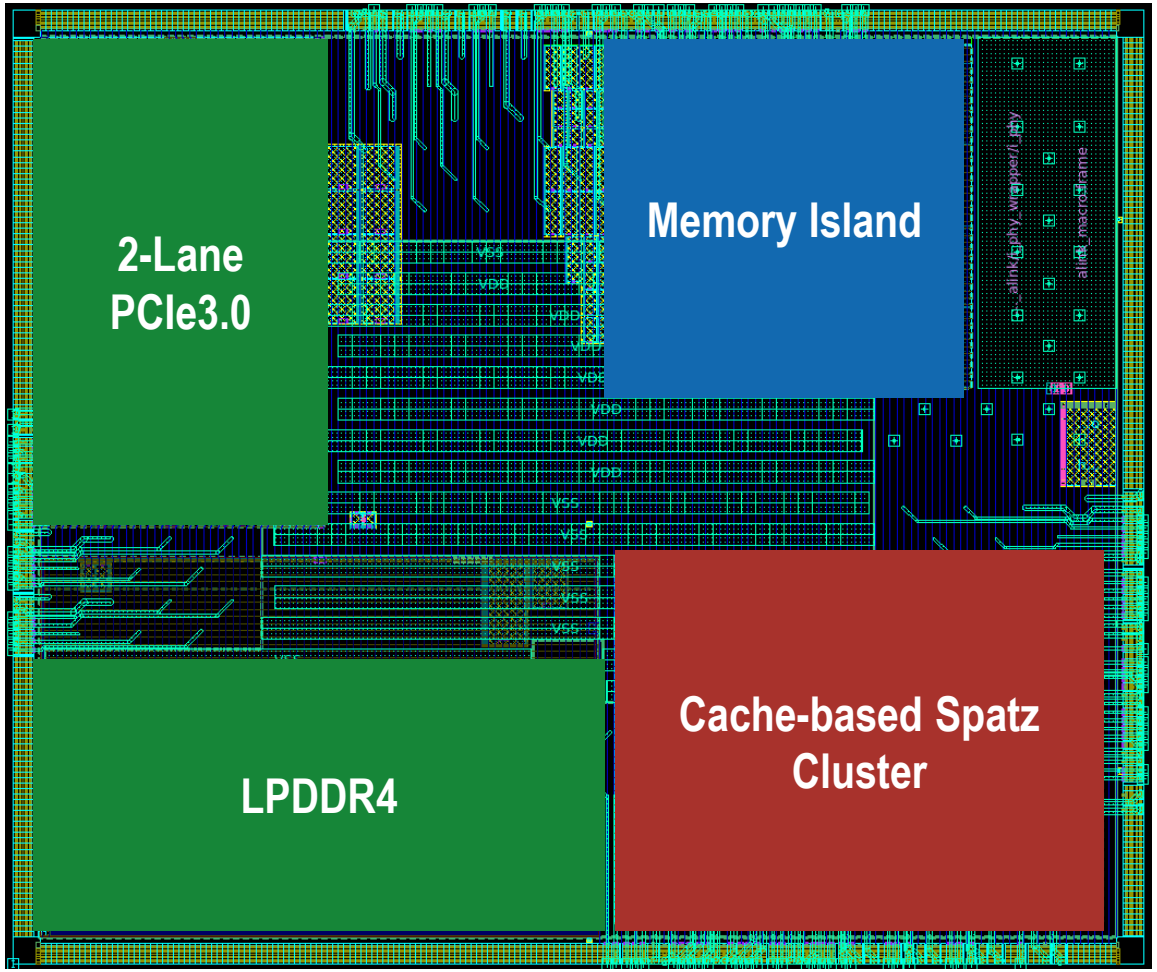
Early Silicon Verification

- **Recently integrated into Flamingo**
  - 22 nm technology
  - DRAM and PCIe controllers on chip
- **Spatz in Flamingo**
  - SPM-based Spatz cluster already in Flamingo
    - Switch from SPM to Cache design
  - 500 MHz
  - Dual **FPU**-enabled **64b** Snitch-Spatz core-complex
  - Shared one 128 KiB L1 InSitu Cache
- **RTL integration done**
  - Backend ongoing
  - Encountered some routing challenges, fixing now



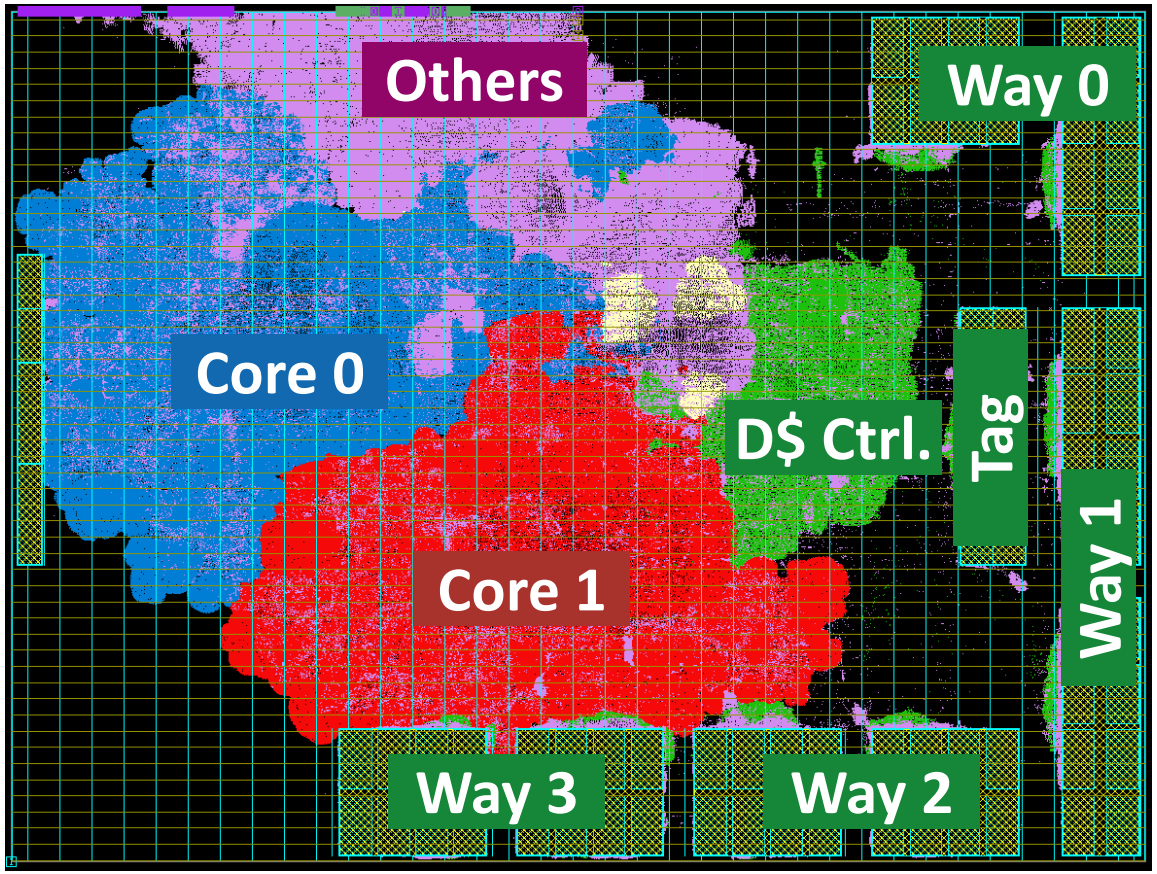
Early Silicon Verification

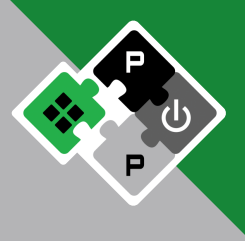
- **Recently integrated into Flamingo**
  - 22 nm technology
  - DRAM and PCIe controllers on chip
- **Spatz in Flamingo**
  - SPM-based Spatz cluster already in Flamingo
    - Switch from SPM to Cache design
  - 500 MHz
  - Dual **FPU**-enabled **64b** Snitch-Spatz core-complex
  - Shared one 128 KiB L1 InSitu Cache
- **RTL integration done**
  - Backend ongoing
  - Encountered some routing challenges, fixing now



Early Silicon Verification

- **Recently integrated into Flamingo**
  - 22 nm technology
  - DRAM and PCIe controllers on chip
- **Spatz in Flamingo**
  - SPM-based Spatz cluster already in Flamingo
    - Switch from SPM to Cache design
  - 500 MHz
  - Dual **FPU**-enabled **64b** Snitch-Spatz core-complex
  - Shared one 128 KiB L1 InSitu Cache
- **RTL integration done**
  - Backend ongoing
  - Encountered some routing challenges, fixing now





Thank you!