

CachePool: Many-core cluster of customizable, lightweight scalar-vector PEs for irregular L2 data-plane workloads

Integrated Systems Laboratory (ETH Zürich)

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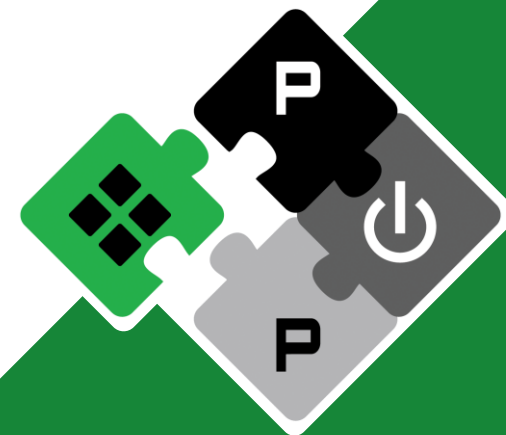
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PULP Platform

Open Source Hardware, the way it should be!



@pulp_platform



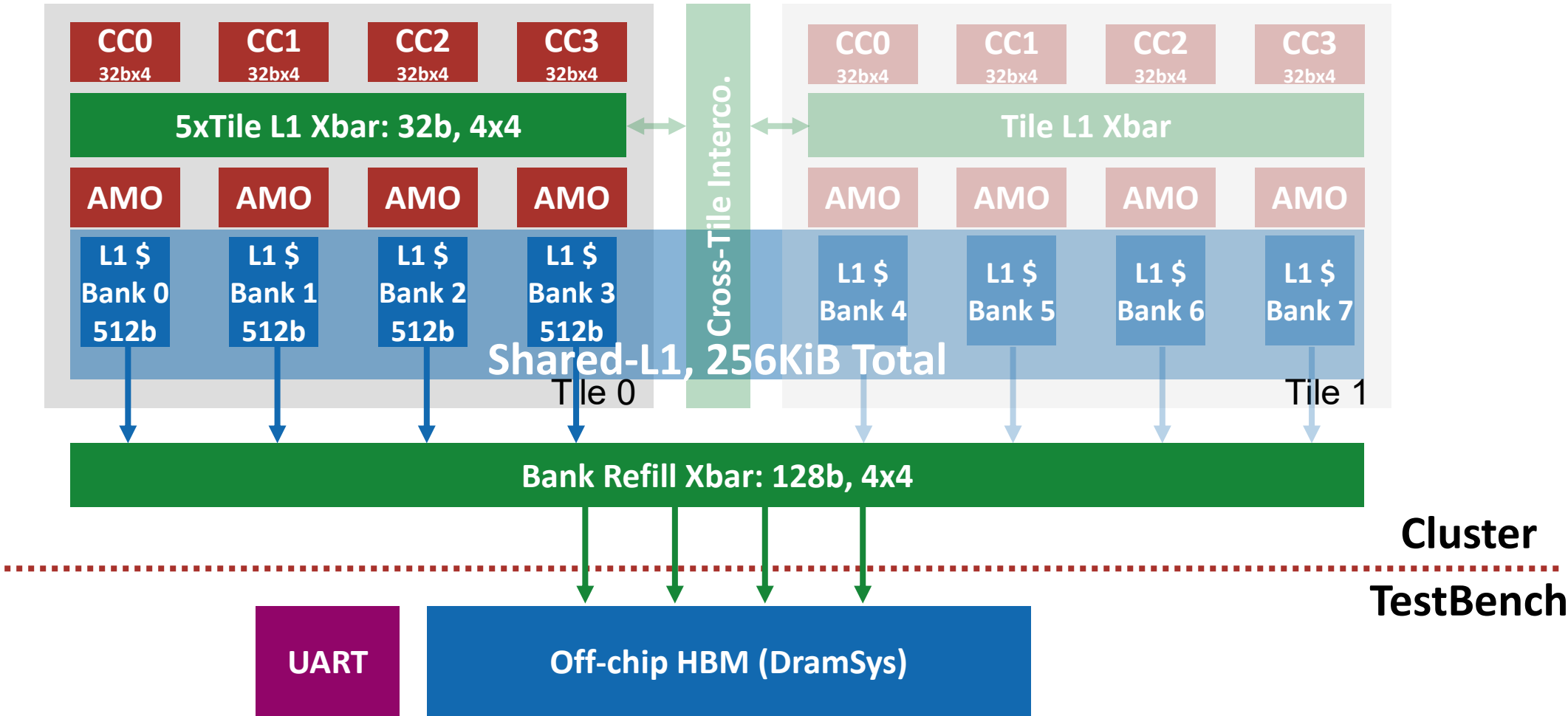
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Hardware Development

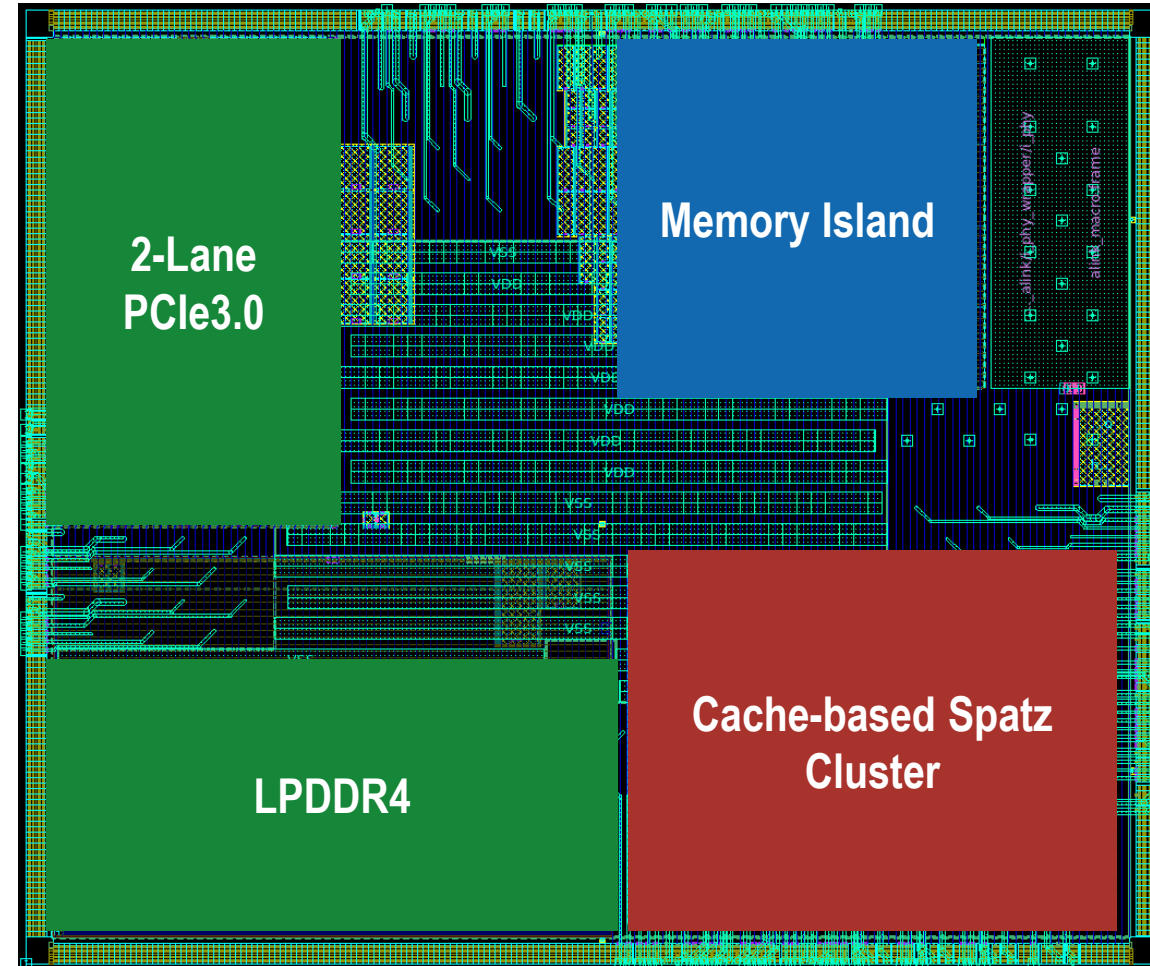


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- This image shows a top-down view of a complex integrated circuit (IC) die. The die is rectangular and densely packed with intricate patterns representing different functional blocks and their interconnections. Key features include:
- Power and Ground Planes:** Large areas labeled "VDD" and "GND" are visible, indicating power and ground distribution.
 - Peripheral Blocks:** Labels such as "top_wgapiu_phy/phy0/pma", "dwc_cl0psie3phy_pma_xl_0...", "top_wgapiu_phy/phy2/pma", and "dwc_cl0psie3phy_pma_xl_0..." are located along the edges, likely representing peripheral controllers or interfaces.
 - Core Logic and Memory:** The central area contains dense grid-like structures, possibly representing memory arrays or core logic blocks.
 - Test Structures:** A label "TEST" is visible near the bottom center, indicating test access points.
 - Die Identification:** A small label "1D.04" is present at the bottom left corner.
- The overall layout is highly symmetrical and organized, typical of modern semiconductor manufacturing.

Early Silicon Verification

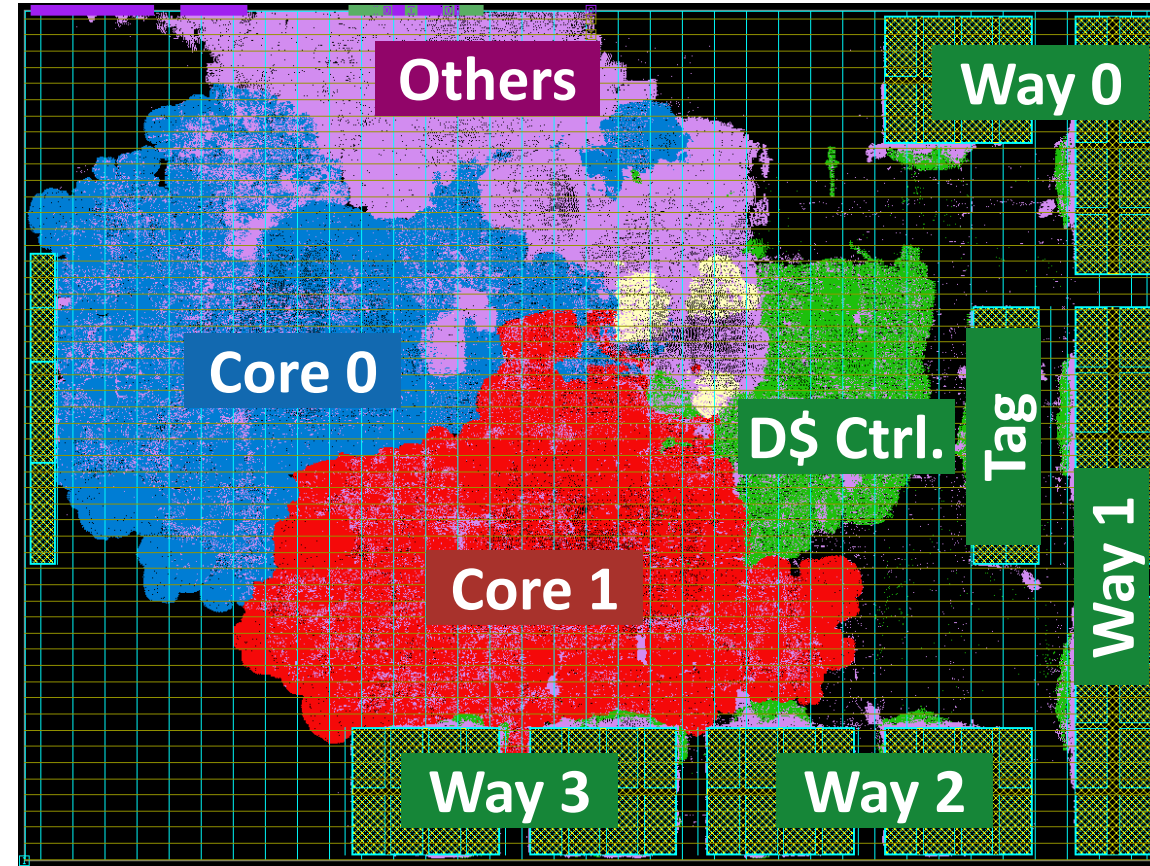


- **Recently integrated into Flamingo**
 - 22 nm technology
 - DRAM and PCIe controllers on chip
- **Spatz in Flamingo**
 - SPM-based Spatz cluster already in Flamingo
 - Switch from SPM to Cache design
 - 500 MHz
 - Dual **FPU-enabled 64b** Snitch-Spatz core-complex
 - Shared one 128 KiB L1 InSitu Cache
- **RTL integration done**
 - Backend ongoing
 - Encountered some routing challenges, fixing now



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Thank you!

Q&A

