ETH zürich

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

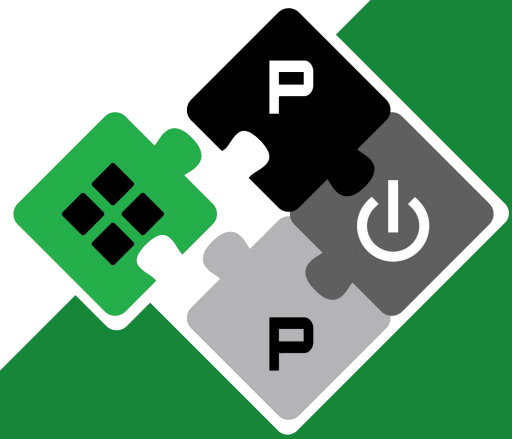
# CachePool: Many-core cluster of customizable, lightweight scalar-vector PEs for irregular L2 data-plane workloads


Integrated Systems Laboratory (ETH Zürich)

**Zexin Fu, Diyou Shen** zexifu, dishen@iis.ee.ethz.ch

**Alessandro Vanelli-Coralli** avanelli@iis.ee.ethz.ch

**Luca Benini** lbenini@iis.ee.ethz.ch

@pulp_platform

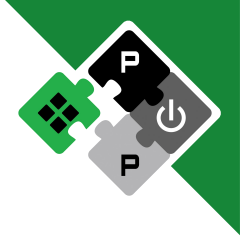
pulp-platform.org

youtube.com/pulp_platform

**PULP Platform**

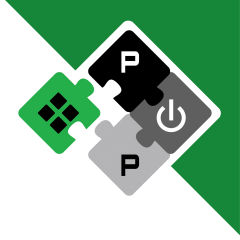
Open Source Hardware, the way it should be!

# Paper Readings



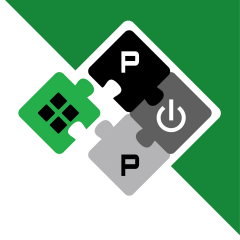
- **Cache Coherence**
  - A Novel Hybrid Cache Coherence with Global Snooping for Many-core Architectures
    https://dl.acm.org/doi/10.1145/3462775
  - SelectDirectory: A Selective Directory for Cache Coherence in Many-Core Architectures
    https://ieeexplore.ieee.org/document/7092378
  - Heterogeneous System Coherence for Integrated CPU-GPU Systems
    https://dl.acm.org/doi/10.1145/2540708.2540747

# A Novel Hybrid Cache Coherence with Global Snooping for Many-core Architectures



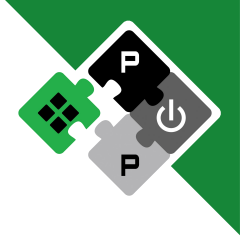
- **Paper Summary**
  - This paper introduce WiSH (Wireless-enabled Share-aware Hybrid) coherence protocol to address scaling challenges in many-core processors.
  - The protocol is built on a Snoopy-over-Directory **hybrid coherence** including **local directory based** within clusters and **global snoopy bus** across clusters by wireless interconnection network.
- **Advantages**
  - Area efficiency: reduce the memory requirements by up to 98% compared to traditional directory-based approach.
  - Better scalability and less traffic.

# A Novel Hybrid Cache Coherence with Global Snooping for Many-core Architectures



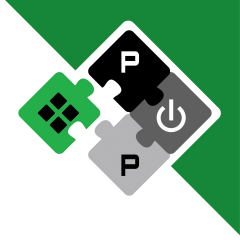
- **Inspirations and Concerns**
  - The **hybrid approach** offers a promising solution for reducing overheads in scaling many-core architectures. Similar strategies, such as **Directory-over-Snoopy**, also warrant consideration as potential solutions for our **cache coherence architecture**.
  - The reliance on **wireless communication between clusters**, while innovative, introduces practical challenges. These include the complexity of **digital-analog co-design**, as well as issues related to **signal integrity**, **power consumption**, and **noise mitigation**. This makes it **inapplicable to our architecture**, which requires simpler and more predictable interconnect mechanisms.
  - Without the wireless communication, the high bandwidth requirement of Snoopy bus between clusters might become the bottleneck in latency and scaling.

# SelectDirectory: A Selective Directory for Cache Coherence in Many-Core Architectures



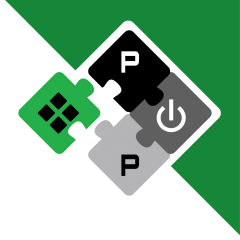
- **Paper Summary**
  - This paper introduces SelectDirectory, a compact directory-based cache coherence protocol for many-core architecture.
  - It contains the following key design points
    - Selective Directory: separate tag array and coherence metadata (data) array. Tag Array tracks all memory block, but Data Array only allocates entries for actively shared blocks
    - Coherence Management: Fill in Data Array entry when a block transit from private to shared and deallocate it when from shared to private.
- **Advantages**
  - Save the SRAM space required for directory up to 2x.
  - Better scalability for many-core architecture

# SelectDirectory: A Selective Directory for Cache Coherence in Many-Core Architectures



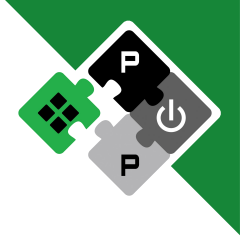

- **Inspirations and Concerns**
  - The approach can be treated as **a "pro" version of MESI** directory based coherence, which also reduce the number of metadata needed to be stored. It can be a good addition on top of other approaches, e.g. Snoopy-over-Directory and Directory-over-Snoopy.
  - This approach alone still face problems when scaling up to hundreds and thousands of cores. For the highly parallel workload, such a strong coherence may not be needed globally. It is possible to apply it across 8-16 cores, and uses software synchronization at a higher hierarchy.

# Heterogeneous System Coherence for Integrated CPU-GPU Systems



- **Paper Summary**
  - This paper introduces Heterogeneous System Coherence (HSC), a hardware solution designed to address the performance bottlenecks caused by high memory bandwidth demands and coherence traffic in heterogeneous systems.
  - It contains the following key design points
    - Region-Based Coherence: HSC replaces the conventional block-level directory with a region directory and introduces region buffers. These structures track coherence permissions at a coarser granularity, reducing the bandwidth and overhead of coherence traffic.
    - Directory bypassing: By granting permissions for entire memory regions rather than blocks, most L2 cache misses can directly access memory without accessing the directory.
- **Advantages**
  - Make the directory more scalable in terms of both access bandwidth and capacity.
  - Allow the system to move bandwidth from the coherence network to the high-bandwidth direct-access bus without sacrificing coherence.

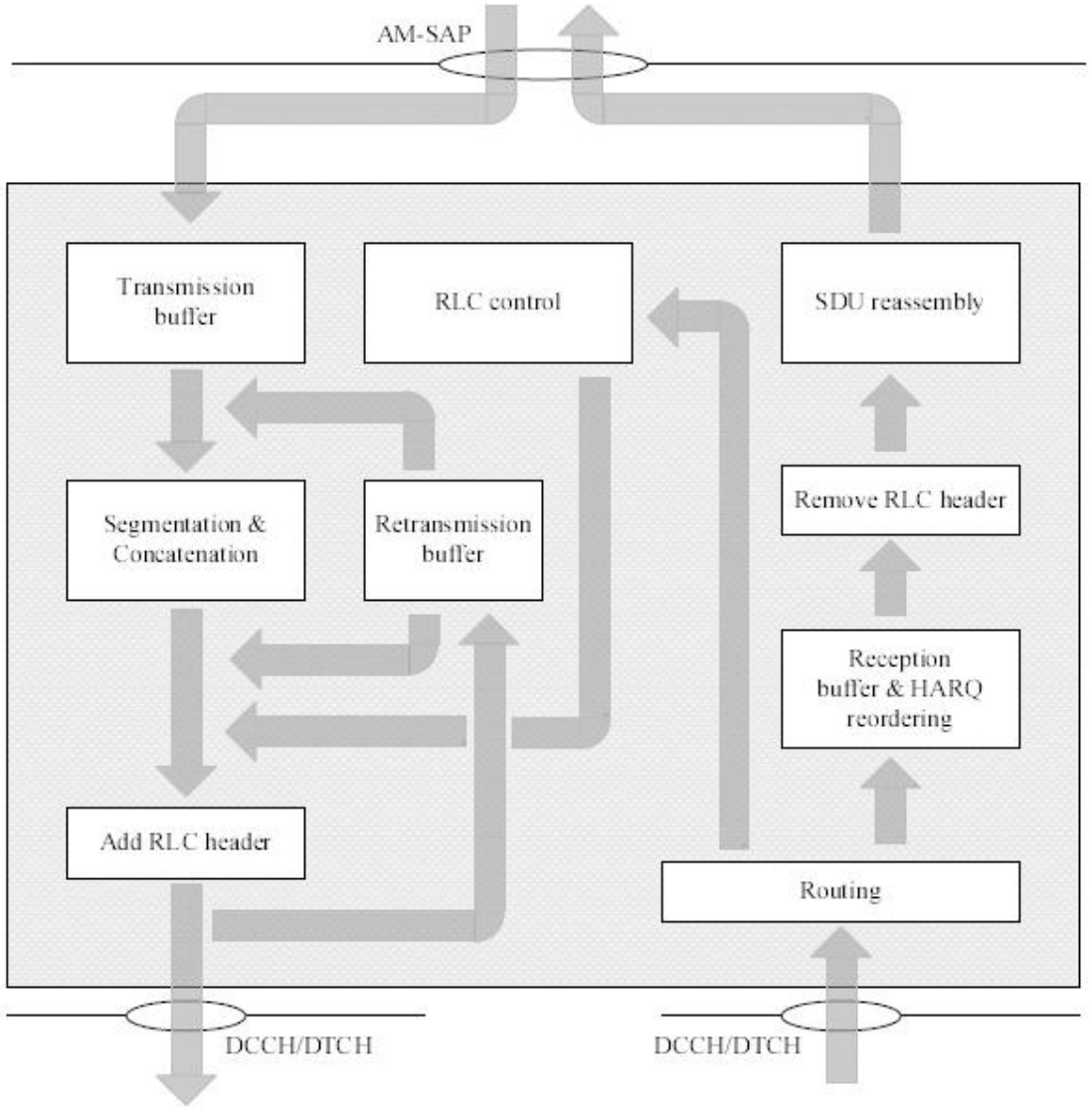
# Heterogeneous System Coherence for Integrated CPU-GPU Systems



- **Inspirations and Concerns**
  - The **Region-Based Coherence** approach introduced in the paper capitalizes on the spatial and temporal locality of memory accesses by granting coherence permissions for **larger memory regions** rather than **individual cache blocks**. This technique is particularly beneficial in systems where specific memory regions are actively used by a small set of cores (e.g., a tile) for a period and then handed off to another set of cores.
  - To further improve efficiency, we can enhance the design by integrating hints or configurations from software side to **dynamically adjust the size** of region directory entries. This adaptability would enable finer-grained coherence management, tailored to specific workload characteristics, further optimizing coherence traffic, memory access bandwidth and directory utilization.

# DataPlane-RLC

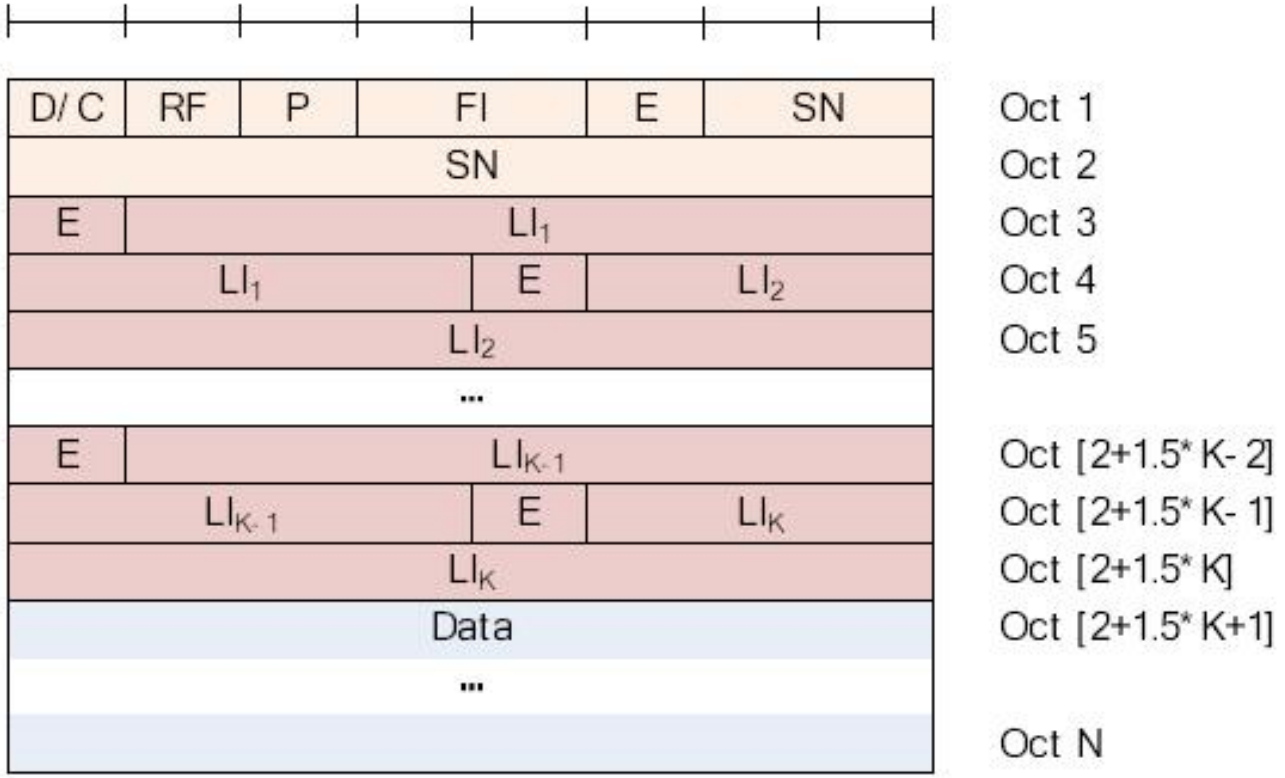
- **Data Flow**
  - *o* Two flows
    - Transmitting Flow
    - Receiving Flow
  - *o* Three modes
    - Transparent Mode
    - Unacknowledge Mode
    - Acknowledge Mode (need retransmission)



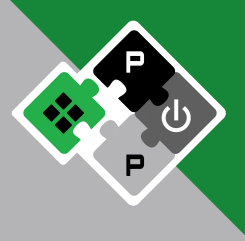

Source: https://www.sharetechnote.com/html/RLC_LTE.html

# DataPlane-RLC

- **Data Structure**
  - Three modes
    - TMD (TM mode data)
    - UMD (UM mode data)
    - AMD (AM mode data)
- Fields
  - D/C: Control or Data PDU
  - RF: Type of the AMD PDU
  - P: Requiring a status report
  - FI: Relative location within a SDU
  - E: End of the header




Source: https://www.sharetechnote.com/html/RLC_LTE.html




# Thank you!