ETH zürich ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA

CachePool: Many-core cluster of customizable, lightweight scalar-vector PEs for irregular L2 data-plane workloads

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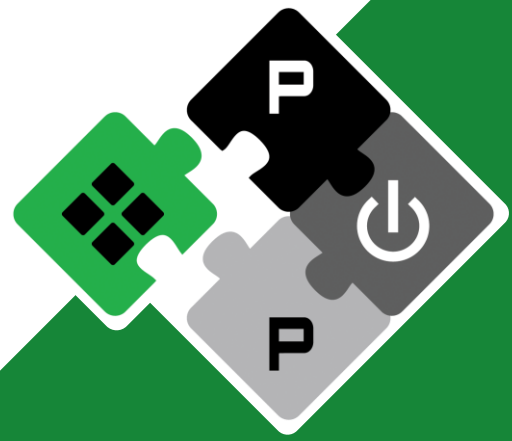

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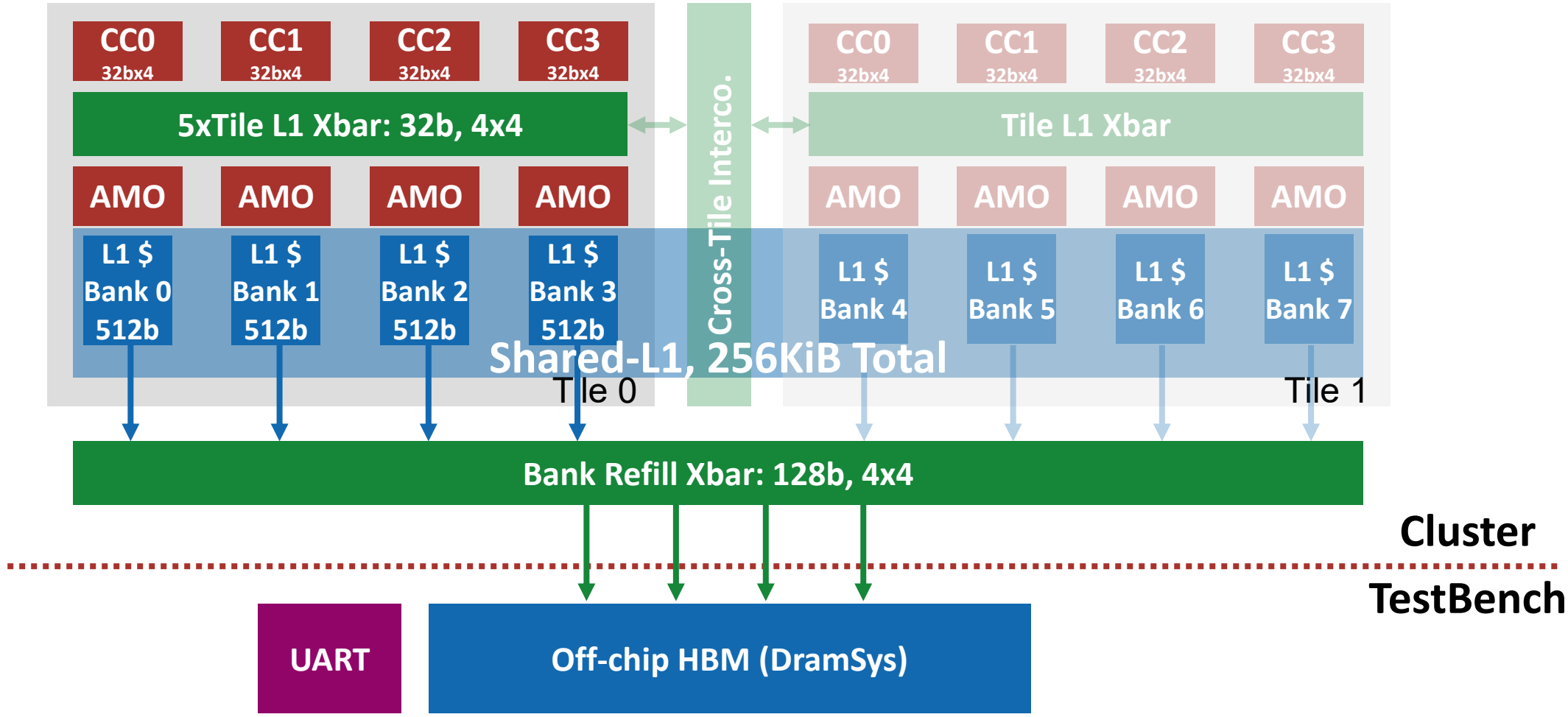
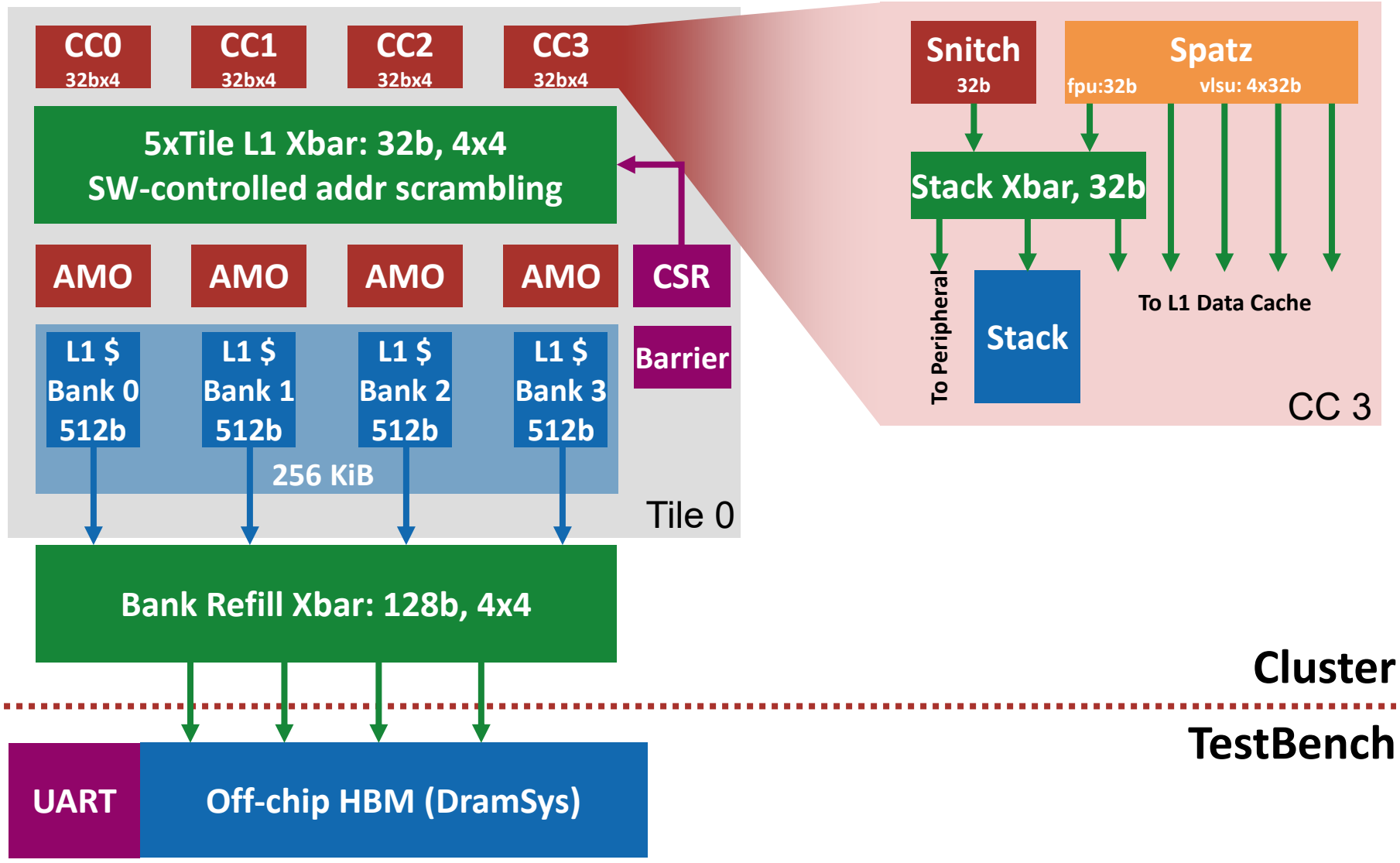
PULP Platform
Open Source Hardware, the way it should be!

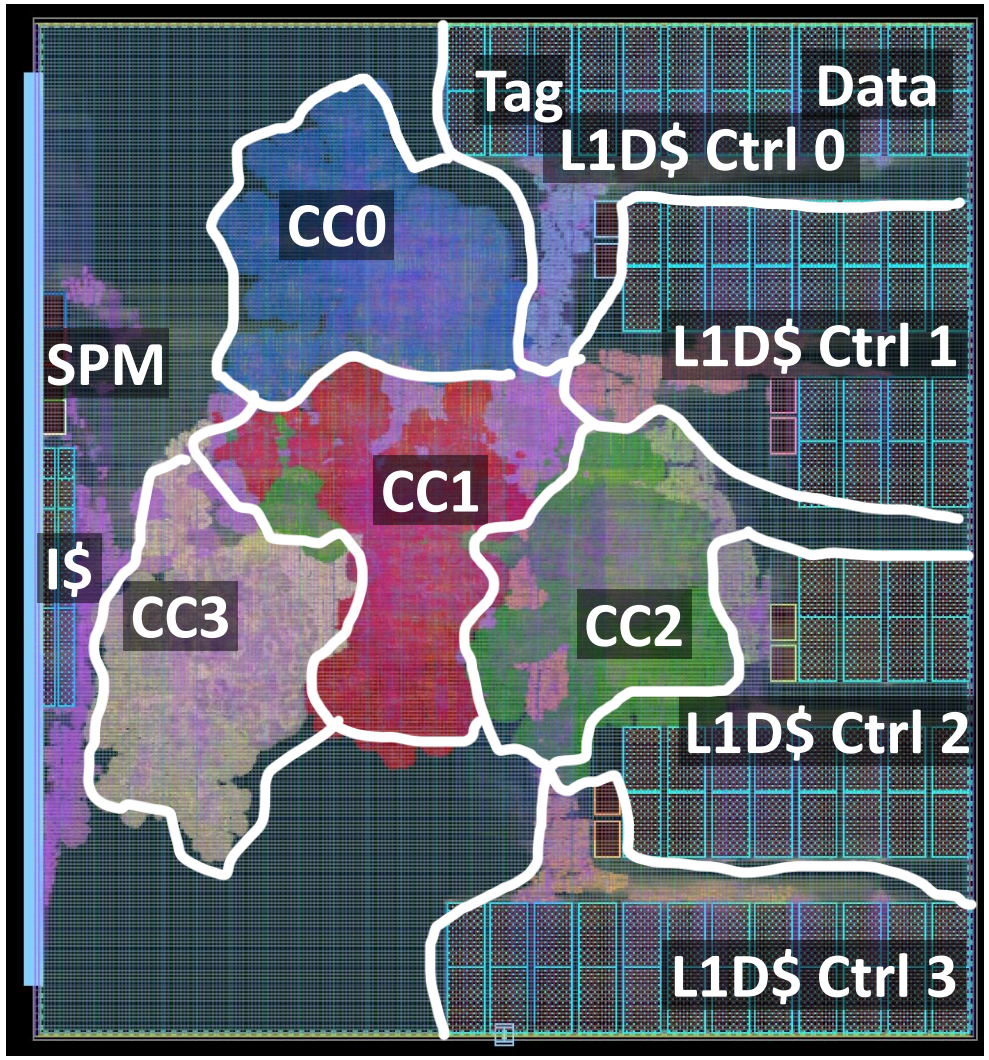
Hardware Development

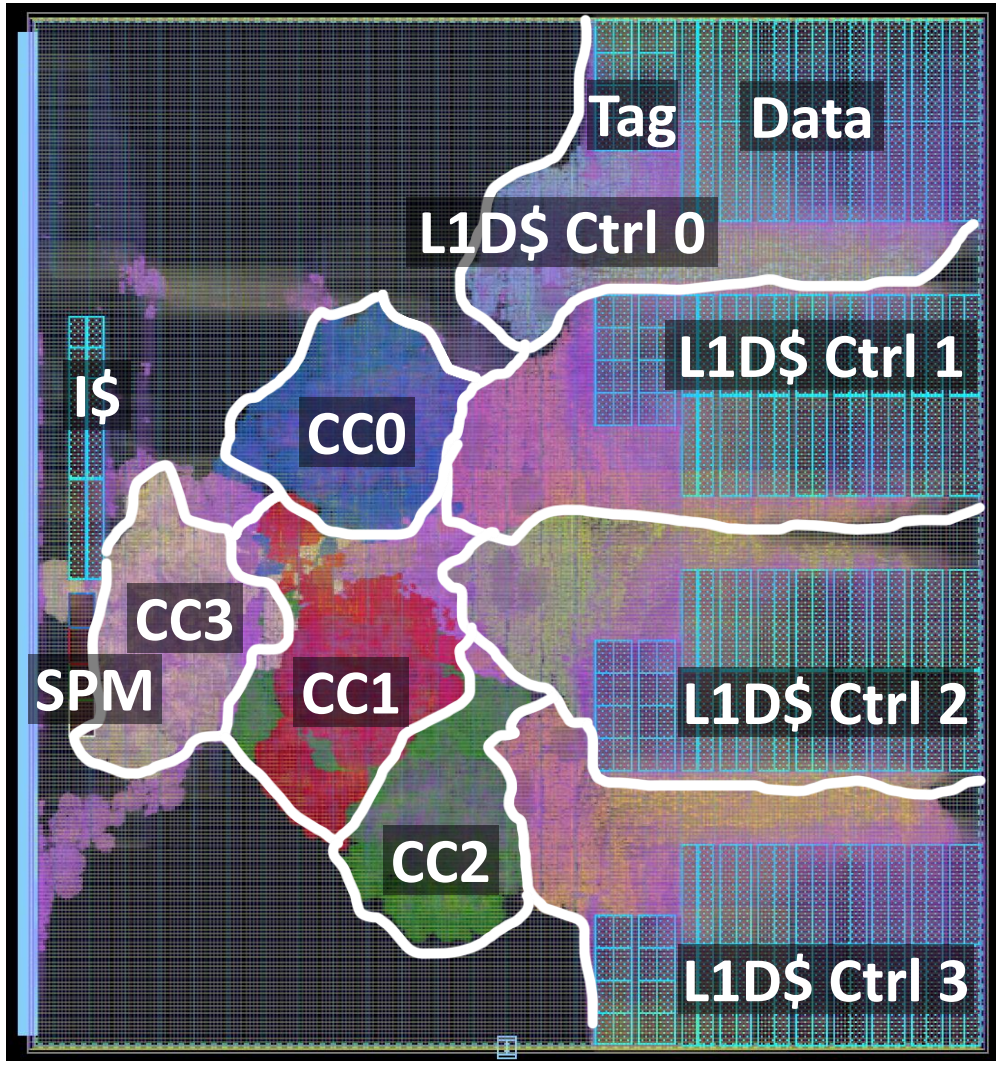


Hardware Development



Area Analysis





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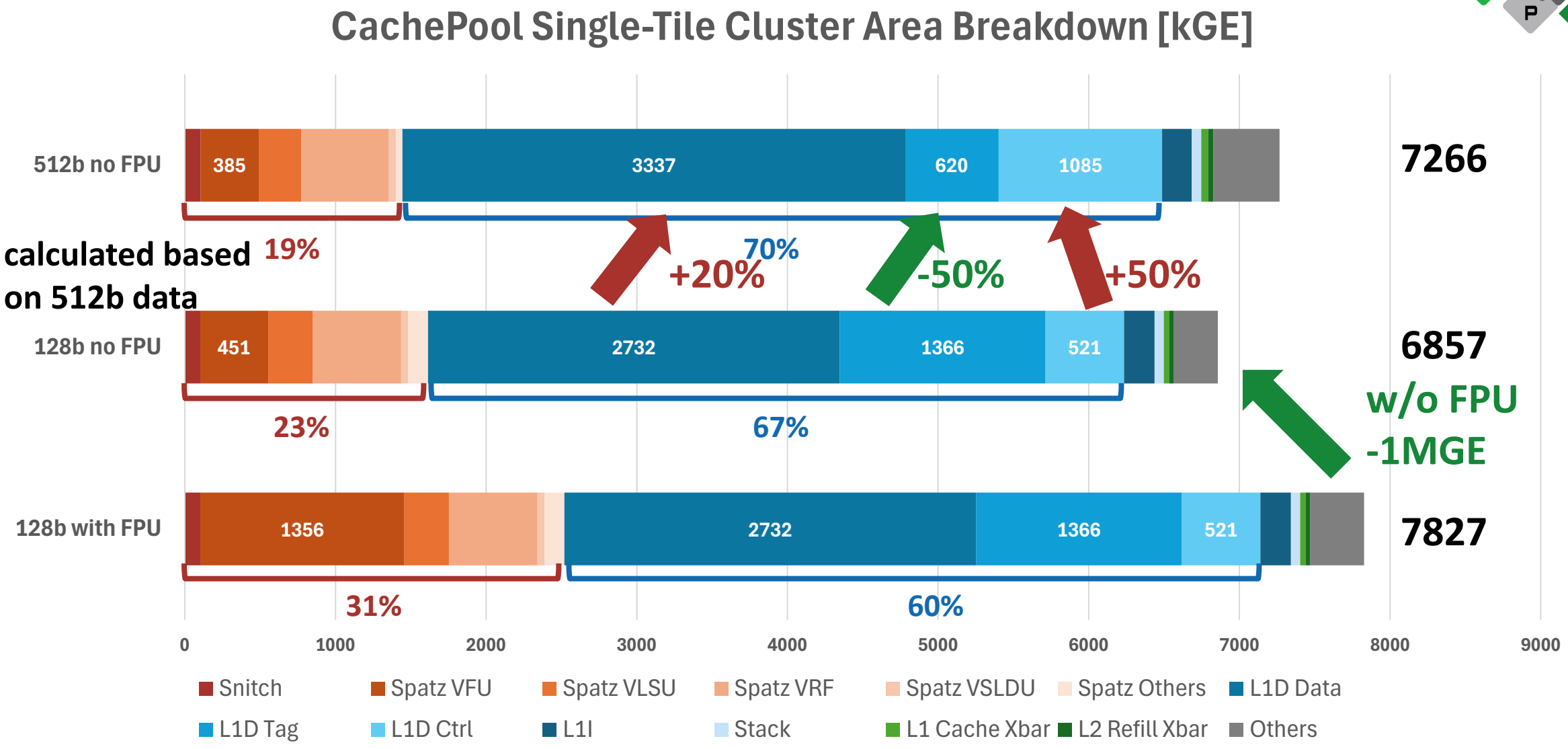
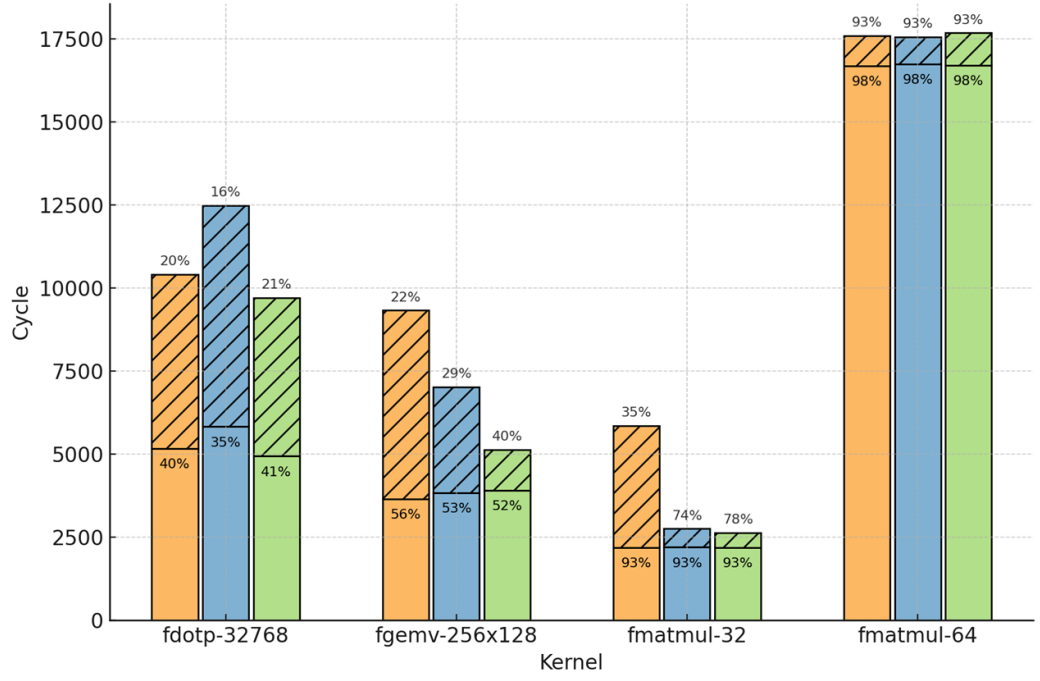


Area Analysis

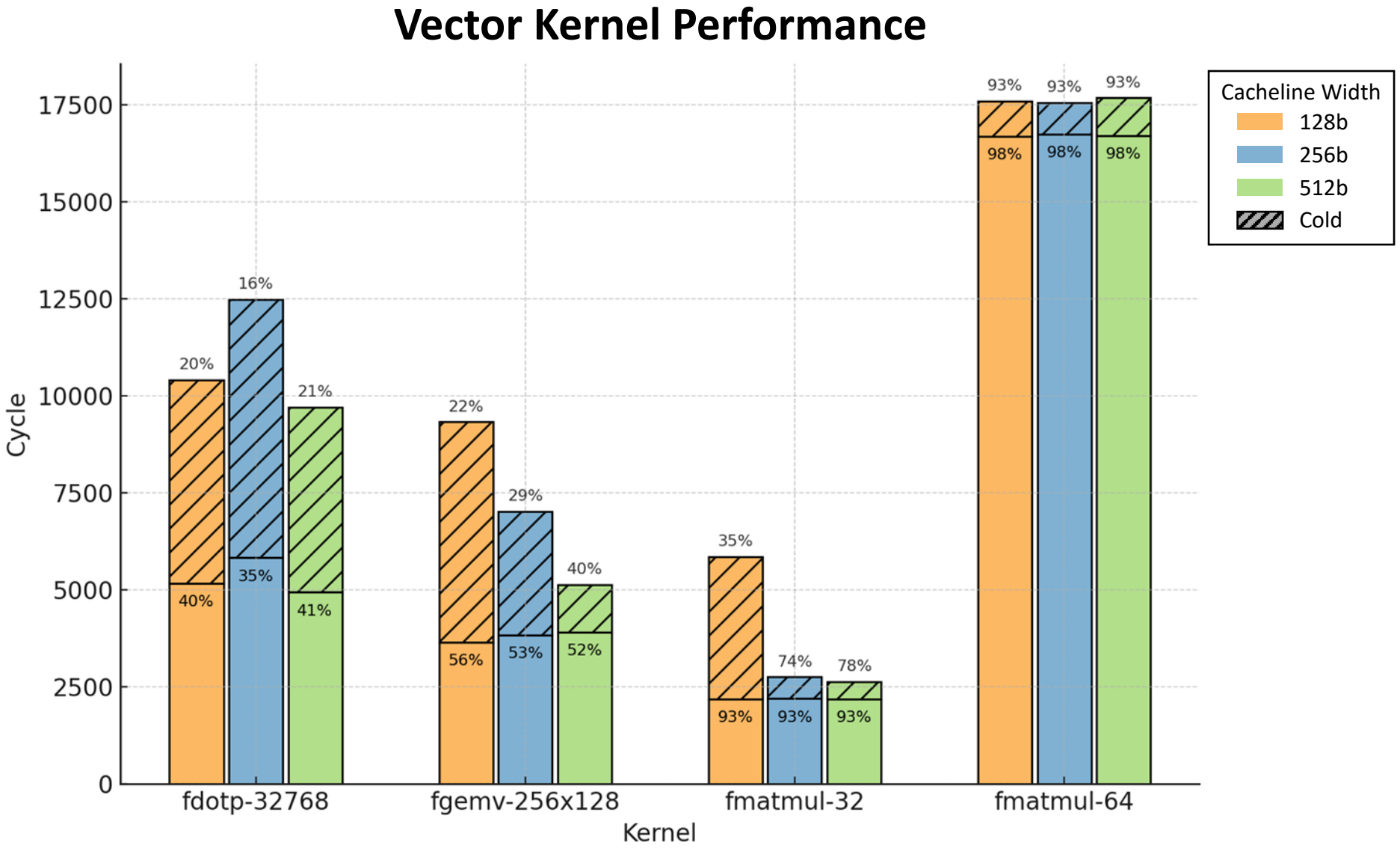
- **More difficult routing encountered**
- **FPU occupies 1MGE**
  - The compute-to-area around 20% without FPU
- **Cache Area Scaling**
  - Controller doubled from 128b to 512b
    - Due to scaling of FIFOs inside controller
    - Have some ideas to fix, will discuss internally first
  - Data bank increased by 20%
    - Due to lack of available macros
  - Tag bank reduced by 50%
    - Expected

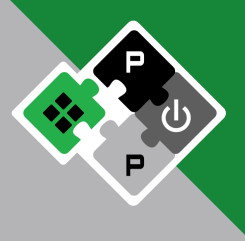
Software Analysis – Different Cacheline Width

- **Performance does not differ much for hot cache**
  - Metrics: FPU/IPU Utilization
  - 256b-cacheline performs bad in dotp
    - Encountered some conflicts between VFU and VLSU
    - Will be fixed soon by my colleague working on vector PE
  - GEMV encounters performance drop with cacheline width
    - Encountered some evictions near the end of kernel



Software Analysis – Different Cacheline Width





Thank you!