1.1 Dependency between REQ_O and GNT_I

1.1.1 Summary

Description	The RI5CY bus interface implies either a combinational path from REQ_O to GNT_I or insertion of pipeline stages (i.e. additional latency) on this path.
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1.1.2 Description

The **Error! Reference source not found.** states the following:

> The protocol that is used by the LSU to communicate with a memory works as follows:
>
> The LSU provides a valid address in data_addr_o and sets data_req_o high. The memory then answers with a data_gnt_i set high as soon as it is ready to serve the request. This may happen in the same cycle as the request was sent or any number of cycles later.

Above definition of the RI5CY bus interface implies either a combinational path from REQ_O to GNT_I (i.e. a master-to-slave-to-master path) or insertion of pipeline stages (i.e. additional latency) on this path. We would like to enable systems without round-trip combinational paths between masters and slaves nor unnecessary mandated pipelining on bus interfaces. Our proposal would be to remove the restriction/requirement highlighted in red above, therefore allowing default grants to be sent by a slave. It should for example be acceptable for a slave to tie its GNT high if the slave knows it can always handle an incoming REQ.