Puneesh Deora

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Education

- **Indian Institute of Technology Roorkee** — Uttarakhand, India
  B.Tech, Electronics and Communication; GPA: 8.259/10.0 — *July 2016 – Present*

Areas of Interest

Image Processing, Inverse Problems, Deep Learning, Signal Processing, Optimization Problems, Compressive Sensing.

Relevant Courses Completed

Digital Image Processing, Digital Signal Processing, Probability & Statistics, Signals & Systems, Principles of Digital Communication, Information and Coding Theory, Machine Learning (Stanford University, Coursera), Communication Systems & Techniques, Technical Communication

Publications

1. **P. Deora**, B. Vasudeva, S. Bhattacharya, P.M. Pradhan, "Robust Compressive Sensing MRI Reconstruction using Generative Adversarial Networks". (*Under review in IEEE ICASSP 2020*)
2. B. Vasudeva, **P. Deora**, P.M. Pradhan, S. Dasgupta, "FPGA Implementation of Efficient Series and Parallel Architectures for LMS Adaptive Filter based FECG Extraction". (*Under review in IEEE ICASSP 2020*)
3. N. Singh, **P. Deora**, P.M. Pradhan, "Simultaneously Concentrated PSWF-Based Synchrosqueezing S-Transform and Its Application to R Peak Detection in ECG Signal". (*Accepted for a special session in IEEE RO-MAN 2019*)

Key Projects

- **Robust CS-MRI Reconstruction using GANs** [Preprint] — Research project
  Guide: Prof. Saumik Bhattacharya, Prof. P.M. Pradhan — *June'19 - Present*
  - A GAN based framework for compressive sensing MRI reconstruction is proposed.
  - To preserve fine textural details, a patchGAN discriminator and SSIM based loss is used.
  - A U-net based generator architecture incorporating residual in residual dense blocks to improve information flow is proposed.
  - To make the reconstruction robust to noise, noisy images are used for data augmentation to train the GAN model.
  - A significant boost in PSNR, MSSIM is achieved as compared to GAN based, and conventional CS-MRI reconstruction techniques.

- **Low Light Image Enhancement** [Report] — Course project
  Guide: Prof. Saumik Bhattacharya — *Feb'19 - Apr'19*
  - A retinex based approach for modelling the low-light input as the product of desired scene and illumination map is used.
  - The illumination map is optimized via an ADMM based approach which aims at preserving structure and smoothening textural variations.
  - This approach is compared with different histogram equalization based techniques, with transformation being applied in different color spaces.

- **FECG extraction and QRS complex study using BSS based techniques** Research project
  Guide: Prof. P.M. Pradhan *July'18 - Aug'18*
  - Preprocessed raw abdominal ECG signals, used the FastICA algorithm to separate the underlying sources.
  - Obtained the morphology of fetal ECG (FECG) by application of PCA on one of the sources (corresponding to the FECG). Implemented in MATLAB.

- **FPGA Implementation of FHR Monitoring System** [Preprint] Research project
  Guide: Prof. P.M. Pradhan & Prof. S. Dasgupta *May'18 - Nov'18*
  - Preprocessed raw thoracic and abdominal ECG signals, extracted FECG using LMS adaptive filter, detected RR intervals and fetal heart rate (FHR) using a modified version of the Pan and Tomkins algorithm.
  - Implemented the system using C on a Raspberry Pi. Tested it on both real and simulated ECG signals.
  - Implemented the entire system on FPGA with series and parallel architectures of the LMS adaptive filter. Developed a floating point unit for carrying out the arithmetic operations.

Other Projects

- **Study of Basic Components of a Wireless Communication System** Lab-based Project
  Guide: Prof. P. M. Pradhan *Feb'19 - Apr'19*
  - Implementation of orthogonal frequency division multiplexing (OFDM) transmitter and receiver. Testing of MPSK, MQAM, MPAM modulators and demodulators under Rayleigh, Rician, time invariant and variant channels.
  - Comparison of variable step size LMS based adaptive filters for channel estimation and equalization.

- **HDL Implementation of PCA for Signal Denoising** [Report] Course project
  Aug'18 - Nov'18
  - Verilog implementation of Principal Component Analysis (PCA) algorithm for noise removal in signals using Givens rotation based QR decomposition.
  - Implementation of various modules for vector centering, transposition, multiplication of matrices, and CORDIC for Givens rotation.

- **Hannibal: A 24-bit pipelined RISC Processor** Course Project
  Guide: Prof. Vaskar Raychoudhury *Sep'17 - Nov'17*
  - Design and Verilog Implementation of 24-bit RISC processor.
  - Python Assembler for the pipelined processor.
  - Compared the performance with non-pipelined 24-bit and 32-bit processors.

Technical Skills

- **Programming Languages**: Python, C, C++, Verilog-HDL, Java
- **Softwares and Tools**: MATLAB, Keras, Vivado, Cadence Virtuoso, LTSpice, LaTeX

Scholastic Achievements

- Secured **All India Rank** 1123, in IIT JEE Advanced 2016, among 1.1 million candidates.
- Eligible for **CBSE INSPIRE** scholarship **2016**.