Puneesh Deora

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Education

- **Indian Institute of Technology Roorkee** — Uttarakhand, India
  B.Tech, Electronics and Communication; GPA: 8.148/10.0 — *July 2016 – Present*
- **Kundan Vidya Mandir School** — Punjab, India
  Class XII; Percentage: 86.2% — *2015*
- **Kundan Vidya Mandir School** — Punjab, India
  Class X; GPA: 10.0/10.0 — *2013*

Relevant Courses Completed

Probability & Statistics, Signals & Systems, Principles of Digital Communication, Machine Learning (Stanford University, Coursera), Communication Systems & Techniques, Embedded Systems, Technical Communication, Digital Image Processing*, Digital Signal Processing*

*will be completed by: *April 2019.*

Projects

- **HDL Implementation of PCA for denoising signals** — Course project
  Aug'18 - Nov'18
  - Verilog implementation of Principal Component Analysis (PCA) algorithm for noise removal in signals using Givens rotation based QR decomposition.
  - Implementation of various modules for vector centering, transposition, multiplication of matrices, and CORDIC for Givens rotation.
- **FECG extraction and QRS complex study using BSS based techniques** — Research project
  Guide: Dr. P.M. Pradhan — *July'18 - Aug'18*
  - Preprocessed the raw abdominal signals, used the FastICA algorithm to separate the underlying sources.
  - Obtained the morphology of fetal ECG (FECG) by application of PCA on one of the sources (corresponding to the FECG). Implemented in MATLAB.
- **Implementation of FHR Monitoring System for FECG extraction** — Research project
  Guide: Dr. P.M. Pradhan & Dr. S. Dasgupta — *May'18 - July'18*
  - Preprocessed raw thoracic and abdominal ECG signals, extracted FECG using Least Mean Squares Adaptive Filter (LMS-AF), detected RR intervals and Fetal Heart Rate (FHR) using the Pan and Tomkins Algorithm.
  - Implemented the system using C on a Raspberry Pi. Tested it on both real and simulated ECG signals.
  - Implemented the entire system on FPGA with series and parallel architectures of the LMS algorithm. Developed a floating point unit for carrying out the arithmetic operations.
  - A manuscript is under review in IEEE-TBioCAS.
- **Hannibal: A 24-bit pipelined RISC Processor** — Course Project
  Guide: Dr. Vaskar Raychoudhury — *Sep'17 - Nov'17*
  - Design and Verilog Implementation of 24-bit RISC processor.
  - Python Assembler for the pipelined processor.
  - Compared the performance with non-pipelined 24-bit and 32-bit processors.

Technical Skills

- **Programming Languages**: C, C++, Python, Verilog-HDL, Java
- **Software Skills**: MATLAB, Vivado, Cadence Virtuoso, LTSpice, Adobe Illustrator, LaTeX
- **Operating Systems**: Windows, Linux-Ubuntu
- **Languages**: English, Hindi, Punjabi

Scholastic Achievements

- Secured **All India Rank** 1123, in IIT JEE Advanced 2016, among 1.1 million candidates.
- Eligible for **CBSE INSPIRE** scholarship **2016**.