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Vellore Institute of Technology

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Reg. No. : 22BAI1166

Final Assessment Test (FAT) - May 2024

Programme	**B.Tech.**	Semester	**WINTER SEMESTER 2023 - 24**
Course Title	**COMPUTER ARCHITECTURE AND ORGANIZATION**	Course Code	**BCSE205L**
Faculty Name	**Prof. Monica K M**	Slot	**F1+TF1**
		Class Nbr	**CH2023240501631**
Time	**3 Hours**	Max. Marks	**100**

General Instructions:

- Write only Register Number in the Question Paper where space is provided (right-side at the top) & do not write any other details.

Answer all questions (10 X 10 Marks = 100 Marks)

01. i) Compare the features of RISC and CISC architectures in terms of the instruction set architecture, instruction formats and lengths, and addressing modes.[5 marks] **[10]**

ii) A processor is going to execute the following instruction

ADD R1 400

Illustrate how the processor will perform *ADD* instruction (*ADD* adds a number at memory location 400 and content of register R1 and stores the result in R1) by using read, execute, and write signals to execute the above instruction. Use diagrams to show the entire operation [5 marks]

02. For a processor that performs multiplication using Booth's Algorithm, answer the following: **[10]**

i. Show the step-by-step process for multiplying $(-22)_{10}$ and $(10)_{10}$. [7 Marks]

ii. Find the decimal equivalent of the content of the accumulator at the end of the second iteration. [3 Marks]

03. Demonstrate floating point subtraction for $(40.625)_{10}$ - $(11.025)_{10}$ **[10]**

i) Show a step-by-step process for performing floating point subtraction for the above decimal number. [7 marks]

ii) Also represent the final result in a single precision format. [3 marks]

04. i) Illustrate the architectural design of multiple cycle data path to fetch and execute the following instructions (4 Marks) **[10]**

LDA (R2)

MUL R1

ADD R1, R2

ii) Write down the micro routine control sequence steps involved in the architecture for the given instructions in 4 (i). (6 Marks)

05. i) A block–set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16384 blocks and each block contains 256 eight-bit words. **[10]**

a. How many bits are required for addressing the main memory? [3 marks]

b. How many bits are needed to represent the TAG, SET, and WORD fields? [4 marks]

ii) Is there a need to include a multi-level cache in computer architecture? Justify your answer with the help of a diagram. [3 marks]

06. A processor is connected to four external devices (D1, D2, D3, and D4) in parallel. One or more than one devices can request access to the CPU. In case of multiple requests, the high-priority device gets access to the CPU. The priority level of each device is given in the table below with 1 denoting highest priority and 4 denoting least priority. **[10]**

Device name	Priority
D1	4
D2	3
D3	1
D4	2

i. Suggest and explain a suitable technique that resolves multiple interrupt-driven I/O requests simultaneously. Use an appropriate diagram to explain your approach. [5 marks]

ii. For the given technique, explain what happens when D1, D3, and D4 requests interrupt service at the same time. [5 marks]

07. A medium-sized e-commerce platform is considering implementing a RAID configuration to enhance data reliability and performance for its online transaction database. The database contains critical customer information and transaction records, and any downtime or data loss could have severe financial repercussions for the company. After assessing their requirements and budget constraints, they are torn between implementing RAID 1 or RAID 5. As a systems architect, how would you advise the company on choosing the most suitable RAID level for their database system? What factors would you consider, and how would you explain the trade-offs between RAID 1 and RAID 5 in terms of data redundancy, performance, and cost-effectiveness to the company's management team? **[10]**

08. A bit-stream 110011101 is transmitted using the standard error detection using the generator polynomial x^4+1. **[10]**

i. Compute the actual bit string transmitted. [4 Marks]

ii. Suppose the third bit from the left is inverted during the transmission. Help the receiver detect the error. [4 Marks]

iii. Draw the flow chart to detect the error [2 Marks]

09. i. A processor's execution time was intended to be reduced by 40% by adding parallel processors to it. However, this resulted in an increase of the CPI by 20%. What % of an increase in the clock rate would result in the estimated decrease in execution time? [5 Marks] **[10]**

ii. A processor works on the non-pipelining concept with an average CPI of 2.5 and a clock rate of 3GHz. After two years, the company decided to upgrade the processor to a pipelined architecture with six stages. Due to design constraints, this upgrade led to a decrease in clock rate to 2GHz. Assume that this upgrade makes the pipelining architecture an ideal one with no stalls, and find the speed up achieved in upgrading the processor. [5 Marks]

10. i) Mul R2,R3,R4 **[10]**

Add R5, R6, R7

During the pipeline execution, it's noticed that both instructions require access to the memory unit simultaneously. Identify the type of hazard encountered in this scenario and propose strategies to address this issue. Provide a step-by-step explanation of each strategy and discuss how it mitigates the hazard effectively [5 marks].

ii) In the realm of processor design, a team of engineers is tasked with developing a high-performance pipelined processor architecture for a next-generation computing platform. As they venture into the intricate realm of pipelining, they encounter the challenge of managing data dependencies and ensuring seamless instruction execution. Amidst this endeavor, the concept of operand forwarding emerges as a critical mechanism to enhance pipeline efficiency and mitigate stalls caused by data hazards. [5 marks]