Reg. No.:

Name :

VIT

Vellore Institute of Technology

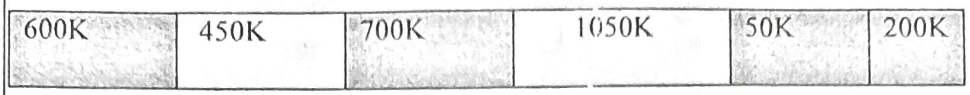
(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test II – October 2023

Programme	:	**B.Tech. CSE** **B.Tech. CSE (AI&ML)** **B.Tech. CSE (CPS)** **B.Tech. CSE (AIR)**	Semester	**Fall 2023-24**
Course Code	:	**BCSE303L**	Class Nbr(s)	**CH2023240100694** **CH2023240100695**
Course Title	:	**Operating Systems**		
Faculty(s)	:	**Dr. K. Vallidevi** **Dr. Afruza Begam**	Slot	**F1+TF1**
Time	:	**90 Minutes**	Max. Marks	**50**

Answer all the Questions

Q. No.	Sub-division	Question Text	Marks
1.	A	If an instruction has ' i ' microsecond access time, with a page fault it takes an additional ' j ' microsecond. Calculate the effective instruction time in the demand paging environment assuming a page fault occurs an average of k instruction.	4
	B	Consider a demand page system, that supports a memory access time is 100ns, and a page fault service time is 8ms if an empty page is available or a replacement page is clean, otherwise if the replace page is modified then it takes 20ms of time for service the page fault. What page fault is required to achieve an effective memory access time of 200ns assuming replace page is modified by 27% 0f the time.	6
2.		Write pseudocode or describe the logic for implementing the strict alternation protocol for the four processes (P1, P2, P3, and P4). Ensure that the processes follow the order P1, P2, P3, P4, P1, P2, and so on.	10

3.	A	Consider the following memory map. Blank partitions (450K, 1050K) are free and shaded (600K, 700K, 50K and 200K) partitions are used.  If requests from processes in the given order 900K, 75K, 375K, and 150K. Which of the following partition allocation schemes can satisfy the above requests (Assuming no compaction and Variable partition)? A) Best fit and First fit. B) Only First Fit C) Both First fit and Best fit. D) First fit and Worst fit. E) Only Worst Fit	4 6
	B	Consider you have a machine that supports a logical address of 32bit, page size 4KB. When a process starts, the page table is copied from memory to hardware at a rate of one entry per 50ns. If the process runs for 90ns of time then i). What % of process time is spent on coping the page table (PT)? ii. If PT entry is 64 bit what is the PT size in Byte? Write the answer with a proper explanation.	
4.		Consider that you are developing a chat application that allows multiple users to exchange messages in real-time. Each user is represented by a separate process, and you want to implement a shared memory-based IPC mechanism to facilitate message exchange between these processes. How would you design an IPC system using shared memory to enable real-time message exchange between multiple user processes in the chat application? Describe the key components and synchronization techniques you would use to ensure that messages are sent and received correctly between the processes while avoiding potential issues such as race conditions or data corruption. Write a C program using IPC Technique for the same application to be built.	10
5.		How can five philosophers efficiently share: i) five forks and 5 plate of noodles are available where two forks are needed for each philosopher; ii) two straws and 5 glasses of juice are available where one straw is needed for each philosopher. Ensure each philosopher can alternate between thinking, eating OR drinking without encountering a deadlock or resource contention issue? Write a pseudocode to explain the above scenario.	10

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