Reg. Number:	22BAI1266

VIT
Vellore Institute of Technology
CHENNAI

Continuous Assessment Test (CAT) – I - FEB 2024

Programme	:	B.Tech CSE & B.Tech CSE all Specializations	Semester	:	Winter Sem 23-24
Course Code & Course Title	:	BCSE205L/CSE2001 and Computer Architecture and Organization	Class Number	:	CH2023240501631/ CH2023240501635/ CH2023240501642/ CH2023240503352
Faculty	:	Dr.Monica/ Dr.Vaidehi/Prof.Nivedita/ Dr.Thanikachalam	Slot	:	F1+TF1
Duration	:	90 Minutes	Max. Mark		50 Marks

Answer all questions

Q. No	Sub Sec.	Description	Marks
1.		LDA 2000 SUB R1 STA 4000 For the above instructions, elaborate the working of von Neumann architecture along with the values of all the registers used. Sketch a neat structure of IAS computer.	10
2.	a)	Sketch an operational system using the functional components including a simple connecting path. Explain the operational flow with an example. [5 marks]	10
	b)	Design a new processor to perform mathematical operations at a high speed. Elucidate your architectural design. [5 marks]	
3.		Design an algorithm by sketching the flowchart for non-restoring division and check the working of it with the following numbers $32_{10} \div 5_{10}$. Find the decimal equivalent of the content of the accumulator at the end of the third iteration.	10
4.		Perform the following Floating-point operation on the numbers $156.625_{10} + 50.2_{10}$ i. Convert the above decimal numbers to normalized notation of binary format. (4 Marks) ii. Perform addition for the given numbers and write the normalized result in IEEE single precision format. (6 Marks)	10
5.		Consider the following expression, Z = (A+B-C) / ((D+E)*F). Write the assembly language code for the expression Z using 3-address, 2 address, 1-address and 0-address instruction formats.	10