

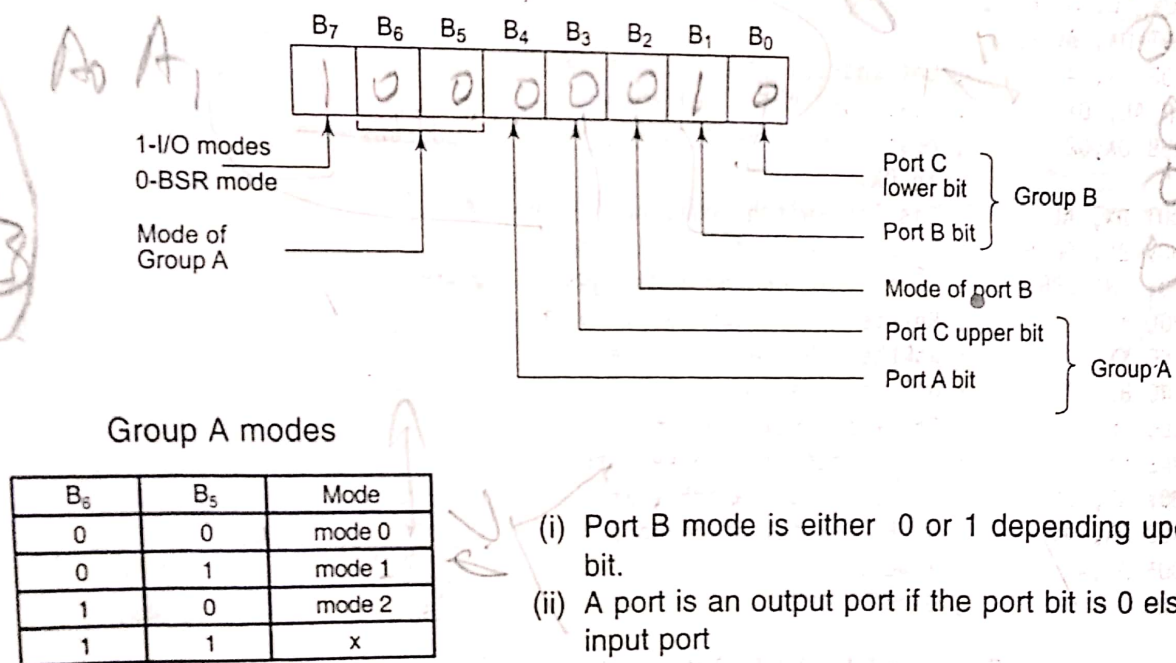
**Problem 5.10**

Interface an 8255 with 8086 to work as an I/O port. Initialize port A as output port, port B as input port and port C as output port. Port A address should be 0740H. Write a program to sense switch positions SW<sub>0</sub>-SW<sub>7</sub> connected at port B. The sensed pattern is to be displayed on port A, to which 8 LEDs are connected, while the port C lower displays number of on switches out of the total eight switches.

**Solution** The control word is decided upon as follows:

B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	Control word
1	0	0	0	0	0	1	0	= 82H
I/O	Port A		Port	Port	Port	Port	Port	
mode	in mode 0		A,o/p	C,o/p	B,mode 0	B,i/p	C,o/p	

Thus 82H is the control word for the requirements in the problem. The port address decoding can be done as given below. The 8255 is to be interfaced with lower order data bus, i.e. D<sub>0</sub>-D<sub>7</sub>. The A<sub>0</sub> and A<sub>1</sub> pins of 8255 are connected to A<sub>01</sub> and A<sub>02</sub> pins of the microprocessor respectively. The A<sub>00</sub> pin of the microprocessor is used for selecting the transfer on the lower byte of the data bus. Hence any change in the status of A<sub>00</sub> does not affect the port to be selected, rather A<sub>01</sub> and A<sub>02</sub> of the microprocessor decide the port to be selected as they are connected to A<sub>0</sub> and A<sub>1</sub> of 8255. The 8255 port addresses are tabulated as shown below.



**Fig. 5.18(b)** I/O Mode Control Word Register Format

8255 Ports	I/O Address lines																Hex. Port Addresses
	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>	A <sub>11</sub>	A <sub>10</sub>	A <sub>09</sub>	A <sub>08</sub>	A <sub>07</sub>	A <sub>06</sub>	A <sub>05</sub>	A <sub>04</sub>	A <sub>03</sub>	A <sub>02</sub>	A <sub>01</sub>	A <sub>00</sub>	
Port A	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0740H
Port B	0	0	0	0	0	1	1	1	0	1	0	0	0	0	1	0	0742H

(Contd.)



(Contd.)																	Hex. Port Addresses
8255	I/O Address lines																
Ports	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>	A <sub>11</sub>	A <sub>10</sub>	A <sub>09</sub>	A <sub>08</sub>	A <sub>07</sub>	A <sub>06</sub>	A <sub>05</sub>	A <sub>04</sub>	A <sub>03</sub>	A <sub>02</sub>	A <sub>01</sub>	A <sub>00</sub>	
Port C	0	0	0	0	0	1	1	1	0	1	0	0	0	1	0	0	0744H
CWR	0	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	0746H

Let us use absolute decoding scheme that uses all the 16 address lines for deriving the device address pulse. Out of A<sub>0</sub> – A<sub>15</sub> lines, two address lines A<sub>02</sub> and A<sub>01</sub> are directly required by 8255 for the three port and CWR address decoding. Hence only A<sub>3</sub> to A<sub>15</sub> are used for decoding addresses. The complete hardware scheme is shown in Fig. 5.19. In the diagram, the 8086 is assumed to be in the maximum mode so that  $\overline{\text{IOR}}\overline{\text{D}}$  and  $\overline{\text{IOWR}}$  are readily available. If the 8086 is in minimum mode,  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  of 8086 are to be connected accordingly to 8255 and  $\text{M}/\overline{\text{IO}}$  pin is combined with the chip select of above hardware suitably so as to select the 8255 when  $\text{M}/\overline{\text{IO}}$  is low.

The ALP for the problem is developed as follows:

```

MOV DX, 0746 H ; Initialise CWR with
MOV AL, 82 H   ; control word 82H
OUT DX, AL
SUB DX, 04     ; Get address of port B in DX
IN AL, DX     ; Read port B for switch
SUB DX, 02     ; positions in to AL and get port A address
               ; in DX.
OUT DX, AL    ; Display switch positions on port A
MOV BL, 00 H  ; Initialise BL for switch count
MOV CH, 08H   ; Initialise CH for total switch number
YY: ROL AL    ; Rotate AL through carry to check,
JNC XX        ; whether the switches are on or
INC BL       ; off, i.e. either 1 or 0
XX: DEC CH   ; Check for next switch. If
JNZ YY       ; all switch are checked, the
MOV AL, BL   ; number of on switches are
ADD DX, 04   ; in BL. Display it on port C
OUT DX, AL   ; lower.
HLT          ; Stop

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Program 5.5 ALP for Problem 5.10

### Problem 5.11

Interface a 4\*4 Keyboard with 8086 using 8255. and write an ALP for detecting a key closure and return the key code in AL. The debouncing period for a key is 10 ms. Use software key debouncing technique. DEBOUNCE is an available 10 ms delay routine.

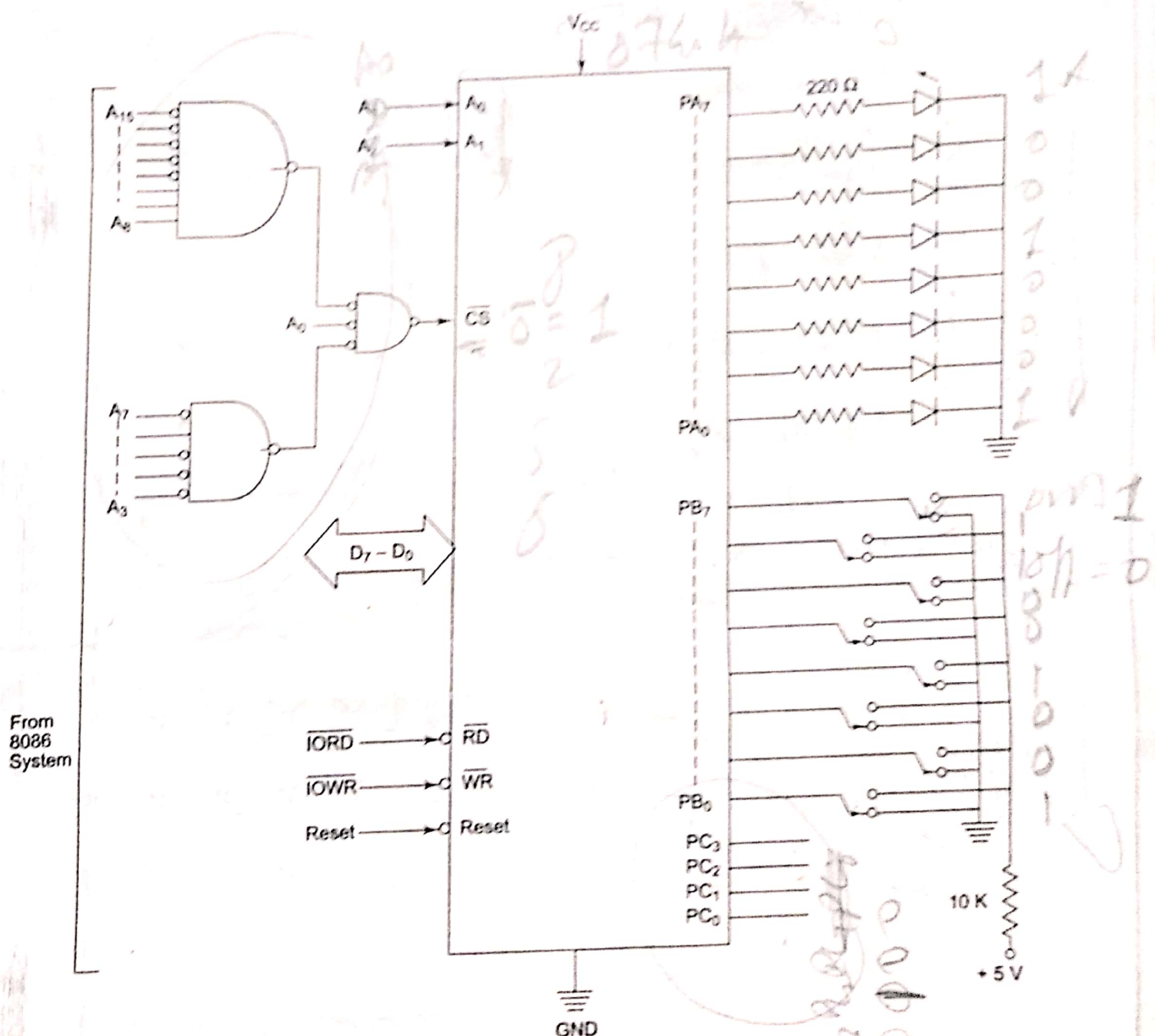


Fig. 5.19 8255 Interfacing with 8086 for Problem 5.10

**Solution** Port A is used as output port for selecting a row of keys while port B is used as an input port for sensing a closed key. Thus the keyboard lines are selected one by one through port A and the port B lines are polled continuously till a key closure is sensed. Then routine DEBOUNCE is called for key debouncing. The key code is decided depending upon the selected row and a low sensed column. The hardware circuit diagram is shown in Fig. 5.21.



- 0.1 BIOS INT 10H PROGRAMMING
- 4.2 DOS INTERRUPT 21H
- 6.1 SIGNAL AND ARITHMETIC OPERATION
- 6.2 STRING AND TABLE OPERATION
- 14.1 8088/86 INTERRUPTS
- 14.2 X86 PC AND INTERRUPTS ASSIGNMENT
- 14.4 PROGRAMMING AND INTERPRETING THE

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