Digital VLSI Final Project Report

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1. Introduction

In this project, a simple microcontroller core has been designed which is a 8 bit accumulator core with 3 bit opcode and 6bit instruction word which performs all the functions at a higher speed. The microcontroller layout and schematic has been designed using Cadence Virtuoso software. The microcontroller is designed with the help of different blocks which has individual functionality. The datacore of the processor is as shown in the fig 1.

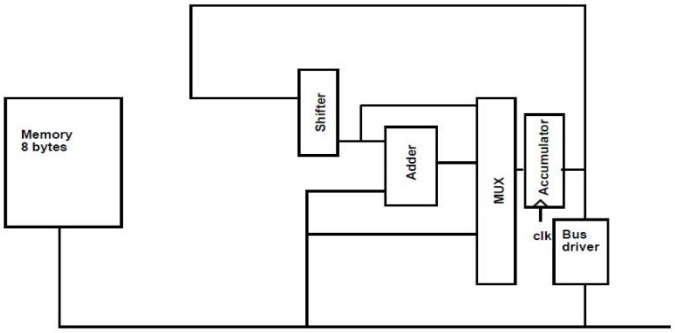


Fig 1. Datacore of the circuit.

Each block has been implemented and tested separately for higher speed and higher performance. The schematic of the circuit is designed using virtuoso and is shown in Fig 2.

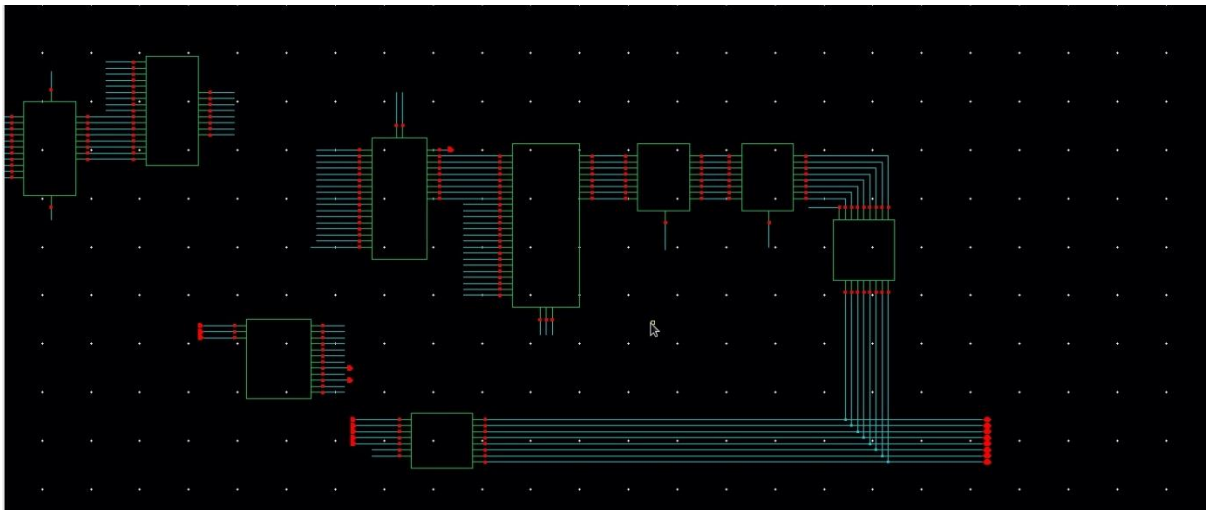


Fig 2. Schematic of the final circuit

The blocks used in this circuit are 8-bit Full adder, 8-bit Shifter, PLA(Decoder) , 8-bit 3*1 Multiplexer, SRAM, Accumulator(8 - bit latch) and Bus driver. Each blocks has been designed keeping in mind the power estimate, size and speed of the final microcontroller.

2. Functionality

Full Adder

First an 8-bit Full adder has been designed and tested using cadence. Depending on the subtract pin, the circuit adds or subtracts two 8- bit data. If subtract is 0, it performs addition and if subtract is 1, then it performs subtraction. The layout and schematic of the circuit is as shown in fig3.

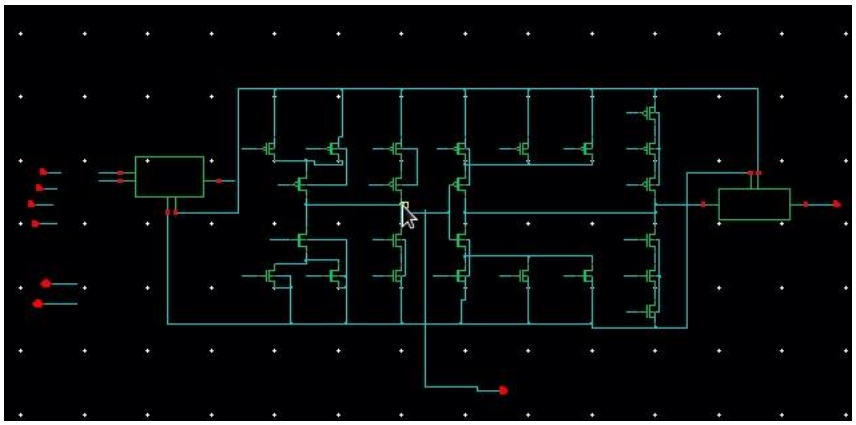


Fig 3. Schematic of 1 bit full adder

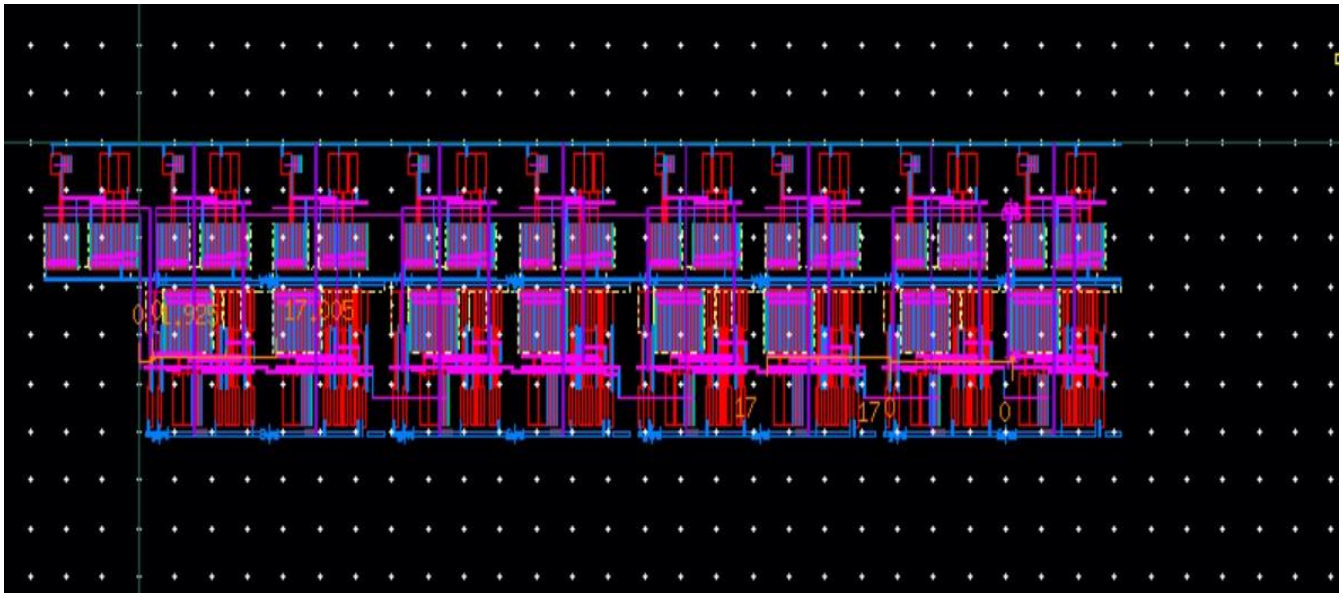


Fig 4. Layout of 8- bit Full Adder

Shifter

Then a 8 bit shifter is designed and using a select pin, left shift operation is performed on the 8-bit input data. The schematic and layout of the 8-bit shifter is as shown in the fig below.

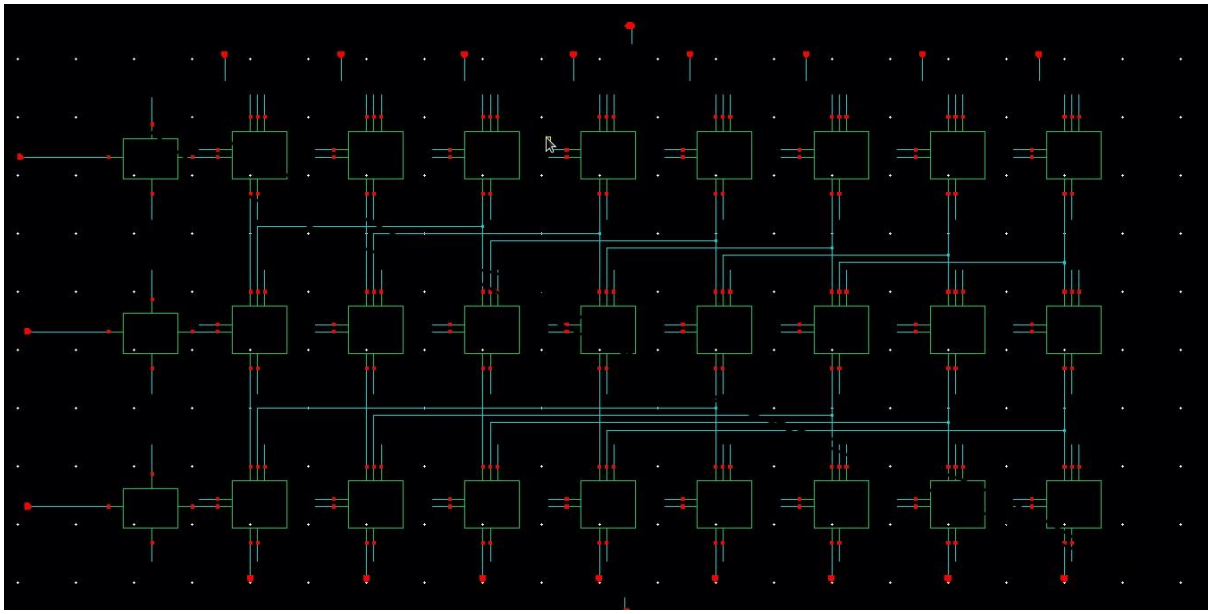


Fig 5. Schematic of 8-bit shifter

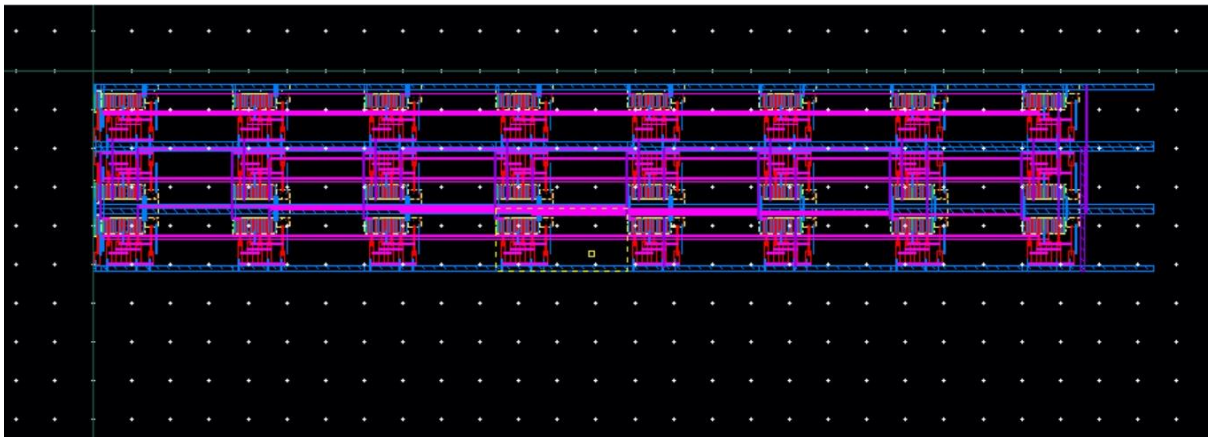


Fig 6. Layout of 8-bit shifter

Accumulator

A 8-bitlatch has been implemented, which on the basis of clock signal, gives the desired output. If clk is 1 then entire input data is obtained at the output. The layout of the circuit is as shown in the fig below.

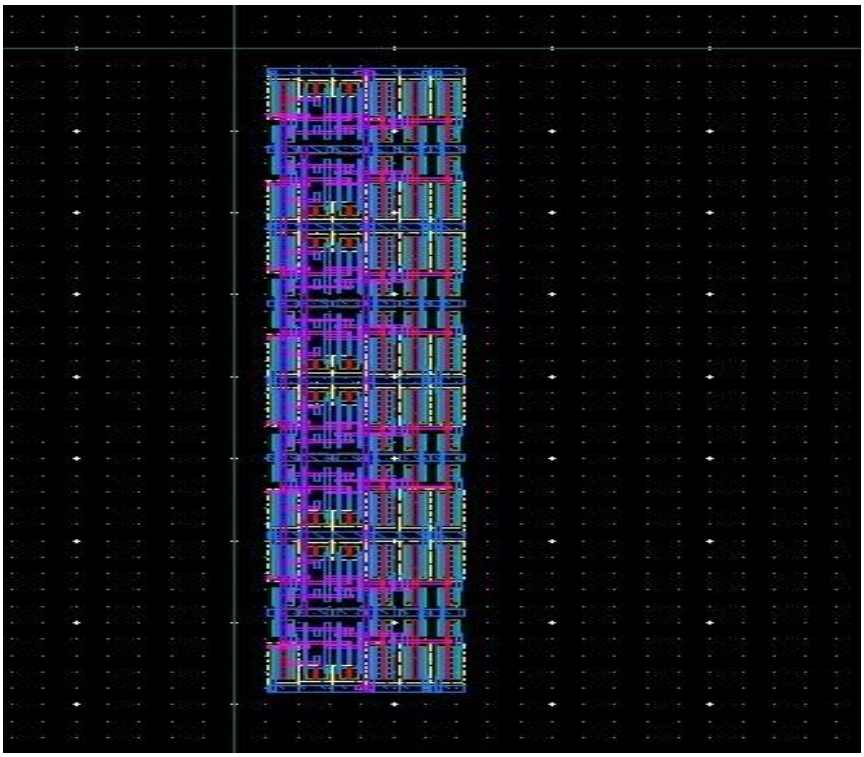


Fig 7. Layout of accumulator

SRAM cell

SRAM is one of the most important blocks in the microcontroller circuit. SRAM cell has been designed and implemented using cadence. The schematic and layout of SRAM circuit is shown in fig below. First using write signal , a 8-bit input data is stored in SRAM and then using read signal the stored data can be accessed. The entire SRAM circuit is designed with sized schematics and keeping area and power constraint in consideration.

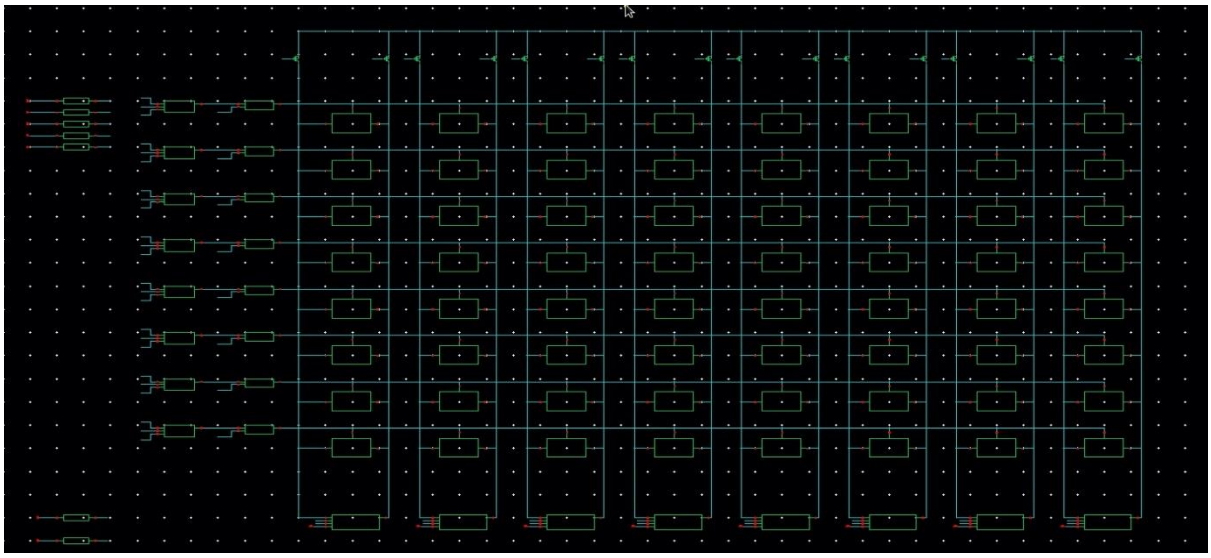


Fig 8. Schematic of SRAM block

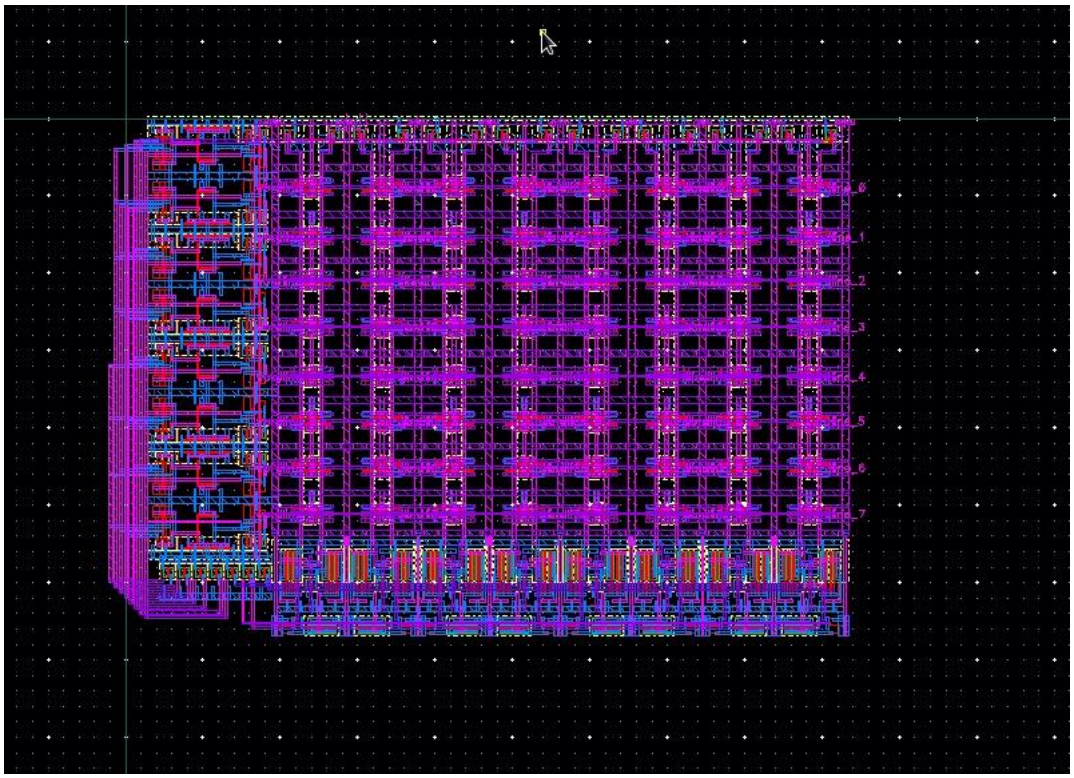


Fig 9. Layout of SRAM cell

Multiplexer

A 8 bit 3*1 MUX has been designed and tested. It determines which operation to be performed i.e. addition/subtraction or shift depending on the 3-bit enable signal. The schematic and layout of the circuit is as shown in fig below.

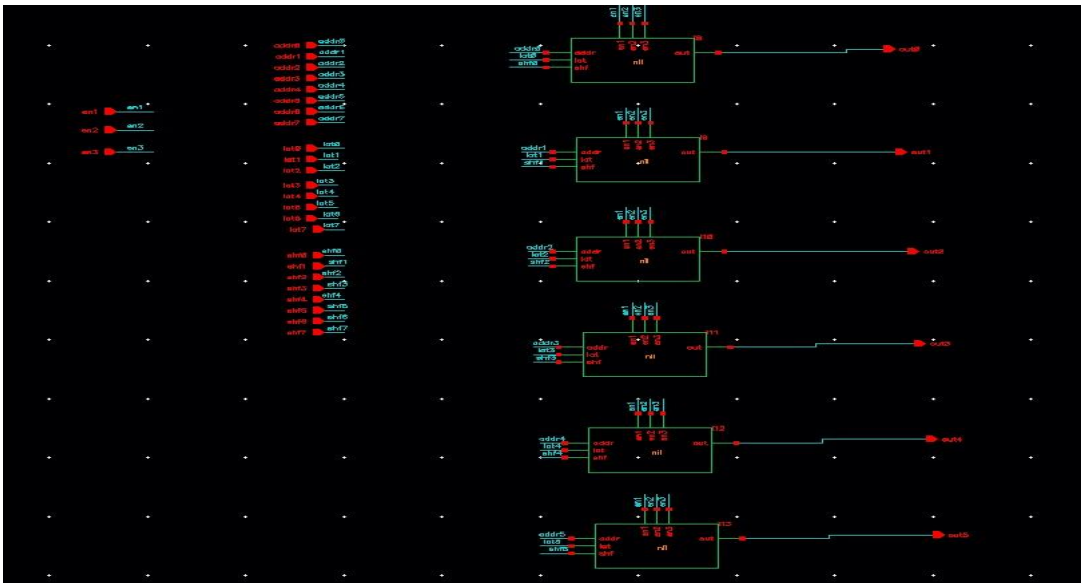


Fig 10. Schematic of multiplexer

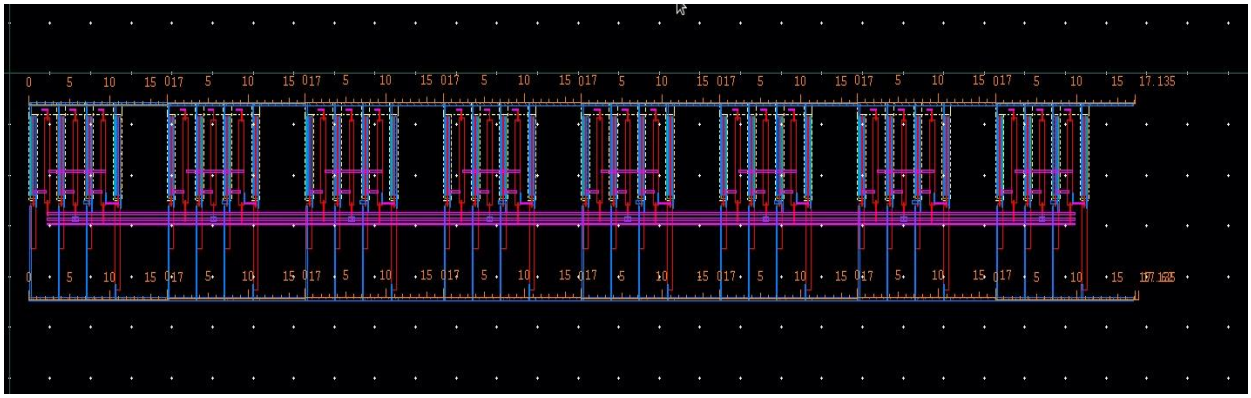


Fig 11. Layout of the multiplexer block

Tristate Buffer (Bus driver)

Tristate buffers are essential to the operation of the microprocessor as it functions as a shared electronic bus. Bus driver schematic and layout has been implemented and has been tested. Both the schematic and layout of the circuit Is shown below

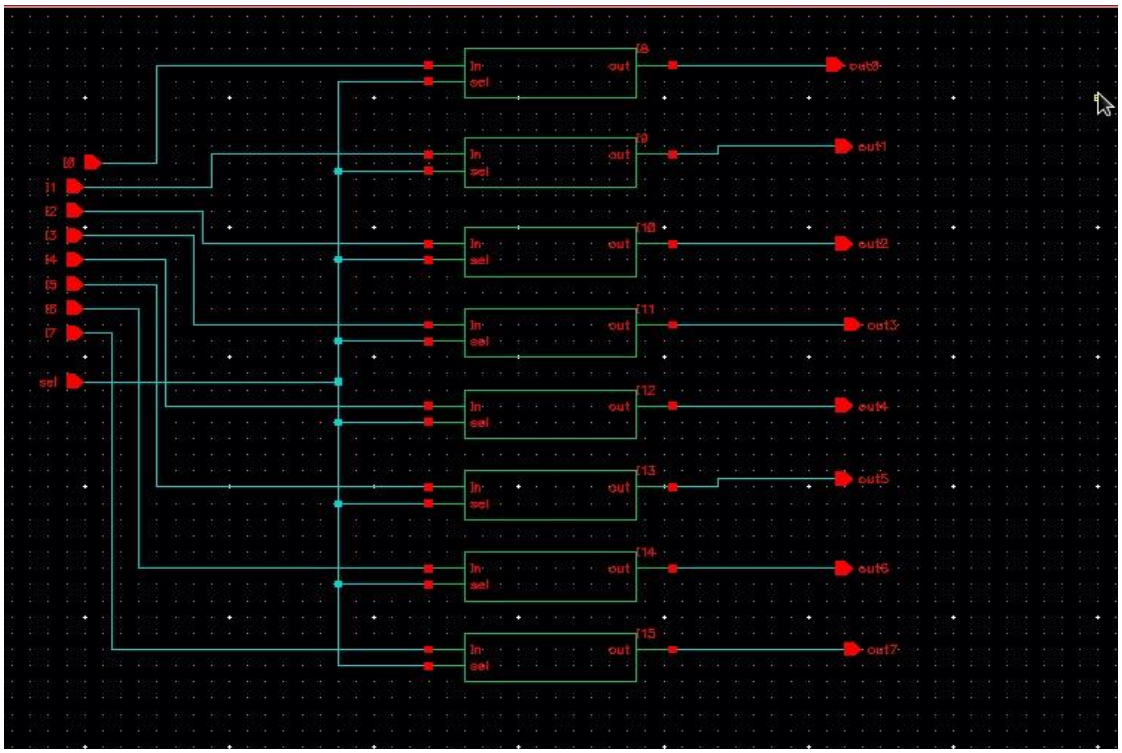


Fig 12. Schematic of tristate buffer

When select pin is high, output becomes the 8-bit input data. When select pin is low it gives high impedance. The functionality of the circuit has been tested using ADE environment in cadence virtuoso.

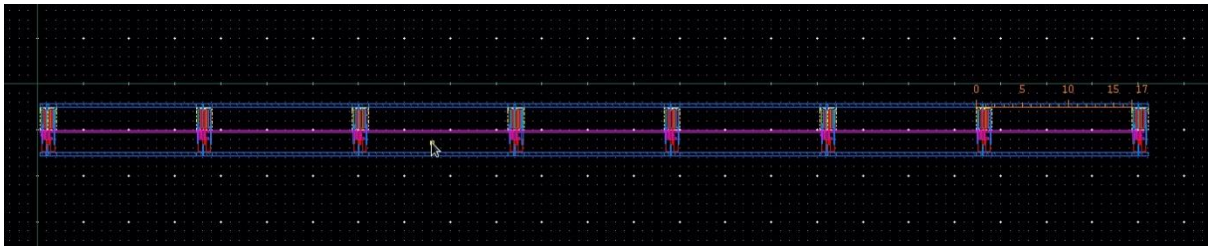


Fig 13. Layout of tristate buffer

Decoder(PLA)

A decoder circuit has been implemented and tested. The functionality of the decoder circuit is as per the table below

Opcode	Load	Store	Sub	Write	Read	Shift(Ms)	Add(Ma)	Bus(Mb)	Enable	Bypass shifter
0 0 0	0	0	X	0	X	1	0	0	X	1
0 0 1	1	0	X	1	0	1	0	0	0	1
0 1 0	0	1	X	0	1	1	0	0	0	1
0 1 1	0	0	X	0	1	0	0	1	0	X
1 0 0	0	0	X	1	0	0	0	1	1	X
1 0 1	0	0	0	0	1	0	1	0	0	1
1 1 0	0	0	1	0	1	0	1	0	1	1
1 1 1	0	0	X	0	X	1	0	0	X	0

The 3-bit opcode determines which operation to be performed. The PLA we designed is based on this operation of opcode.

Opcode	Operation
0 0 0	Normal
0 0 1	Load
0 1 1	Get
1 0 0	Put
1 0 1	Addition
1 1 0	Subtraction
1 1 1	Logical left shift

We designed the decoder according to this functionality and it has been tested. The schematic and layout of the decoder is as shown in fig below.

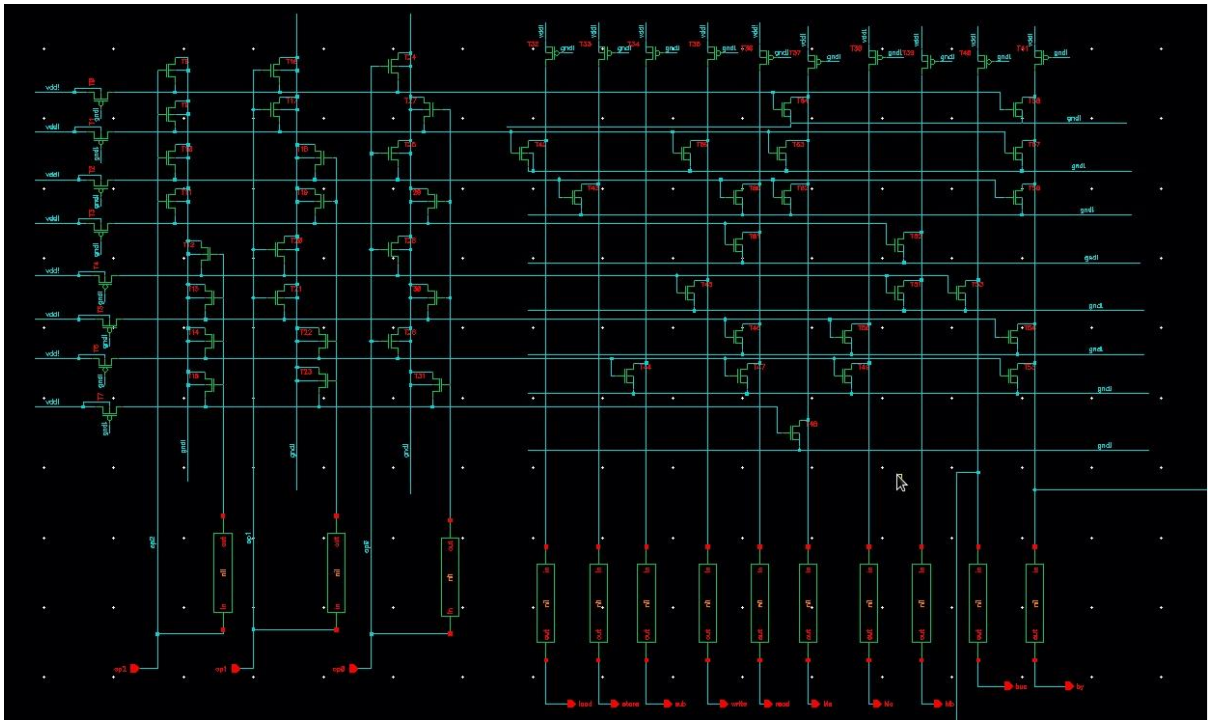


Fig 14. Layout of PLA(Decoder)

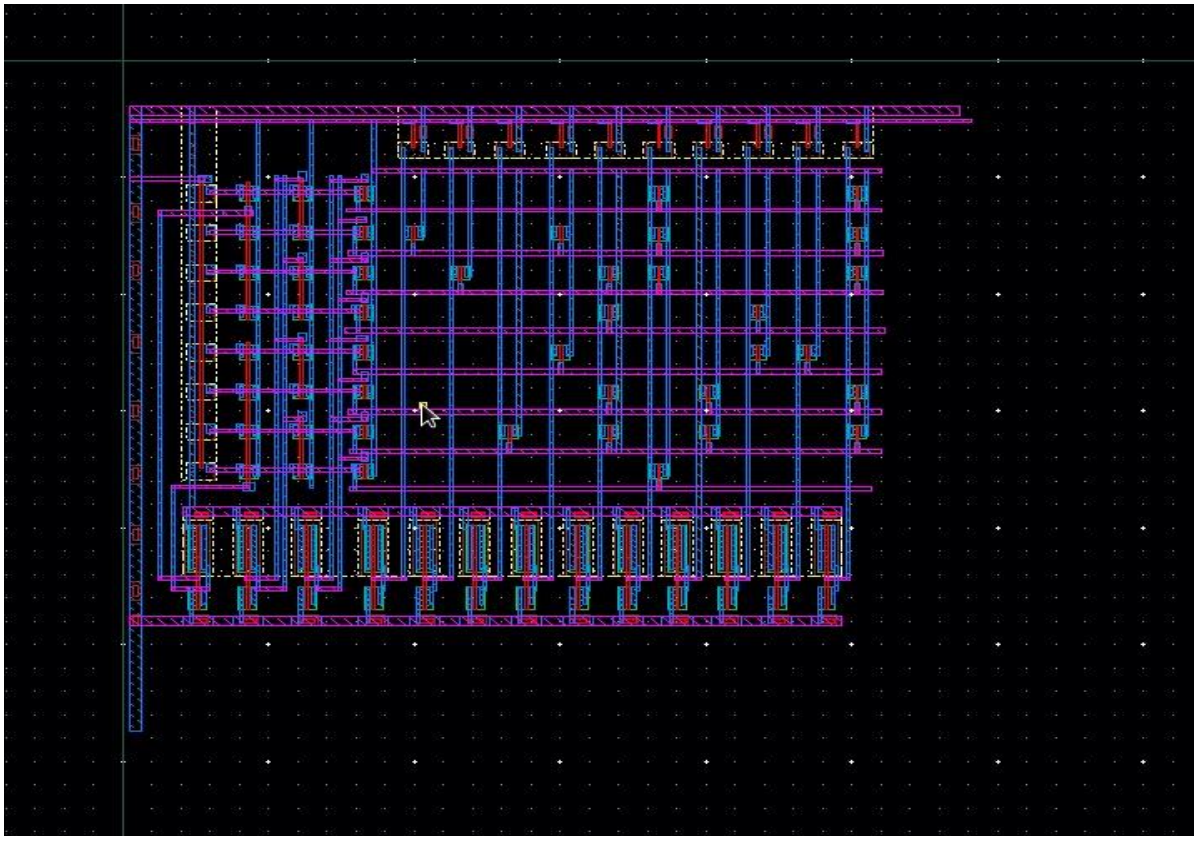


Fig 15. Layout of the decoder circuit

3. Operation and testing

Using all the blocks, we designed the final circuit of the microcontroller core which performs all the functions specified. Layout hierarchy as well as the bit pitch has been taken care of so as to make the performance of the microcontroller better. The schematic of the circuit has been designed according to the block diagram shown in fig 1. The schematic of the circuit has been implemented using cadence and is shown below.

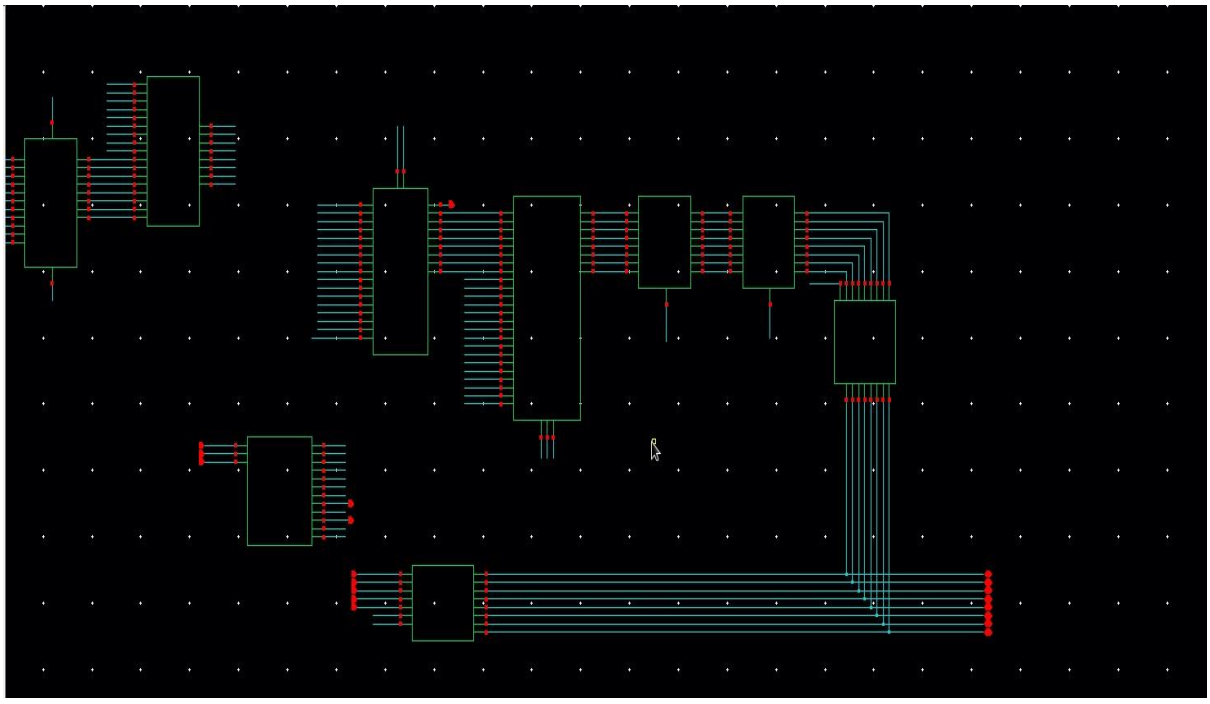
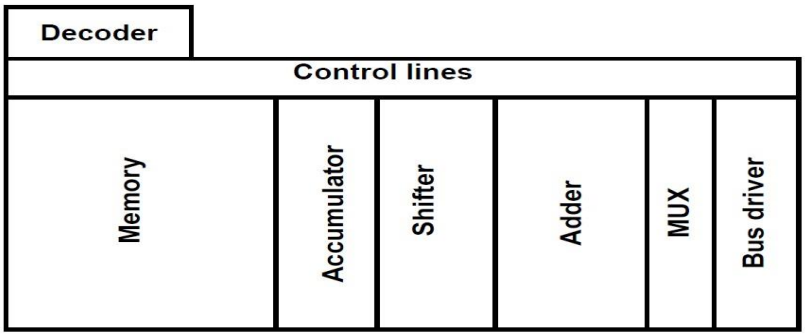


Fig 16. Schematic of the microcontroller core

First input data is written on to the memory of the microcontroller using 001 opcode(write). Then it is read using get command. Using addition command, the new input data is added with the data that is already stored in the memory. Also in the design we have given an overflow output pin which shows whether overflow occurs or not while performing addition. Using shift command(opcode 111), the entire input data is shifted to the left by one bit.

The circuit is tested for all possible combinations of input using ADE environment of virtuoso and the functionality of microcontroller core has been verified. The floorplan of the layout implemented is as shown



The layout of the microcontroller is done by combining all the individual blocks according to the floorplan discussed above. Care has been taken regarding the overall size of core so as to increase the performance and speed of the microcontroller.

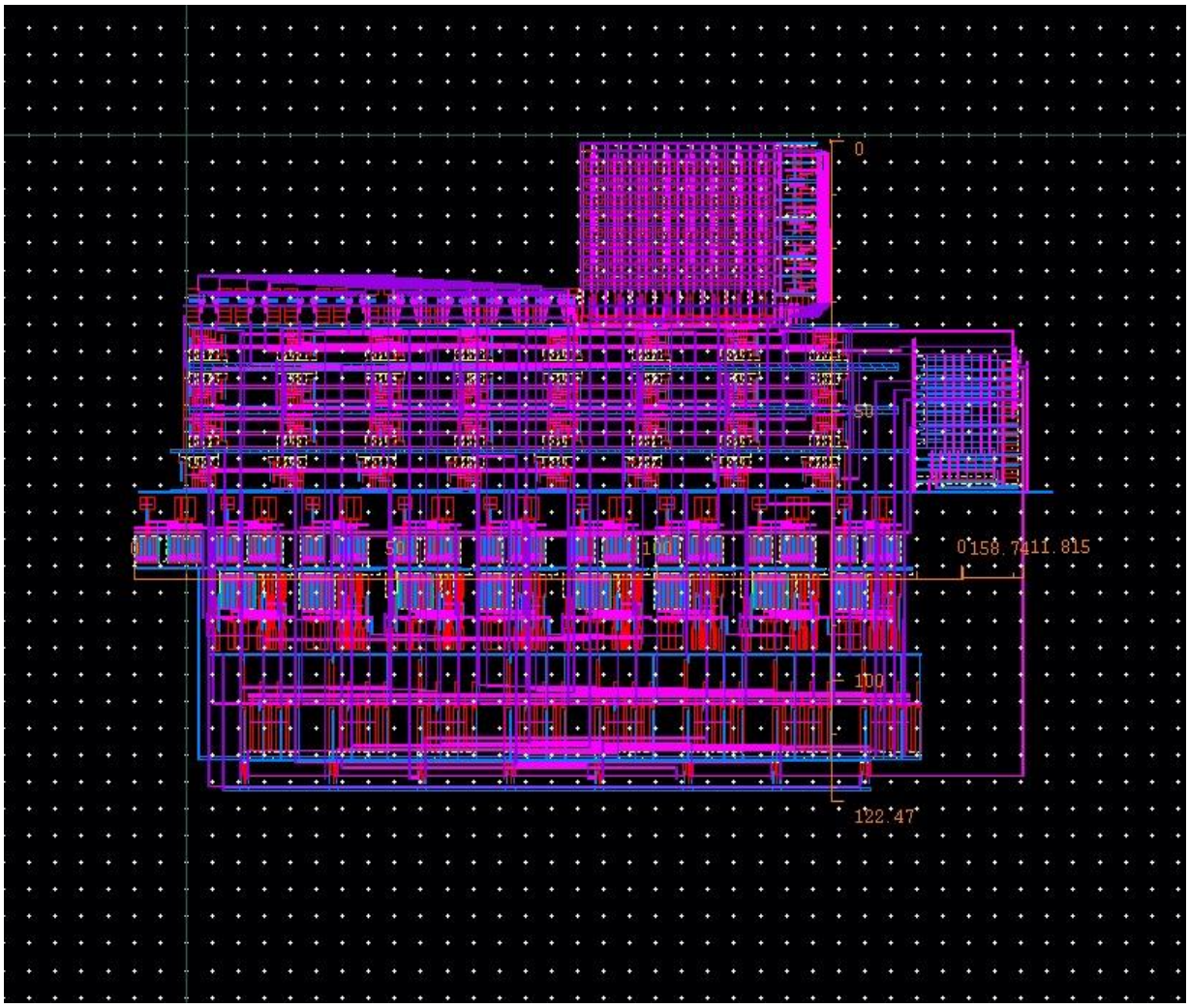


Fig 17. Layout of the microcontroller core

The test circuitry of this microcontroller core is implemented and it has been tested for all the possible combinations of input. The test circuitry and the outputs are as shown in the fig below.

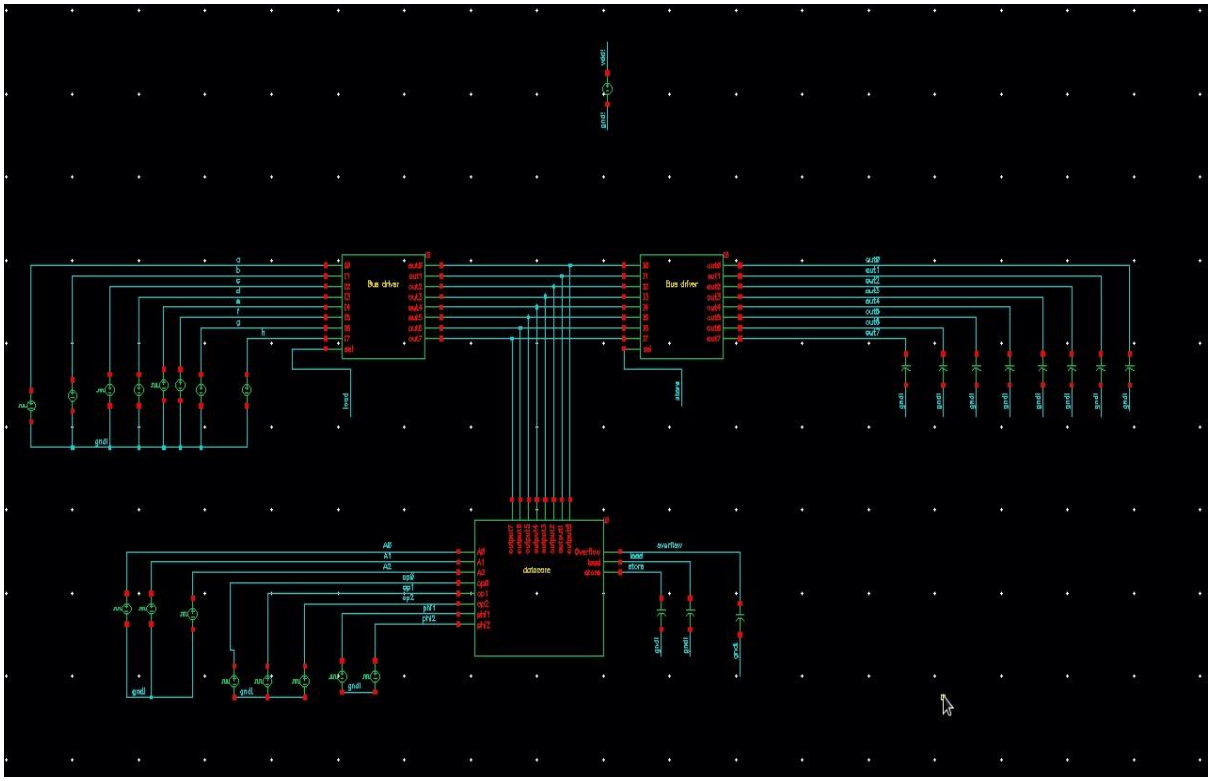


Fig 18. Test circuit of the microcontroller core

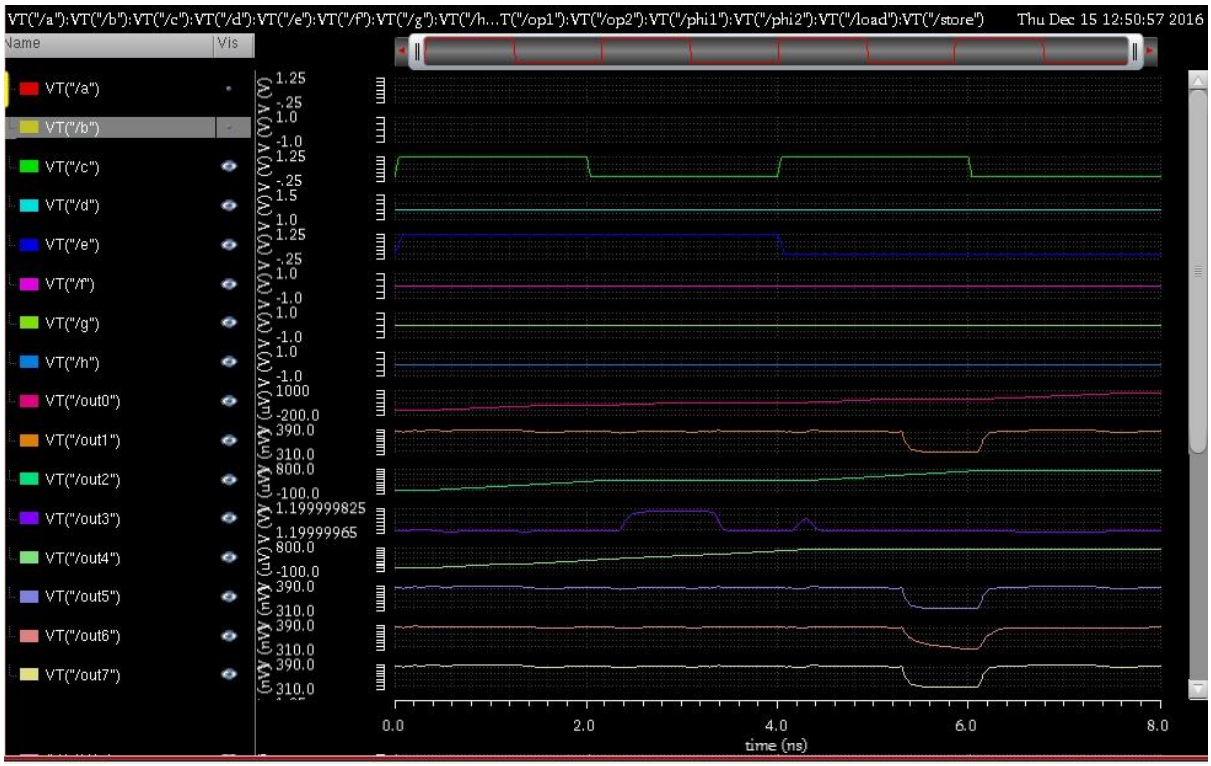


Fig 19. Output of the test circuit tested for 7ns

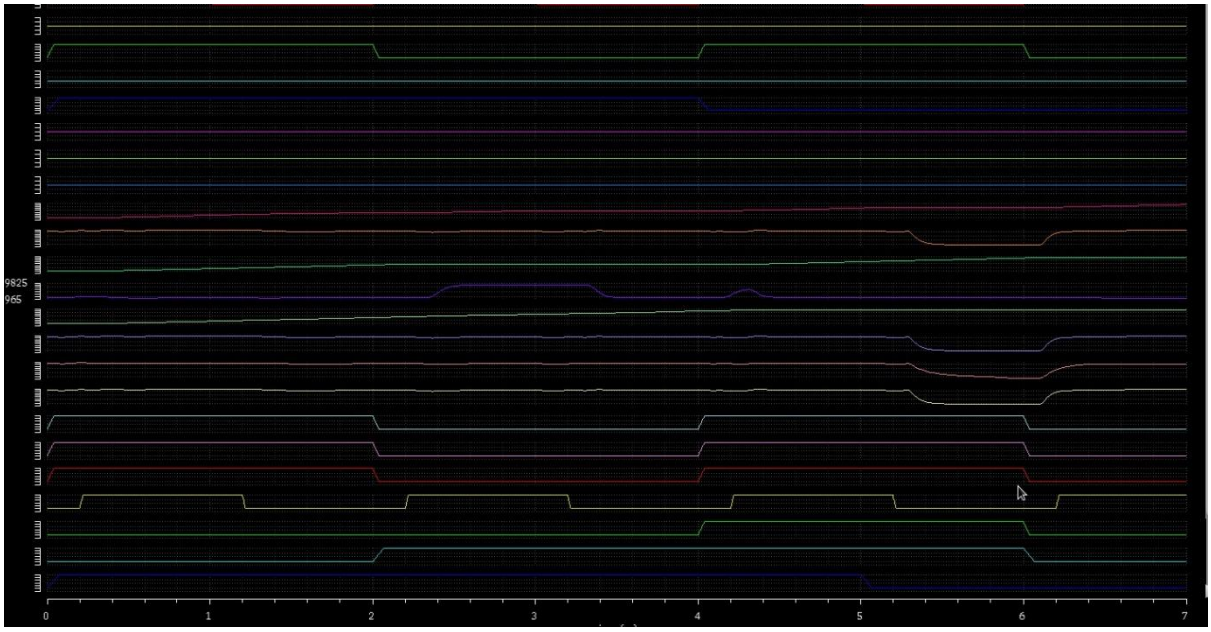


Fig 20. Output for the overflow condition

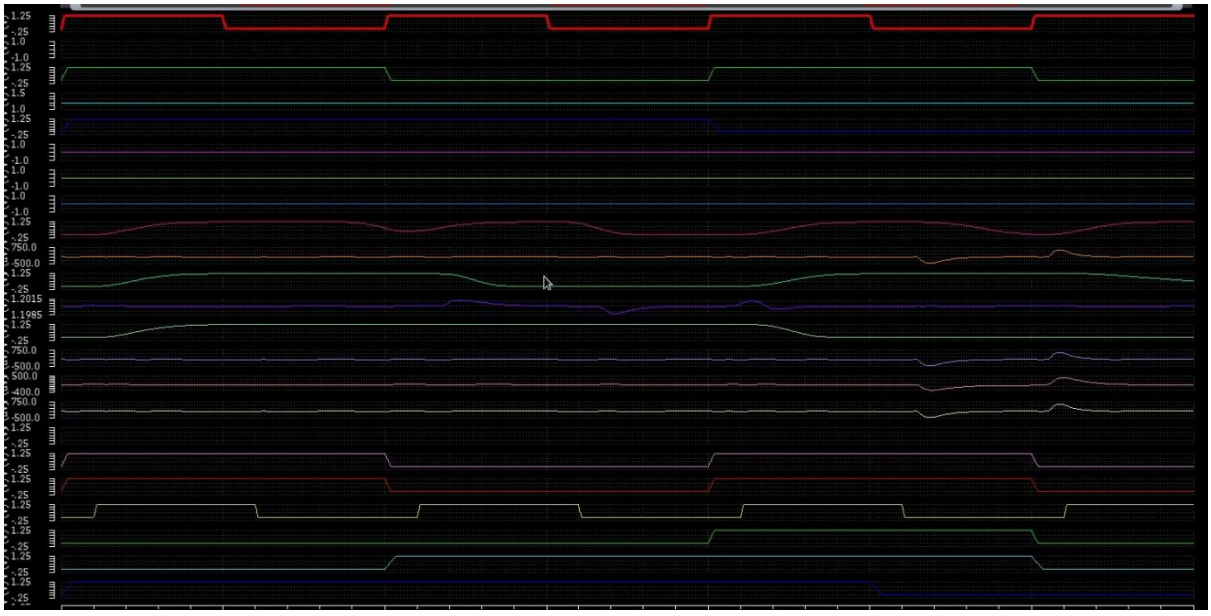


Fig 21. Output for shifter bypass

First we gave input 11010101 which was initially written into the memory when opcode was 001. When opcode becomes 011, it shows the same value because of the get condition. When opcode becomes 101, the current input 00010001 gets added to the already stored value and becomes 11100110 which is shown in fig 19. The same case has been tried for overflow condition by making the MSB for the current input 1 keeping everything same. And we get the overflow peak in 101 opcode as shown in fig 20. When opcode becomes 111, it operates in shift mode (left) and corresponding bits gets shifted to its left by one bit as given in fig 21. The circuit has been tested for different combinations of inputs and the results have been verified and found to be correct.

4. Conclusion

The circuit has been tested for all the possible combinations of input and the correct functionality of the microcontroller has been verified. The circuit has passed both DRC and LVS checks(clean). The results have been attached. The area of the layout is 20280um^2 (Length=169um and Width=120um). The correct operation of the circuit occurs at 7ns. The speed of the microcontroller core turns out to be 125 MHz.

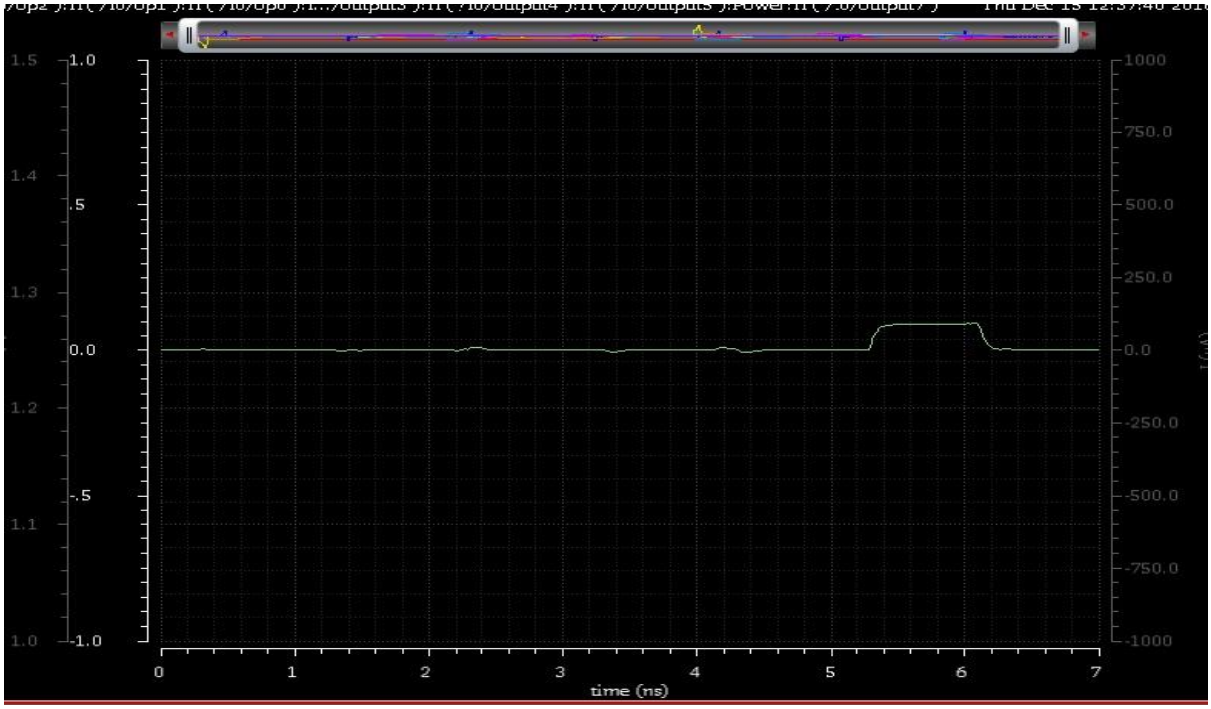


Fig 22. Determining the speed of the microcontroller

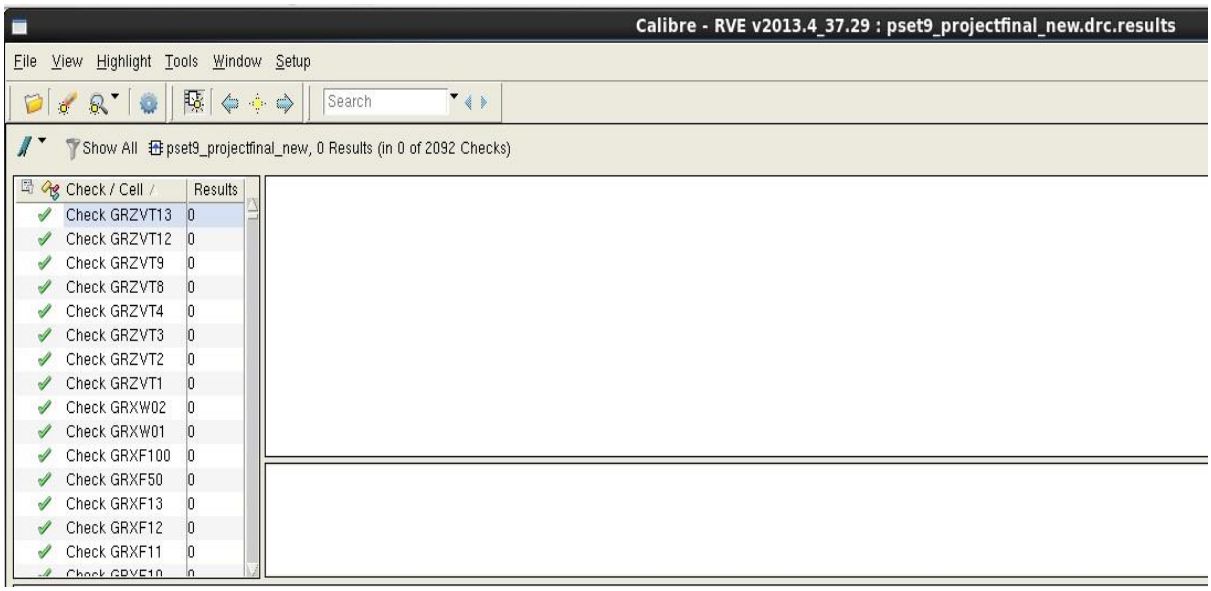


Fig 23. DRC Clean

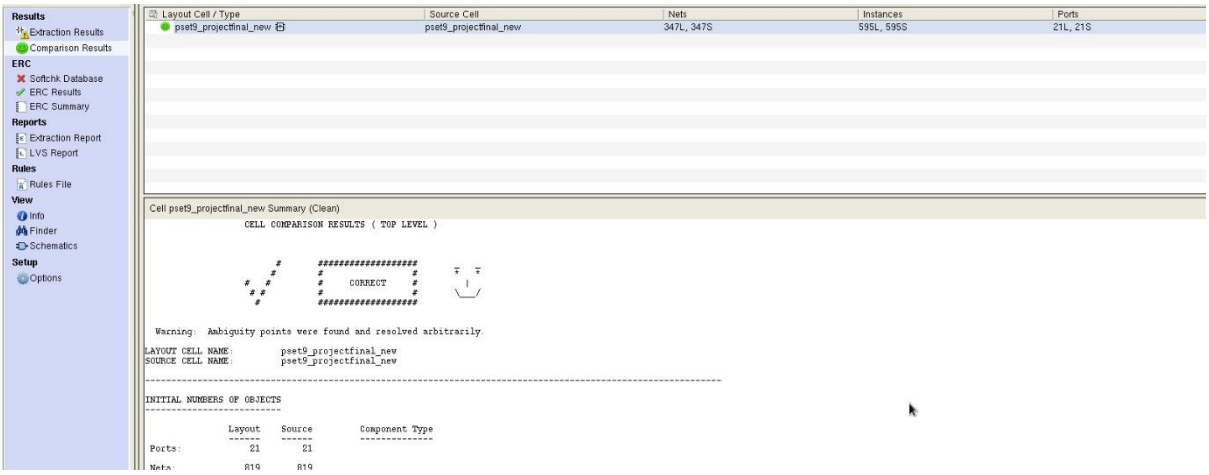


Fig 24. LVS Clean

The power is found out by measuring the current and integrating it with the Vdd voltage using the calculator over the operation time i.e 7ns in the ADE environment.

Power = 1/T $\int Vdd * Idd \ dt$

The power turns out to be 157mW.

In addition, the gds file was also submitted along with the report.