DW1000 IEEE802.15.4-2011 UWB Transceiver

Product Overview

The DW1000 is a fully integrated single chip Ultra Wideband (UWB) low-power low-cost transceiver IC compliant to IEEE802.15.4-2011. It can be used in 2-way ranging or TDOA location systems to locate assets to a precision of 10 cm. It also supports data transfer at rates up to 6.8 Mbps

Key Features

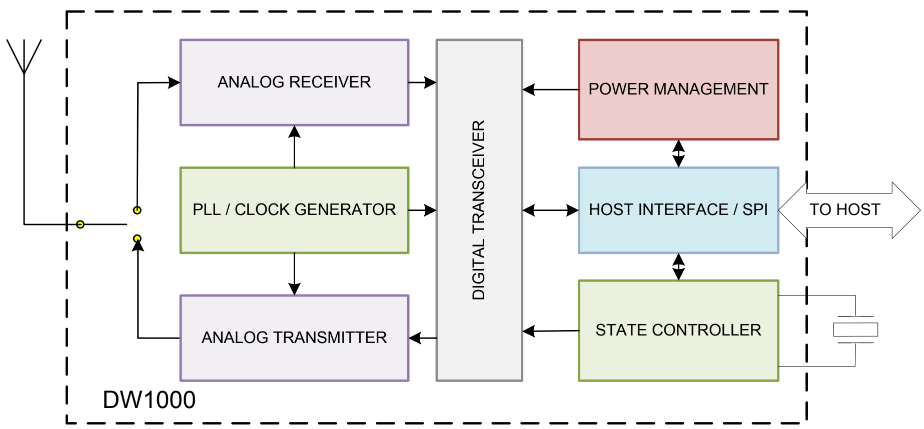
- IEEE802.15.4-2011 UWB compliant
- Supports 6 RF bands from 3.5 GHz to 6.5 GHz
- Programmable transmitter output power
- Fully coherent receiver for maximum range and accuracy
- Complies with FCC & ETSI UWB spectral masks
- Supply voltage 2.8 V to 3.6 V
- Low power consumption
- SLEEP mode current 2 uA
- DEEP SLEEP mode current 100 nA
- Data rates of 110 kbps, 850 kbps, 6.8 Mbps
- Maximum packet length of 1023 bytes for high data throughput applications
- Integrated MAC support features
- Supports 2-way ranging and TDOA
- SPI interface to host processor
- 6 mm x 6 mm 48-pin QFN package
- Small number of external components

Key Benefits

- Supports precision location and data transfer concurrently
- Asset location to a precision of 10 cm
- Extended communications range up to 290 m @ 110 kbps 10% PER minimises required infrastructure in RTLS
- High multipath fading immunity
- Density of > 11,000 tags in a 20 m radius NLOS
- Small PCB footprint allows cost-effective hardware implementations
- Long battery life minimises system lifetime cost

Applications

- Precision real time location systems (RTLS) using two-way ranging or TDOA schemes in a variety of markets: -
    - Healthcare
    - Consumer
    - Industrial
    - Other
- Location aware wireless sensor networks



High Level Block Diagram

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1 IC DESCRIPTION

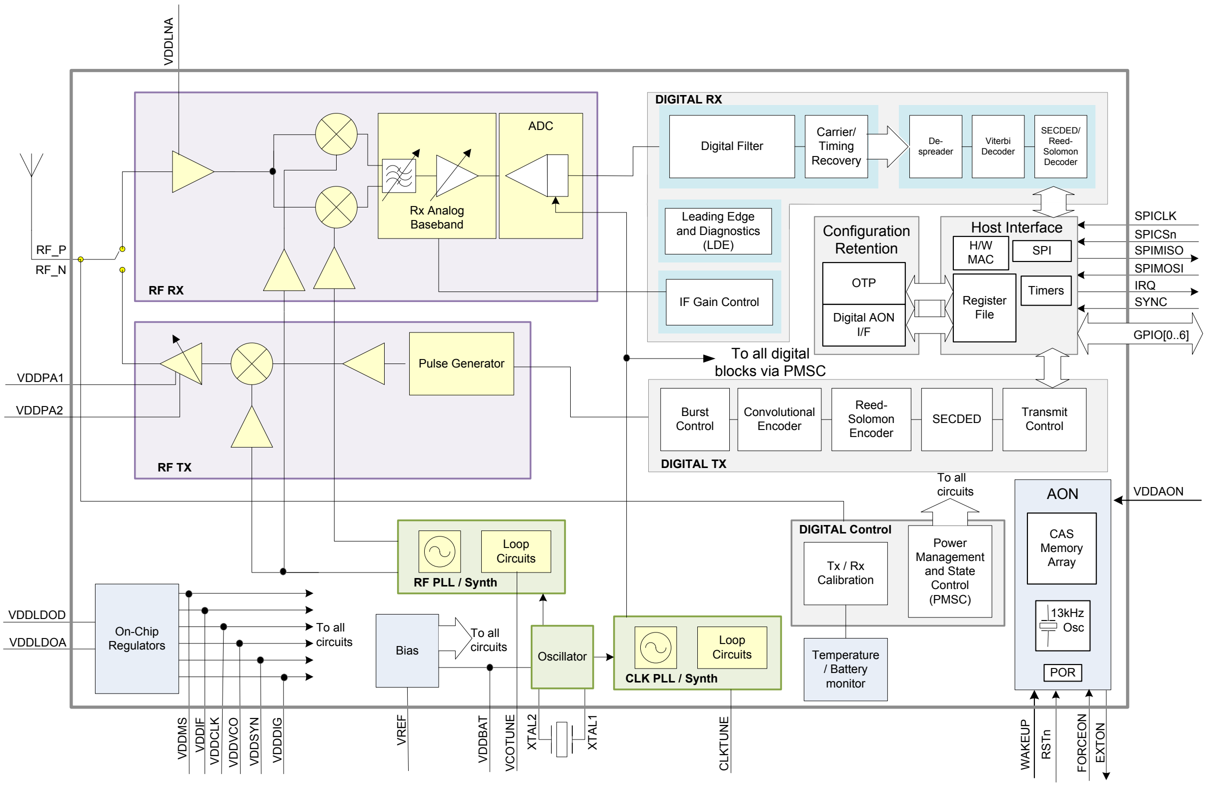


Figure 1: IC Block Diagram

DW1000 is a fully integrated low-power, single chip CMOS RF transceiver IC compliant with the IEEE802.15.4-2011 [1] UWB standard.

DW1000 consists of an analog front end containing a receiver and a transmitter and a digital back end that interfaces to an off-chip host processor. A TX/RX switch is used to connect the receiver or transmitter to the antenna port. Temperature and voltage monitors are provided on-chip

The receiver consists of an RF front end which amplifies the received signal in a low-noise amplifier before down-converting it directly to baseband. The receiver is optimized for wide bandwidth, linearity and noise figure. This allows each of the supported IEEE802.15.4-2011 [1] UWB channels to be down converted with minimum additional noise and distortion. The baseband signal is demodulated and the resulting received data is made available to the host controller via SPI.

The transmit pulse train is generated by applying digitally encoded transmit data to the analog pulse generator. The pulse train is up-converted by a double balanced mixer to a carrier generated by the synthesizer and centred on one of the permitted IEEE802.15.4-2011 [1] UWB channels. The modulated RF waveform is amplified before transmission from the external antenna.

The IC has an on-chip One-Time Programmable (OTP) memory. This memory can be used to store calibration data such as TX power level, crystal initial frequency error adjustment, and range accuracy adjustment. These adjustment values can be automatically retrieved when needed. See section 5.14 for more details.

The Always-On (AON) memory can be used to retain DW1000 configuration data during the lowest power operational states when the on-chip voltage regulators are disabled. This data is uploaded and downloaded automatically. Use of DW1000 AON memory is configurable.

The DW1000 clocking scheme is based around 3 main circuits; Crystal Oscillator, Clock PLL and RF PLL. The on-chip oscillator is designed to operate at a frequency of 38.4 MHz using an external crystal. An external 38.4 MHz clock signal may be applied in place of the crystal if an appropriately stable clock is available elsewhere in the user's system. This 38.4 MHz clock is used as the reference clock input to the two on-chip PLLs. The clock PLL (denoted CLKPLL) generates the clock required by the digital back end for signal processing. The RF PLL generates the down-conversion local oscillator (LO) for the receive chain and the up-conversion LO for the transmit chain. An internal 13 kHz oscillator is provided for use in the SLEEP state.

The host interface includes a slave-only SPI for device communications and configuration. A number of MAC features are implemented including CRC generation, CRC checking and receive frame filtering.

2 PIN CONNECTIONS

2.1 Pin Numbering

QFN-48 package with pin assignments as follows: -

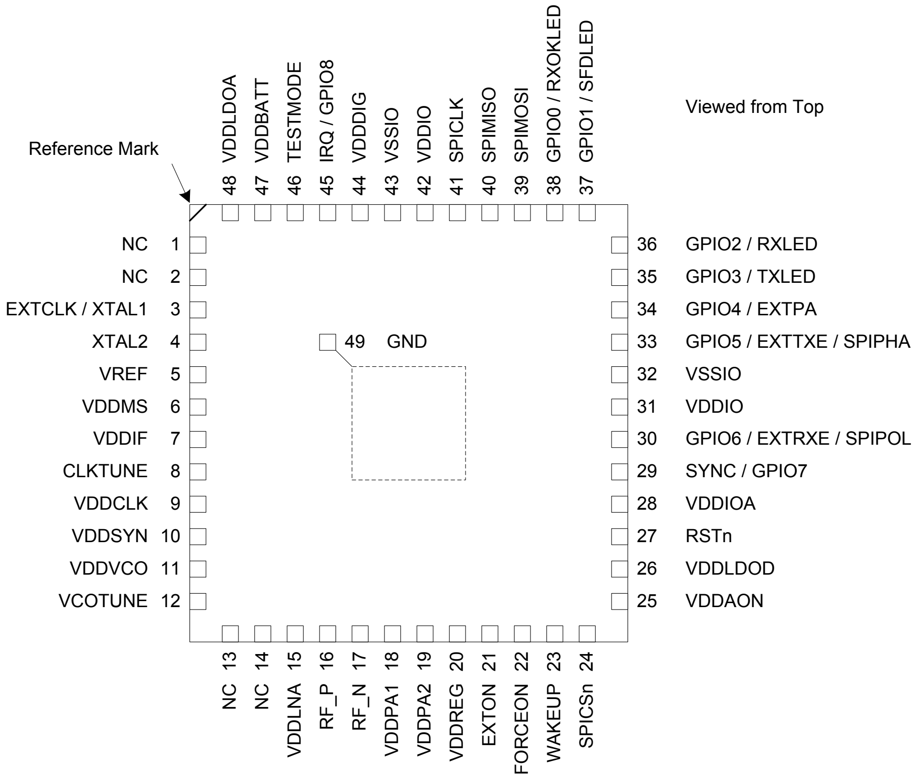


Figure 2: DW1000 Pin Assignments

2.2 Pin Descriptions

SIGNAL NAME	PIN	I/O	DESCRIPTION
Crystal Interface			
EXTCLK / XTAL1	3	AI	Reference crystal input or external reference overdrive pin
XTAL2	4	AI	Reference crystal input
Digital Interface			
SPICLK	41	DI	SPI clock
SPIMISO	40	DO	SPI data output. Refer to section 5.8.
SPIMOSI	39	DI	SPI data input. Refer to section 5.8.
SPICSn	24	DI	SPI chip select. This is an active low enable input. The high-to-low transition on SPICSn signals the start of a new SPI transaction. SPICSn can also act as a wake-up signal to bring DW1000 out of either SLEEP or DEEPSLEEP states. Refer to section 6.
SYNC / GPIO7	29	DI	The SYNC input pin is used for external synchronization (see section 5.13). When the SYNC input functionality is not being used this pin may be reconfigured as a general purpose I/O pin, GPIO7
WAKEUP	23	DI	When asserted into its active high state, the WAKEUP pin brings the DW1000 out of SLEEP or DEEPSLEEP states into operational mode.
EXTON	21	DO	External device enable. Asserted during wake up process and held active until device enters sleep mode. Can be used to control external DC-DC converters or other circuits that are not required when the device is in sleep mode so as to minimize power consumption. Refer to sections 5.5.1 & 7.
FORCEON	22	DI	Not used in normal operation. Must be connected to ground

SIGNAL NAME	PIN	I/O	DESCRIPTION
IRQ / GPIO8	45	DO	Interrupt Request output from the DW1000 to the host processor. By default IRQ is an active-high output. When the IRQ functionality is not being used the pin may be reconfigured as a general purpose I/O line, GPIO8.
GPIO6 / EXTRXE / SPIPOL	30	DIO	General purpose I/O pin. On power-up it acts as the SPIPOL (SPI polarity selection) pin for configuring the SPI operation mode. For details of this please refer to section 5.8. After power-up, the pin will default to a General Purpose I/O pin. It may be configured for use as EXTRXE (External Receiver Enable). This pin goes high when the DW1000 is in receive mode.
GPIO5 / EXTTXE / SPIPHA	33	DIO	General purpose I/O pin. On power-up it acts as the SPIPHA (SPI phase selection) pin for configuring the SPI mode of operation. Refer to section 5.8 for further information. After power-up, the pin will default to a General Purpose I/O pin. It may be configured for use as EXTTXE (External Transmit Enable). This pin goes high when the DW1000 is in transmit mode.
GPIO4 / EXTPA	34	DIO	General purpose I/O pin. It may be configured for use as EXTPA (External Power Amplifier). This pin can enable an external Power Amplifier.
GPIO3 / TXLED	35	DIO	General purpose I/O pin. It may be configured for use as a TXLED driving pin that can be used to light a LED following a transmission. Refer to the DW1000 User Manual [2] for details of LED use.
GPIO2 / RXLED	36	DIO	General purpose I/O pin. It may be configured for use as a RXLED driving pin that can be used to light a LED during receive mode. Refer to the DW1000 User Manual [2] for details of LED use.
GPIO1 / SFDLED	37	DIO	General purpose I/O pin. It may be configured for use as a SFDLED driving pin that can be used to light a LED when SFD (Start Frame Delimiter) is found by the receiver. Refer to the DW1000 User Manual [2] for details of LED use.
GPIO0 / RXOKLED	38	DIO	General purpose I/O pin. It may be configured for use as a RXOKLED driving pin that can be used to light a LED on reception of a good frame. Refer to the DW1000 User Manual [2] for details of LED use.
RSTn	27	DIO	Reset pin. Active Low Output. May be pulled low by external open drain driver to reset the DW1000. Refer to section 5.6.
TESTMODE	46	DIO	Not used in normal operation. Must be connected to ground
Reference voltages			
VREF	5	AIO	Used for on-chip reference current generation. Must be connected to an 11 kΩ (1% tolerance) resistor to ground
Digital Power Supplies			
VDDLDOD	26	P	External supply for digital circuits.
VDDIOA	28	P	External supply for digital IO ring.
VSSIO	32 43	G	Negative I/O ring supply. Must be connected to ground
Digital Decoupling			
VDDREG	20	PD	Output of on-chip regulator. Connect to VDDDIG on PCB
VDDDIG	44	PD	Output of on-chip regulator. Connect to VDDREG on PCB
VDDIO	31 42	PD	Digital IO Ring Decoupling.
RF Interface			
RF_P	16	AIO	Positive pin of the 100 Ω differential RF pair. Should be AC coupled.

SIGNAL NAME	PIN	I/O	DESCRIPTION
RF_N	17	AIO	Negative pin of the 100 Ω differential RF pair. Should be AC coupled.
PLL Interface			
CLKTUNE	8	AIO	Clock PLL loop filter connection to off-chip filter components. Referenced to VDDCLK.
VCOTUNE	12	AIO	RF PLL loop filter connection to off-chip filter components. Referenced to VDDVCO.
Analog Power Supplies			
VDDAON	25	P	External supply for the Always-On (AON) portion of the chip.
VDDPA1	18	P	External supply to the transmitter power amplifier.
VDDPA2	19	P	External supply to the transmitter power amplifier.
VDDLNA	15	P	External supply to the receiver LNA
VDDLDOA	48	P	External supply to analog circuits.
VDDBATT	47	P	External supply to all other on-chip circuits.
Analog Supply Decoupling			
VDDCLK	9	PD	Output of on-chip regulator to off-chip decoupling capacitor.
VDDIF	7	PD	Output of on-chip regulator to off-chip decoupling capacitor.
VDDMS	6	PD	Output of on-chip regulator to off-chip decoupling capacitor.
VDDSYN	10	PD	Output of on-chip regulator to off-chip decoupling capacitor.
VDDVCO	11	PD	Output of on-chip regulator to off-chip decoupling capacitor.
Ground Paddle			
GND	49	G	Ground Paddle on underside of package. Must be soldered to the PCB ground plane for thermal and RF performance.
Others			
NC	1 2 13 14	NC	Not used in normal operation. Do not connect

Table 1: DW1000 Pin functions

ABBREVIATION	EXPLANATION
AI	Analog Input
AIO	Analog Input / Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input / Output
DO	Digital Output
G	Ground
P	Power Supply
PD	Power Decoupling
NC	No Connect
Note: Any signal with the suffix 'n' indicates an active low signal.	

Table 2: Explanation of Abbreviations

3 ELECTRICAL SPECIFICATIONS

3.1 Nominal Operating Conditions

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Operating temperature	-40		+85	˚C	
Supply voltage VDDIOA	2.8	3.3	3.6	V	
Supply voltage VDDBATT, VDDAON, VDDLNA, VDDPA	2.8	3.3	3.6	V	
Supply voltage VDDLDOA, VDDLDOD	1.6	1.8	3.6	V	See section 7.2

Table 3: DW1000 Operating Conditions

Note: Unit operation is guaranteed by design when operating within these ranges

3.2 DC Characteristics

T_{amb} = 25 ˚C, all supplies centered on typical values

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Supply current DEEP SLEEP mode		100		nA	Total current drawn from all 3.3 V and 1.8 V supplies
Supply current SLEEP mode		2		µA	
Supply current IDLE mode		18		mA	
Supply current INIT mode		4		mA	
TX : 3.3 V supplies (VDDBAT, VDDPA1, VDDPA2, VDDLNA, VDDAON, VDDIOA)			70	mA	Channel 5:TX Power: 9.3 dBm/500 MHz
TX : 1.8 V supplies (VDDLDOA, VDDLDOD)			90*	mA	
RX : 3.3 V supplies (VDDBAT, VDDPA1, VDDPA2, VDDLNA, VDDAON, VDDIOA)			30	mA	Channel 5
RX : 1.8 V supplies (VDDLDOA, VDDLDOD)			210*	mA	
Digital input voltage high	0.7*VDDIO			V	
Digital input voltage low			0.3*VDDIO	V	
Digital output voltage high	0.7*VDDIO			V	Assumes 500 Ω load
Digital output voltage low			0.3*VDDIO	V	Assumes 500 Ω load
Digital Output Drive Current GPIOx, IRQ SPIMISO EXTON	 4 8 3	 6 10 4		mA	

** These currents are on the 1.8 V supplies, not referenced back to the 3.3 V supply*

Table 4: DW1000 DC Characteristics

3.3 Receiver AC Characteristics

T_{amb} = 25 ˚C, all supplies centered on nominal values

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Frequency range	3244		6999	MHz	
Channel bandwidths		500 900		MHz	Channel 1,2,3 and 5 Channel 4 and 7
In-band blocking level		30		dBc	Continuous wave interferer
Out-of-band blocking level		55		dBc	Continuous wave interferer

Table 5: DW1000 Receiver AC Characteristics

3.4 *Receiver Sensitivity Characteristics*

T_{amb} = 25 ˚C, all supplies centered on typical values. 20 byte payload

Packet Error Rate	Data Rate	Receiver Sensitivity	Units	Condition/Note		
1%	110 kbps	-106	dBm/500 MHz	Preamble 2048	Carrier frequency offset ±1 ppm	All measurements performed on Channel 5, PRF 16 MHz
10%	110 kbps	-107	dBm/500 MHz	Preamble 2048		
1%	110 kbps	-102	dBm/500 MHz	Preamble 2048	Carrier frequency offset ±10 ppm	
	850 kbps	-101	dBm/500 MHz	Preamble 1024		
	6.8 Mbps	-93	dBm/500 MHz	Preamble 256		
10%	110 kbps	-106	dBm/500 MHz	Preamble 2048		
	850 kbps	-102	dBm/500 MHz	Preamble 1024		
	6.8 Mbps	-94	dBm/500 MHz	Preamble 256		

Table 6: Typical Receiver Sensitivity Characteristics

3.5 *Reference Clock AC Characteristics*

T_{amb} = 25 ˚C, all supplies centered on typical values

3.5.1 Reference Frequency

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Crystal oscillator reference frequency		38.4		MHz	A 38.4 MHz signal can be provided from an external reference in place of a crystal if desired. See 5.1.7
Crystal specifications					
Load capacitance	1		15	pF	
Shunt capacitance	0		4	pF	
Drive level			50	µW	
Equivalent Series Resistance (ESR)			60	Ω	
Frequency tolerance			±20	ppm	DW1000 includes circuitry to trim the crystal oscillator to reduce the initial frequency offset
Crystal trimming range		±25		ppm	Trimming range provided by on-chip circuitry. Depends on the crystal used and PCB design.
External Reference					
Amplitude	0.8			V_{pp}	Must be AC coupled
SSB phase noise power density			-132	dBc/Hz	@1 kHz offset
SSB phase noise power density			-145	dBc/Hz	@10 kHz offset
Duty Cycle	40		60	%	
Low Power RC Oscillator	5	12	15	kHz	

Table 7: DW1000 Reference Clock AC Characteristics

3.6 Transmitter AC Characteristics

T_{amb} = 25 ˚C, all supplies centered on typical values

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Frequency range	3244		6999	MHz	
Channel Bandwidths		500 900		MHz	Channel 1, 2, 3 and 5 Channel 4 and 7
Output power spectral density (programmable)		-39	-35	dBm/MHz	See Section 5.5
Load impedance		100		Ω	Differential
Power level range		37		dB	
Coarse Power level step		3		dB	
Fine Power level step		0.5		dB	
Output power variation with temperature		0.05		dB/°C	
Output power variation with voltage		2.73 3.34		dB/V	Channel 2 Channel 5

Table 8: DW1000 Transmitter AC Characteristics

3.7 Temperature and Voltage Monitor Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Voltage Monitor Range	2.4		3.75	V	
Voltage Monitor Precision		20		mV	
Voltage Monitor Accuracy		140		mV	
Temperature Monitor Range	-40		+100	°C	
Temperature Monitor Precision		0.9		°C	
Temperature Monitor Accuracy		2		°C	

Table 9: DW1000 Temperature and Voltage Monitor Characteristics

3.8 Absolute Maximum Ratings

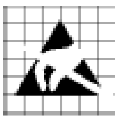
Parameter	Min.	Max.	Units
Voltage VDDPA / VDDLNA / VDDLDOD / VDDLDOA / VDDBATT / VDDIOA / VDDAON / VDDIO	-0.3	4.0	V
Receiver Power		0	dBm
Temperature - Storage temperature	-65	+150	˚C
Temperature - Operating temperature	-40	+85	˚C
ESD (Human Body Model)		2000	V

Table 10: DW1000 Absolute Maximum Ratings

Stresses beyond those listed in this table may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond those indicated in the operating conditions of the specification is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

LIFE SUPPORT POLICY

DecaWave products are not authorized for use in safety-critical applications (such as life support) where a failure of the DecaWave product would reasonably be expected to cause severe personal injury or death. DecaWave customers using or selling DecaWave products in such a manner do so entirely at their own risk and agree to fully indemnify DecaWave and its representatives against any damages arising out of the use of DecaWave products in such safety-critical applications.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage

4 Typical Performance

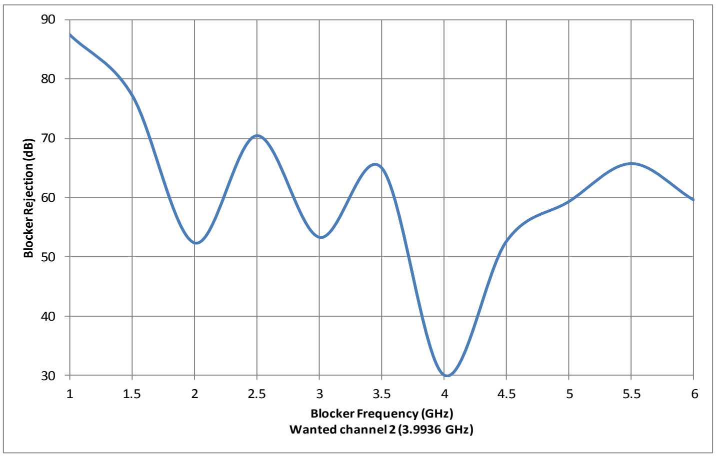


Figure 3 : RX Interferer Immunity on Channel 2

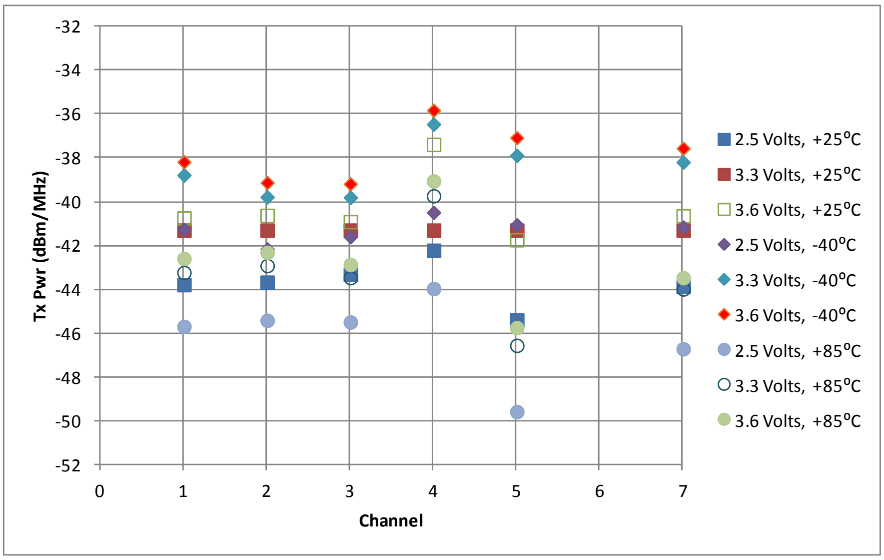


Figure 4: TX output Power over Temp & Voltage

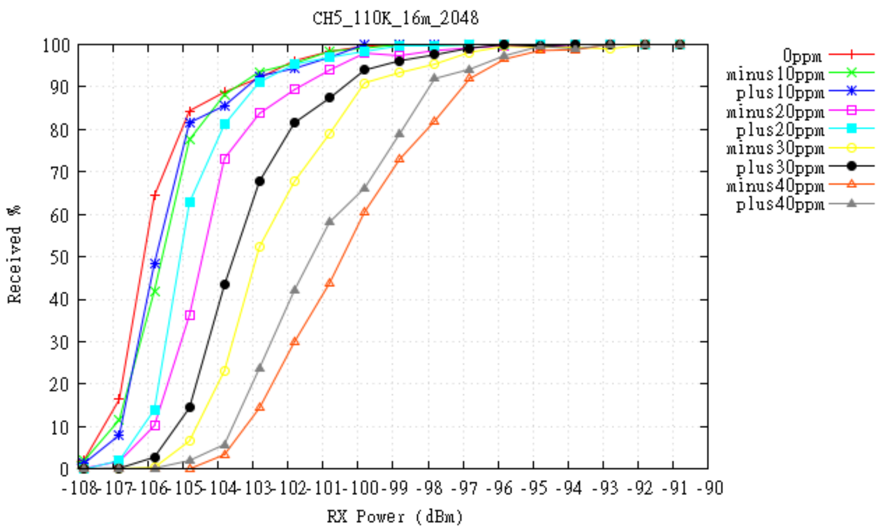


Figure 5: Receiver Sensitivity Channel 5 110K Data Rate 16M PRF 2048 Preamble Symbols

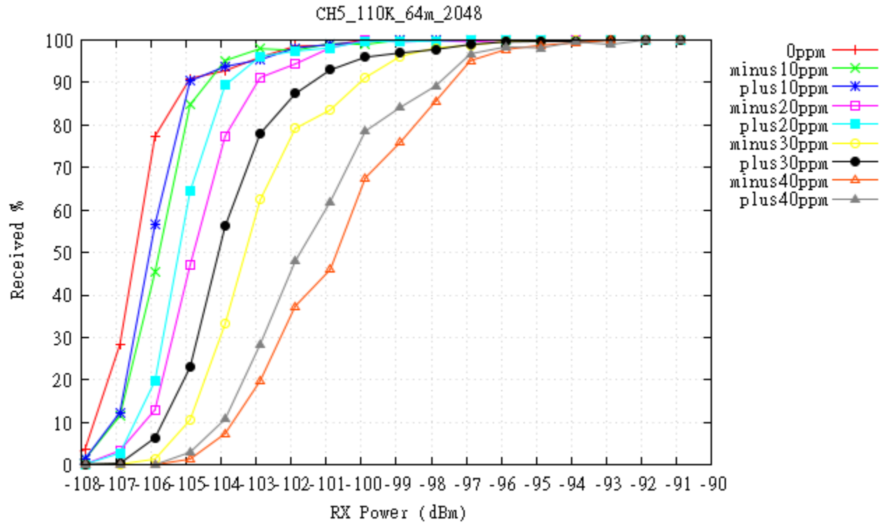


Figure 6: Receiver Sensitivity Channel 5 110K Data Rate 64M PRF 2048 Preamble Symbols

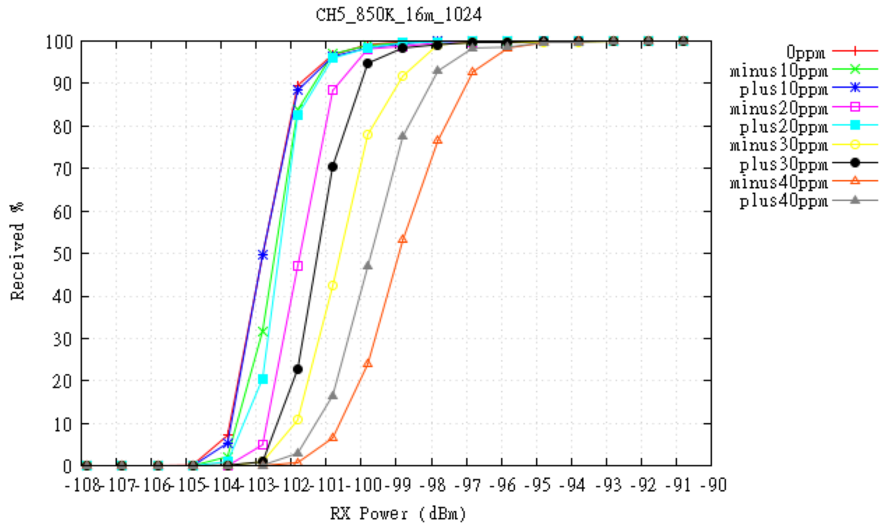


Figure 7: Receiver Sensitivity Channel 5 850K Data Rate 16M PRF 1024 Preamble Symbols

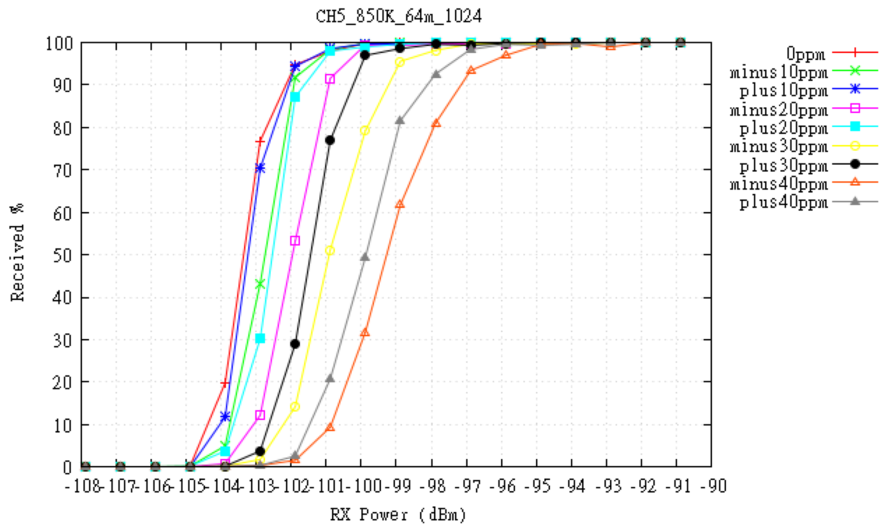


Figure 8: Receiver Sensitivity Channel 5 850K Data Rate 64M PRF 1024 Preamble Symbols

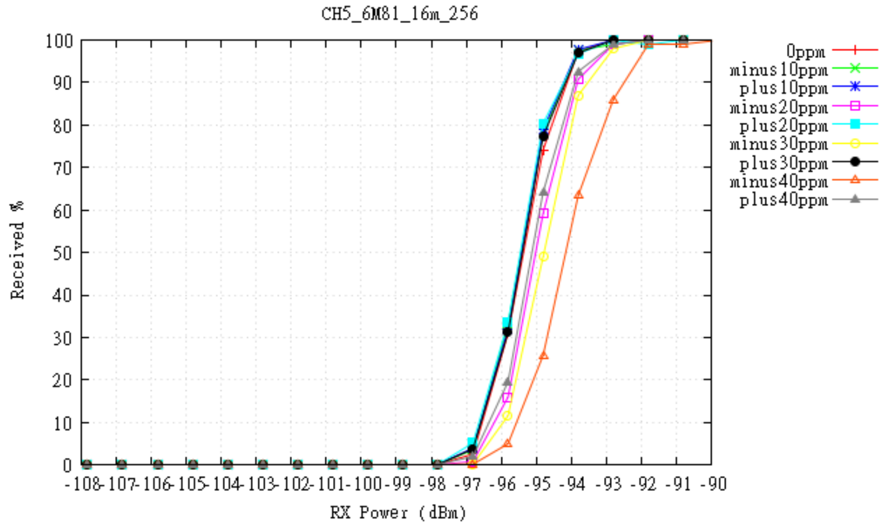


Figure 9: Receiver Sensitivity Channel 5 6.81M Data Rate 16M PRF 256 Preamble Symbols

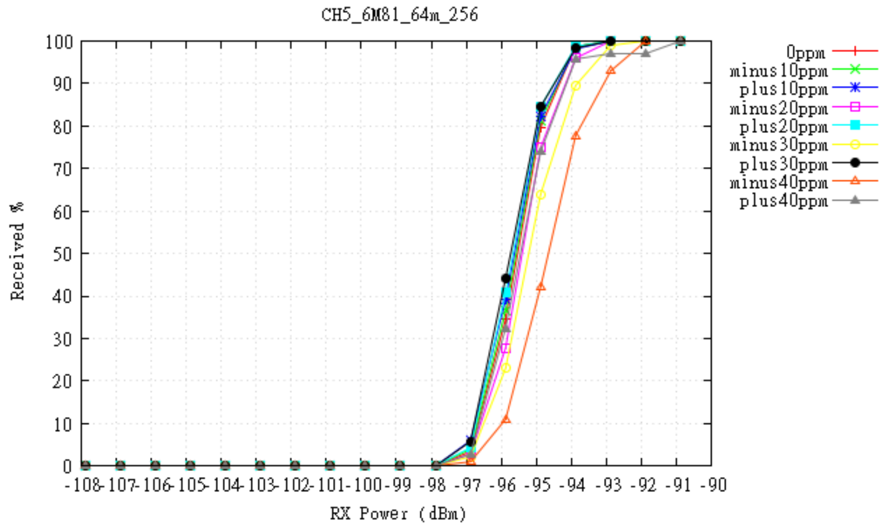


Figure 10: Receiver Sensitivity Channel 5 6.81M Data Rate 64M PRF 1256 Preamble Symbols

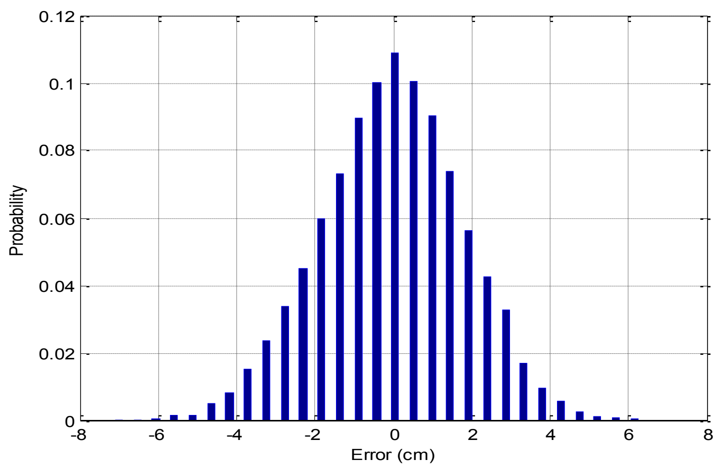


Figure 11: Typical probability distribution of 2 way ranging errors at 16MHz PRF

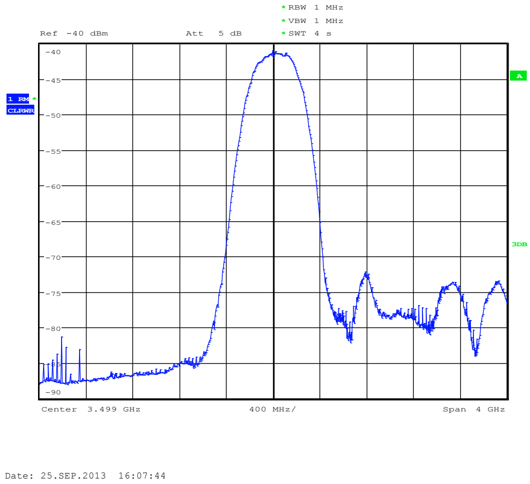


Figure 12: TX Spectrum Channel 1

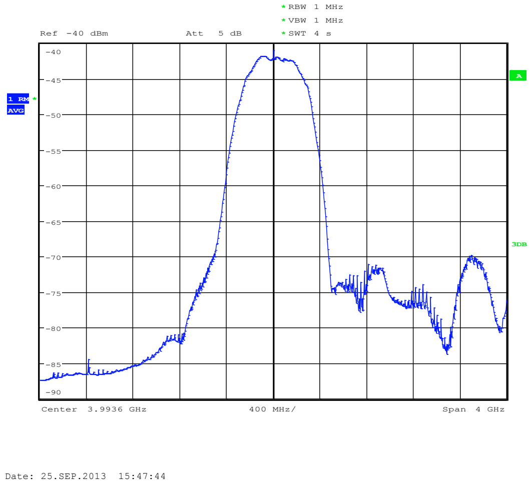


Figure 13: TX Spectrum Channel 2

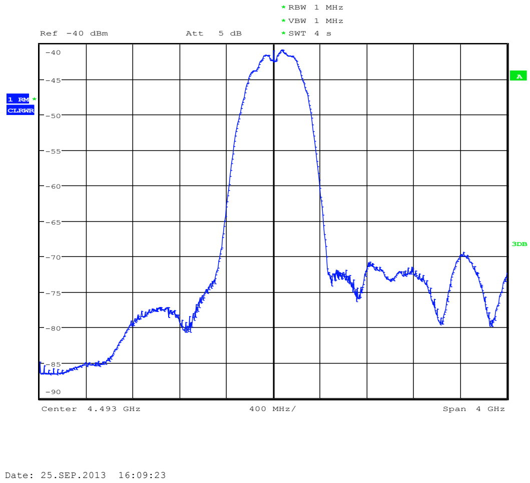


Figure 14: TX Spectrum Channel 3

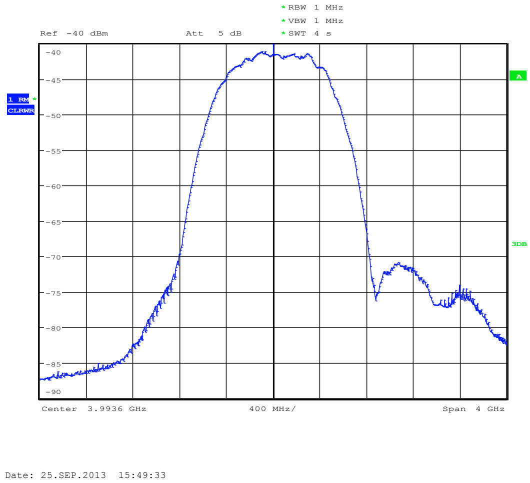


Figure 15: TX Spectrum Channel 4

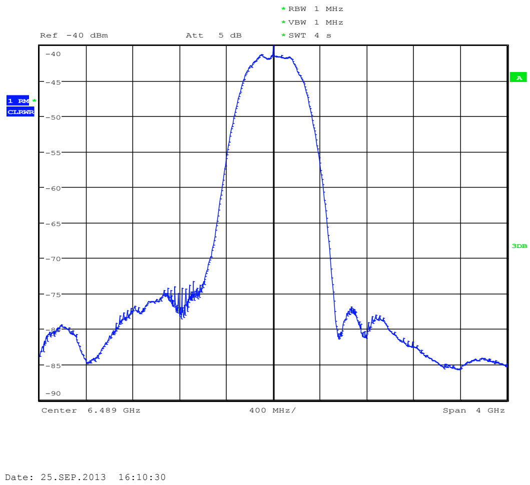


Figure 16: TX Spectrum Channel 5

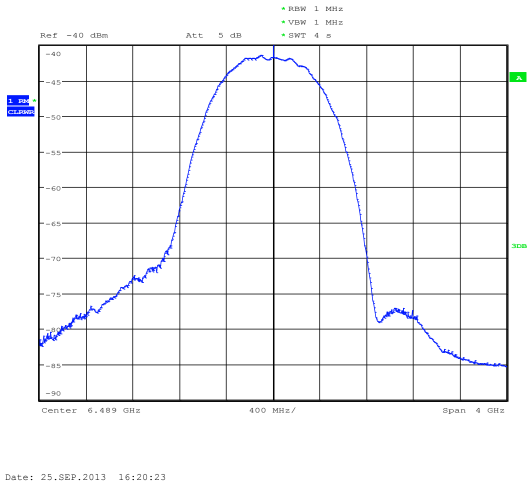


Figure 17: TX Spectrum Channel 7

5 Functional Description

5.1 Physical Layer Modes

Please refer to IEEE802.15.4-2011 [1] for the PHY specification.

5.1.1 Supported Channels and Bandwidths

The DW1000 supports the following six IEEE802.15.4-2011 [1] UWB channels: -

UWB Channel Number	Centre Frequency (MHz)	Band (MHz)	Bandwidth (MHz)
1	3494.4	3244.8 – 3744	499.2
2	3993.6	3774 – 4243.2	499.2
3	4492.8	4243.2 – 4742.4	499.2
4	3993.6	3328 – 4659.2	1331.2*
5	6489.6	6240 – 6739.2	499.2
7	6489.6	5980.3 – 6998.9	1081.6*

**DW1000 maximum receiver bandwidth is approximately 900 MHz*

Table 11: UWB IEEE802.15.4-2011 UWB channels supported by the DW1000

5.1.2 Supported Bit Rates and Pulse Repetition Frequencies (PRF)

The DW1000 supports IEEE802.15.4-2011 [1] UWB standard bit rates of 110 kbps, 850 kbps and 6.81 Mbps and nominal PRF values of 16 and 64 MHz.

PRF* (MHz)	Data Rate (Mbps)
16	0.11
16	0.85
16	6.81
64	0.11
64	0.85
64	6.81

**Actual PRF mean values are slightly higher for SYNC as opposed to the other portions of a frame. Mean PRF values are 16.1/15.6 MHz and 62.89/62.4 MHz, nominally referred to as 16 and 64MHz in this document. Refer to [1] for full details of peak and mean PRFs.*

Table 12: UWB IEEE802.15.4-2011 [1] UWB bit rates and PRF modes supported by the DW1000

5.1.3 Frame Format

IEEE802.15.4-2011 [1] frames are structured as shown in Figure 18. Detailed descriptions of the frame format are given in the standard [1]. The frame consists of a synchronisation header (SHR) which includes the preamble symbols and start frame delimiter (SFD), followed by the PHY header (PHR) and data. The data frame is usually specified in number of bytes and the frame format will include 48 Reed-Solomon parity bits following each block of 330 data bits (or less).

The maximum standard frame length is 127 bytes, including the 2-byte FCS.

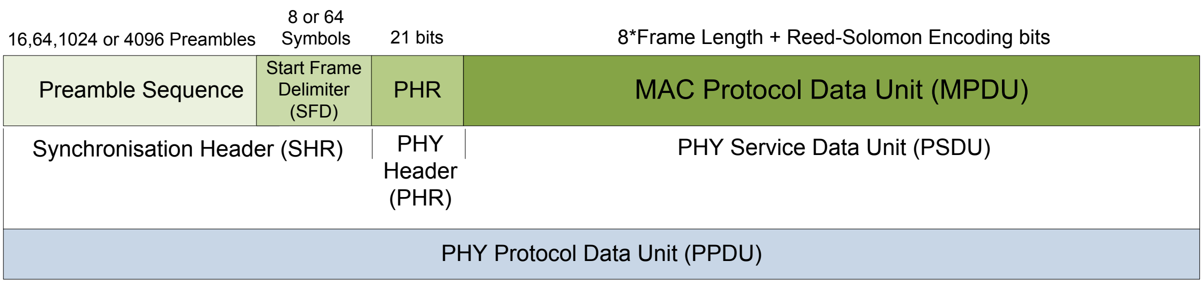


Figure 18: IEEE802.15.4-2011 PPDU Structure

5.1.4 Symbol Timings

Timing durations in IEEE802.15.4-2011 [1] are expressed in an integer number of symbols. This convention is adopted in DW1000 documentation. Symbol times vary depending on the data rate and PRF configuration of the device and the part of the frame. See Table 13 for all symbol timings supported by DW1000.

PRF (MHz)	Data Rate (Mbps)	SHR (ns)	PHR (ns)	Data (ns)
16	0.11	993.59	8205.13	8205.13
16	0.85	993.59	1025.64	1025.64
16	6.81	993.59	1025.64	128.21
64	0.11	1017.63	8205.13	8205.13
64	0.85	1017.63	1025.64	1025.64
64	6.81	1017.63	1025.64	128.21

Table 13: DW1000 Symbol Durations

5.1.5 Proprietary Long Frames

The DW1000 offers a proprietary long frame mode where frames of up to 1023 bytes may be transferred. This requires a non-standard PHR encoding and so cannot be used in a standard system. Refer to the DW1000 User Manual for full details [2].

5.1.6 Turnaround Times

Turn-around times given in the table below are as defined in [1].

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Turn-around time RX to TX*		10		µs	Achievable turnaround time depends on device configuration and frame parameters and on external host controller.
Turn-around time TX to RX*		6		µs	

Table 14: Turn-around Times

5.1.7 Frame Filter

A standard frame filtering format is defined in IEEE802.15.4-2011 [1]. An overview of the MAC frame format is given in Figure 19 . Note that the Auxiliary Security Header is not processed in DW1000 hardware.

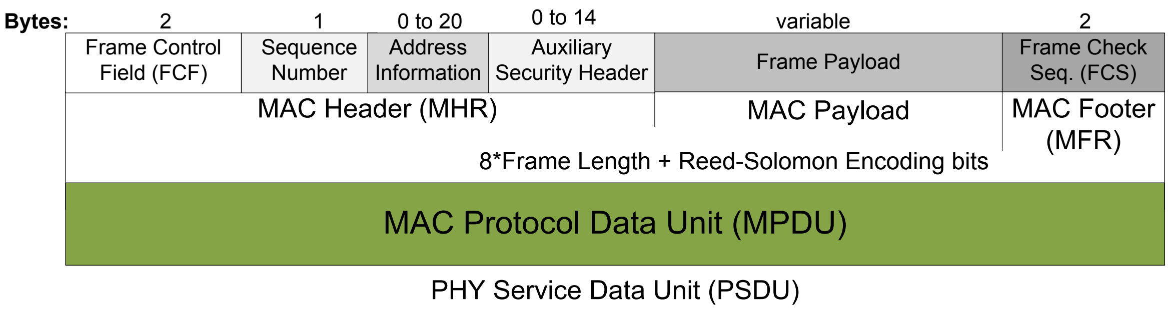


Figure 19: IEEE802.15.4-2011 MAC Frame Format

Frame filtering allows the receiver to automatically discard frames that do not match a defined set of criteria. The DW1000 has a number of separately configurable frame filtering criteria to allow selection of the frame types to accept or discard. See IEEE802.15.4-2011 [1] for filtering field definition and acceptance rules.

5.1.8 Frame Check Sequence (FCS)

The FCS is also known as the MAC Footer (MFR). It is a 2-byte CRC appended to frames. See IEEE802.15.4-2011 [1] for information on FCS generation.

5.2 Reference Crystal Oscillator

The on-chip crystal oscillator generates the reference frequency for the integrated frequency synthesizers RFPLL and CLKPLL. The oscillator operates at a frequency of 38.4 MHz.

DW1000 provides the facility to trim out initial frequency error in the 38.4 MHz reference crystal, see section 5.14. Up to ±25 ppm trimming range is available. Loading capacitors should be chosen such that minimum frequency error (from the channel center frequency) is achieved when the trim value is approximately mid-range.
In applications that require tighter frequency tolerance (maximum range) an external oscillator such a TCXO can be used to drive the XTAL1 pin directly.

5.3 Synthesizer

DW1000 contains 2 frequency synthesizers, RFPLL which is used as a local oscillator (LO) for the TX and RX and CLKPLL which is used as a system clock. Both of these synthesizers are fully integrated apart from external passive 2nd order loop filters. The component values for these loop filters do not change regardless of the RF channel used. The register programming values for these synthesizers is contained in the user manual [2]

5.4 Receiver

5.4.1 Bandwidth setting

The receiver can be configured to operate in one of two bandwidth modes; 500 MHz or 900 MHz. The selection of a particular bandwidth mode is made by register settings and is described in the DW1000 User Manual [2].

5.4.2 Automatic Gain Control (AGC)

Automatic Gain Control is provided to ensure optimum receiver performance by adjusting receiver gain for changing signal and environmental conditions. The DW1000 monitors the received signal level and makes appropriate automatic adjustments to ensure optimum receiver performance is maintained.

5.5 Transmitter

5.5.1 Transmit Output Power

DW1000 transmit power is fully adjustable as is the transmit spectrum width ensuring that applicable regulatory standards such as FCC [4] and ETSI [3] can be met. For maximum range the transmit power should be set such that the EIRP at the antenna is as close as possible to the maximum allowed, -41.3 dBm/MHz in most regions. See section 5.14.3 for more details.

5.5.2 Transmit Bandwidth Setting

The transmitter can be configured to operate over a wide range of bandwidths. The selection of a particular bandwidth mode is made by register settings and is described in the DW1000 User Manual [2].

Transmit spectral shape can also be adjusted to compensate for PCB and external components in order to give an optimal transmit spectral mask.

5.6 Power Up

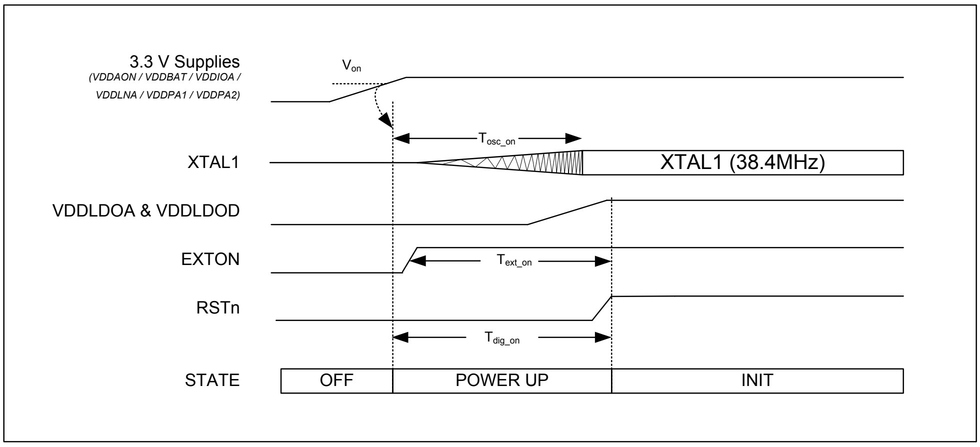


Figure 20: DW1000 Power-up Sequence

When power is applied to the DW1000, RSTn is driven low by the DW1000 internal circuitry as part of its power up sequence. See Figure 20 above. RSTn remains low until the XTAL oscillator has powered up and its output is suitable for use by the rest of the device. Once that time is reached the DW1000 de-asserts RSTn.

Parameter	Description	Nominal Value	Units
V_{ON}	Voltage threshold to enable power up	2.0	V
T_{OSC_ON}	Time taken for oscillator to start up and stabilise	1.5	ms
T_{EXT_ON}	EXTON goes high this long before RSTn is released	3	ms
T_{DIG_ON}	RSTn held low by internal reset circuit / driven low by external reset circuit	3	ms

Table 15: DW1000 Power-up Timings

RSTn may be used as an output to reset external circuitry as part of an orderly bring up of a system as power is applied.

An external circuit can reset the DW1000 by asserting RSTn for a minimum of 10 ns. RSTn is an asynchronous input. DW1000 initialization will proceed when the pin is released to high impedance.

An external source should open-drain the RSTn pin once the DW1000 has been reset. When in DEEPSLEEP mode, the DW1000 drives RSTn to ground. This can result in current flowing if RSTn is driven high externally. RSTn should never be driven high by an external source.

5.7 Voltage/Temperature Monitors

The on-chip voltage and temperature monitors allow the host to read the voltage on the VDDAON pin and the internal die temperature information from the DW1000. See Table 9 for characteristics.

5.8 Host Controller Interface

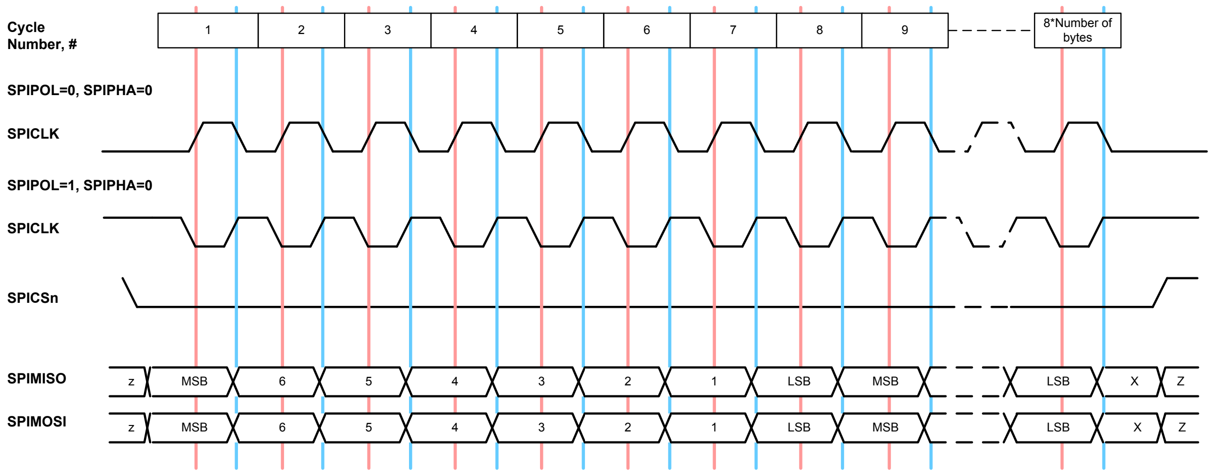


Figure 21: DW1000 SPIPHA=0 Transfer Protocol

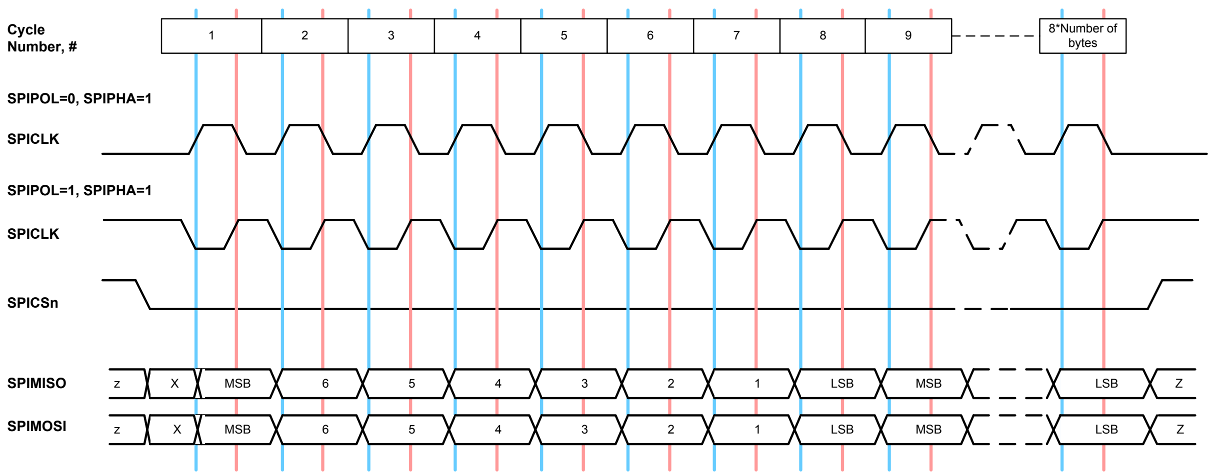


Figure 22: DW1000SPIPHA=1 Transfer Protocol

The DW1000 host communications interface is a slave-only SPI. Both clock polarities (SPIPOL=0/1) and phases (SPIPHA=0/1) are supported. The data transfer protocol supports single and multiple byte read/writes accesses. All bytes are transferred MSB first and LSB last. A transfer is initiated by asserting SPICSn low and terminated when SPICSn is deasserted high.

The DW1000 transfer protocols for each SPIPOL and SPIPHA setting are given in Figure 21 and Figure 22.

The MSB of the first byte is the read/write indicator, a low bit indicates a read access and a high bit indicates a write access. The second bit, bit 6 of the first byte, indicates whether a sub address byte will be included in the SPI access, a high bit indicates a further address byte to follow the initial byte and a low bit indicating that the bytes to follow the first byte are data. The 6 LSBs of the first byte contain an access address.

The second byte of a transfer command, if included, gives the sub address being accessed. If the MSB of this optional second byte is high, it indicates a second sub address byte to follow in the third transfer byte. The 7 LSBs of this second byte give the 7 LSBs of the sub address.

The third byte of a transfer command, if included give the 8 MSBs of the sub address.

The number of data bytes to follow the 1-3 command bytes is not limited by the DW1000 transfer protocol.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	Read/Write 0 – Read 1 – Write	Sub address 0 – no sub address 1 – sub address present	6-bit access address					
Sub Address 0 (Optional)	Extended sub address 0 – 1 byte sub address 1 – 2 byte sub address	7-bits of sub address. These will be the LSBs if more bits are to follow.						
Sub Address 1 (Optional)	8 bits of sub address. These will form the MSBs, bits [14:7] of the 15-bit sub address.							
Data	8-bit read/write bytes(variable number)							

Figure 23: SPI Byte Formatting

The SPIMISO line may be connected to multiple slave SPI devices each of which is required to go open-drain when their respective SPICSn lines are de-asserted.

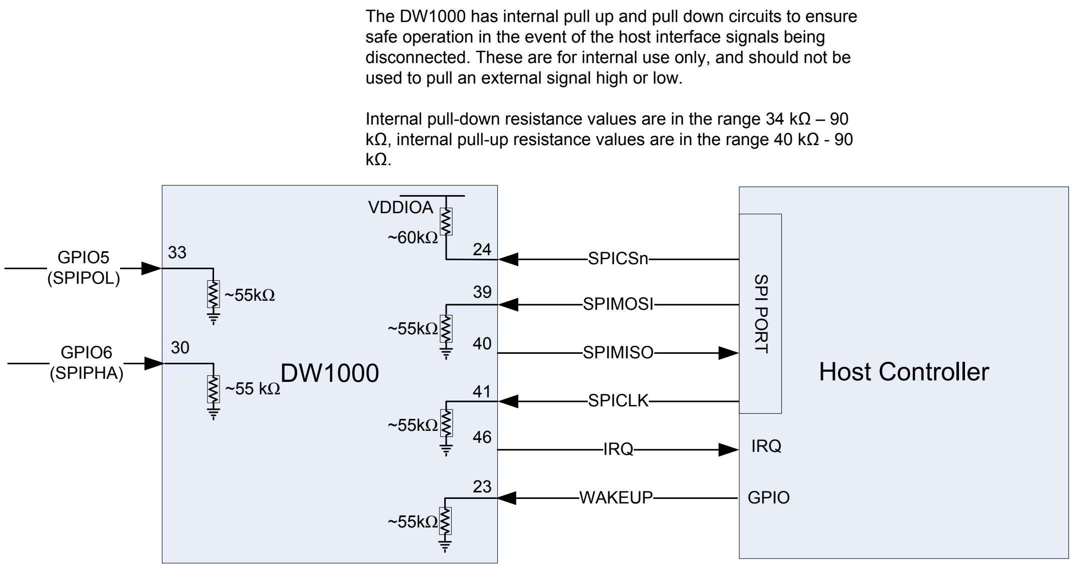


Figure 24: SPI Connections

More details of the protocol used for data transfer, the description of the accessible registers and the description of the bit functions of those registers are published in the DW1000 User Manual [2].

5.8.1 Configuring the SPI Mode

The SPI interface supports a number of different clock polarity and clock / data phase modes of operation. These modes are selected using GPIO5 & 6 as follows: -

GPIO 5 (SPIPOL)	GPIO 6 (SPIPHA)	SPI Mode	Description
0	0	0	Data is sampled on the rising (first) edge of the clock and launched on the falling (second) edge.
0	1	1	Data is sampled on the falling (second) edge of the clock and launched on the rising (first) edge
1	0	2	Data is sampled on the falling (first) edge of the clock and launched on the rising (second) edge.
1	1	3	Data is sampled on the rising (second) edge of the clock and launched on the falling (first) edge.
Note: The 0 on the GPIO pins can either be open circuit or a pull down to ground. The 1 on the GPIO pins is a pull up to VDDIO.			

Table 16: DW1000 SPI Mode Configuration

GPIO 5 / 6 are sampled / latched on the rising edge of the RSTn pin to determine the SPI mode. They are internally pulled low to configure a default SPI mode 0 without the use of external components. If a mode other 0 is required then they should be pulled up using an external resistor of value no greater than 10 kΩ to the VDDIO output supply.

If GPIO5 / 6 are also being used to control an external transmit / receive switch then external pull-up resistors of no less than 1 kΩ should be used so that the DW1000 can correctly drive these outputs in normal operation after the reset sequence / SPI configuration operation is complete.

The recommended range of resistance values to pull-up GPIO 5 / 6 is in the range of 1-10 kΩ. If it is required to pull-down GPIO 5 / 6, such as in the case where the signal is also pulled high at the input to an external IC, the resistor value chosen needs to take account of the DW1000 internal pull-down resistor values as well as those of any connected external pull-up resistors.

It is possible to set the SPI mode using the DW1000's one-time programmable configuration block to avoid the need for external components and to leave the GPIO free for use. This is a one-time activity and cannot be reversed so care must be taken to ensure that the desired SPI mode is set. Please refer to the DW1000 User Manual [2] for details of OTP use and configuration.

5.8.2 SPI Signal Timing

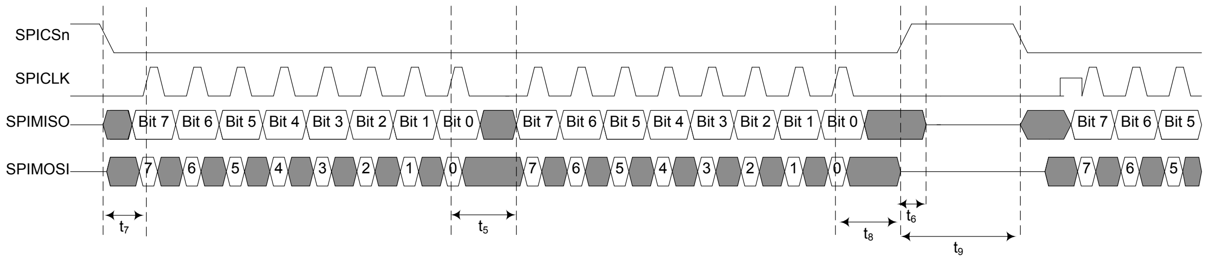


Figure 25: DW1000 SPI Timing Diagram

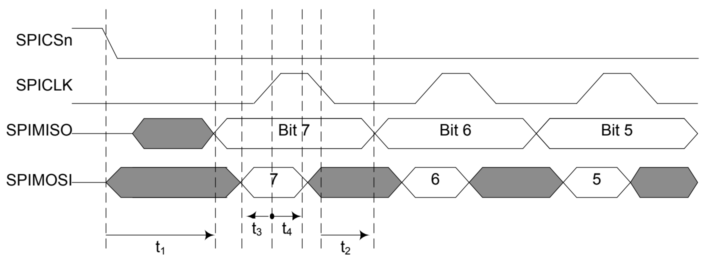


Figure 26: DW1000 SPI Detailed Timing Diagram

Parameter	Min	Typ	Max	Unit	Description
SPICLK Period	50			ns	The maximum SPI frequency is 20 MHz when the CLKPLL is locked, otherwise the maximum SPI frequency is 3 MHz.
t_1			38	ns	SPICSn select asserted low to valid slave output data

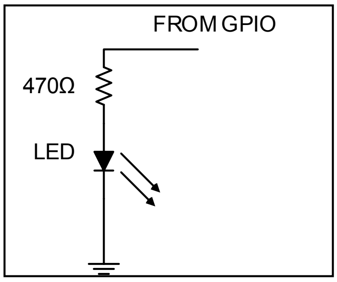
Parameter	Min	Typ	Max	Unit	Description
t_2	12			ns	SPICLK low to valid slave output data
t_3	10			ns	Master data setup time
t_4	10			ns	Master data hold time
t_5	32			ns	LSB last byte to MSB next byte
t_6			10	ns	SPICSn de-asserted high to SPIMISO tri-state
t_7	16			ns	Start time; time from select asserted to first SPICLK
t_8	40			ns	Idle time between consecutive accesses
t_9	40			ns	Last SPICLK to SPICSn de-asserted

Table 17: DW1000 SPI Timing Parameters

5.9 General Purpose Input Output (GPIO)

The DW1000 provides 8 user-configurable I/O pins.

On reset, all GPIO pins default to input. GPIO inputs, when appropriately configured, are capable of generating interrupts to the host processor via the IRQ signal. Some GPIO lines have multiple functions as described in 2.2 above.



GPIO0, 1, 2, & 3, as one of their optional functions, can drive LEDs to indicate the status of various chip operations. Any GPIO line being used to drive an LED in this way should be connected as shown. GPIO5 & 6 are used to configure the operating mode of the SPI as described in 5.8.1. GPIO4, 5 & 6 may be optionally used to implement a scheme with an external power amplifier to provide a transmit power level in excess of that provided by the DW1000.

The DW1000 User Manual [2] provides details of the configuration and use of the GPIO lines.

5.10 Memory

The DW1000 includes a number of user accessible memories: -

5.10.1 Receive and Transmit data buffers

Buffers used to store received data to be read from the DW1000 by the host controller and data for transmission written into the DW1000 by the host controller. These are sized as follows: -

Memory	Size (bits)	Description
Tx Buffer	1024 x 8	Transmit data buffer. Contains data written by the host processor to be transmitted via the transmitter
Rx Buffer	1024 x 8 x 2	Receive data buffer. Contains data received via the receiver to be read by the host processor via the SPI interface. Double buffered so that the receiver can receive a second packet while the first is being read by the host controller

Table 18: Transmit & Receive Buffer Memory Size

5.10.2 Accumulator memory

The accumulator memory is used to store the channel impulse response estimate.

Memory	Size (bits)	Description
Accumulator	1016 x 32	Accumulator buffer. Used to store channel impulse response estimate data to be optionally read by the host controller

Table 19: Accumulator Memory Size

5.10.3 One Time Programmable (OTP) Calibration Memory

The DW1000 contains a small amount of user programmable OTP memory that is used to store per chip calibration information.

Memory	Size (bits)	Description
Calibration	56 x 32	One time programmable area of memory used for storing calibration data.

Table 20: OTP calibration memory

5.11 Interrupts and Device Status

DW1000 has a number of interrupt events that can be configured to drive the IRQ output pin. The default IRQ pin polarity is active high. A number of status registers are provided in the system to monitor and report data of interest. See DW1000 User Manual [2] for a full description of system interrupts and their configuration and status registers.

5.12 MAC Features

5.12.1 Timestamping

DW1000 generates transmit timestamps and captures receive timestamps. These timestamps are 40-bit values at a nominal 64 GHz resolution, for approximately 15 ps event timing precision. These timestamps enable ranging calculations.

DW1000 allows antenna delay values to be programmed for automatic adjustment of timestamps. See the DW1000 User Manual [2] for more details of DW1000 implementation and IEEE802.15.4-2011 [1] for details of definitions and required precision of timestamps and antenna delay values.

5.12.2 FCS Generation and Checking

DW1000 will automatically append a 2-byte FCS to transmitted frames and check received frames' FCS. The DW1000 can be used to send frames with a host-generated FCS, if desired.

5.12.3 Automatic Frame Filtering

Automatic frame filtering can be carried out using the DW1000. Incoming frames can be rejected automatically if they fail frame type or destination address checks. See the DW1000 User Manual [2] for details.

5.12.4 Automatic Acknowledge

The DW1000 can be configured to automatically acknowledge received frames requesting acknowledgement. See the DW1000 User Manual [2] for details.

Note that RX-TX turnaround is optimised for Automatic Acknowledge and is typically ~6.5 µs, but depends on the configured frame parameters. The delay applied between frames is programmable in preamble symbol durations to allow compliance with IEEE802.15.4-2011 [1] SIFS and LIFS requirements.

5.12.5 Double Receive Buffer

The DW1000 has two receive buffers to allow the device to receive another frame whilst the host is accessing a previously received frame. Achievable throughput is increased by this feature. See the DW1000 User Manual [2] for details.

5.13 External Synchronization

The DW1000 provides a SYNC input. This allows: -

- Synchronization of multiple DW1000 timestamps.
- Transmission synchronous to an external reference.
- Receive timestamping synchronous to an external counter.

As shown in Figure 27 the SYNC input must be source synchronous with the external frequency reference. The SYNC input from the host system provides a common reference point in time to synchronise all the devices with the accuracy necessary to achieve high resolution location estimation.

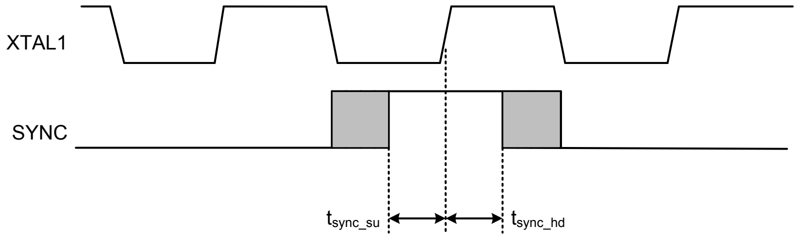


Figure 27: SYNC signal timing relative to XTAL1

Parameter	Min	Typ	Max	Unit	Description
t_{SYNC_SU}	10			ns	SYNC signal setup time before XTAL1 rising edge
t_{SYNC_HD}	10			ns	SYNC signal hold time after XTAL1 rising edge

Table 21: SYNC signal timing relative to XTAL

Further details on wired and wireless synchronisation are available from DecaWave.

5.14 Calibration and Spectral Tuning of the DW1000

5.14.1 Introduction

Depending on the end use application and the system design, certain internal settings in the DW1000 may need to be tuned. To help with this tuning a number of built in functions such as continuous wave TX and continuous packet transmission can be enabled. See the DW1000 User Manual [2] for further details on the sections described below.

5.14.2 Crystal Oscillator Trim

Minimising the carrier frequency offset between different DW1000 devices improves receiver sensitivity. The DW1000 allows trimming to reduce crystal initial frequency error. The simplest way to measure this frequency error is to observe the output of the transmitter at an expected known frequency using a spectrum analyzer or frequency counter.

To adjust the frequency offset, the device is configured to transmit a CW signal at a particular channel frequency (e.g. 6.5 GHz). By accurately measuring the actual centre frequency of the transmission the difference between it and the desired frequency can be determined. The trim value is then adjusted until the smallest frequency offset from the desired centre frequency is obtained.

If required, crystal trimming should be carried out on a per DW1000 PCB/module basis.

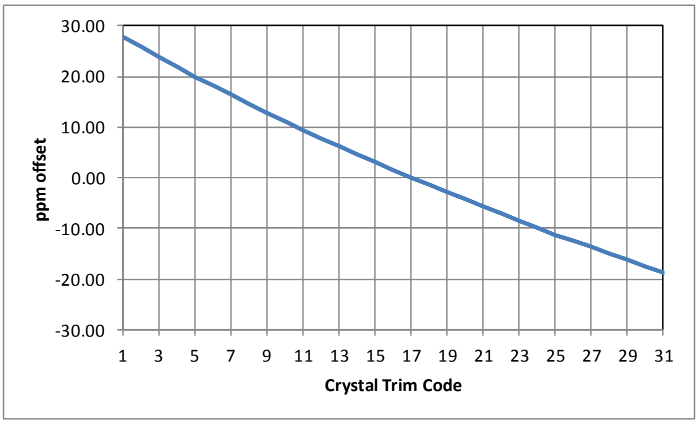


Figure 28: Typical Device Crystal Trim PPM Adjustment

5.14.3 Transmitter Calibration

In order to maximise range DW1000 transmit power spectral density (PSD) should be set to the maximum allowable for the geographic region. For most regions this is -41.3 dBm/MHz.

The DW1000 provides the facility to adjust the transmit power in coarse and fine steps; 3 dB and 0.5 dB nominally. It also provides the ability to adjust the spectral bandwidth. These adjustments can be used to maximise transmit power whilst meeting regulatory spectral mask.

If required, transmit calibration should be carried out on a per DW1000 PCB/module basis.

5.14.4 Antenna Delay Calibration

In order to measure range accurately, precise calculation of timestamps is required. To do this the antenna delay must be known. The DW1000 allows this delay to be calibrated and provides the facility to compensate for delays introduced by PCB, external components, antenna and internal DW1000 delays.

To calibrate the antenna delay, range is measured at a known distance using 2 DW1000 systems. Antenna delay is adjusted until the known distance and report range agree. The antenna delay can be stored in OTP memory.

Antenna delay calibration must be carried out as a once off measurement for each DW1000 design implementation. If required, for greater accuracy, antenna delay calibration should be carried out on a per DW1000 PCB/module basis.

6 Operational States and Power Management

6.1 Overview

The DW1000 has a number of basic operating states as follows: -

Name	Description
OFF	The chip is powered down
INIT	This is the lowest power state that allows external micro-controller access. In this state the DW1000 host interface clock is running off the 38.4 MHz reference clock. In this mode the SPICLK frequency can be no greater than 3 MHz.
IDLE	In this state the internal clock generator is running and ready for use. The analog receiver and transmitter are powered down. Full speed SPI accesses may be used in this state.
DEEPSLEEP	This is the lowest power state apart from the OFF state. In this state SPI communication is not possible. This state requires an external pin to be driven (can be SPICSn held low or WAKEUP held high) for a minimum of 500 µs to indicate a wake up condition. Once the device has detected the wake up condition, the EXTON pin will be asserted and internal reference oscillator (38.4 MHz) is enabled.
SLEEP	In this state the DW1000 will wake up after a programmed sleep count. The low power oscillator is running and the internal sleep counter is active. The sleep counter allows for periods from approximately 300 ms to 450 hours before the DW1000 wakes up.
RX	The DW1000 is actively looking for preamble or receiving a packet
RX PREAMBLE SNIFF	In this state the DW1000 periodically enters the RX state, searches for preamble and if no preamble is found returns to the IDLE state. If preamble is detected it will stay in the RX state and demodulate the packet. Can be used to lower overall power consumption.
TX	The DW1000 is actively transmitting a packet

Table 22: Operating States

For more information on operating states please refer to the user manual [2].

6.2 Operating States and their effect on power consumption

The DW1000 can be configured to return to any one of the states, IDLE, INIT, SLEEP or DEEPSLEEP between active transmit and receive states. This choice has implications for overall system power consumption and timing, see table below.

	DEVICE STATE				
	IDLE	**INIT**	**SLEEP**	**DEEPSLEEP**	**OFF**
Entry to State	Host controller command or previous operation completion	Host controller command	Host controller command or previous operation completion	Host controller command or previous operation completion	External supplies are off
Exit from State	Host controller command	Host controller command	Sleep counter timeout	SPICSn held low Or WAKEUP held high for 500 µs	External 3.3 V supply on
Next state	Various	IDLE	INIT	INIT	INIT
Current Consumption	19 mA (No DC/DC) 12 mA (with DC/DC)	4 mA	2 µA	100 nA	0
Configuration	Maintained	Maintained	Maintained	Maintained	Not maintained
Time before RX State Ready	Immediate	5 µs	3 ms	3 ms	3 ms
Time before TX State Ready	Immediate	5 µs	3 ms	3 ms	3 ms

Table 23: Operating States and their effect on power consumption

In the SLEEP, DEEPSLEEP and OFF states, it is necessary to wait for the main on-board crystal oscillator to power up and stabilize before the DW1000 can be used. This introduces a delay of up to 3 ms each time the DW1000 exits SLEEP, DEEPSLEEP and OFF states.

6.3 *Transmit and Receive power profiles*

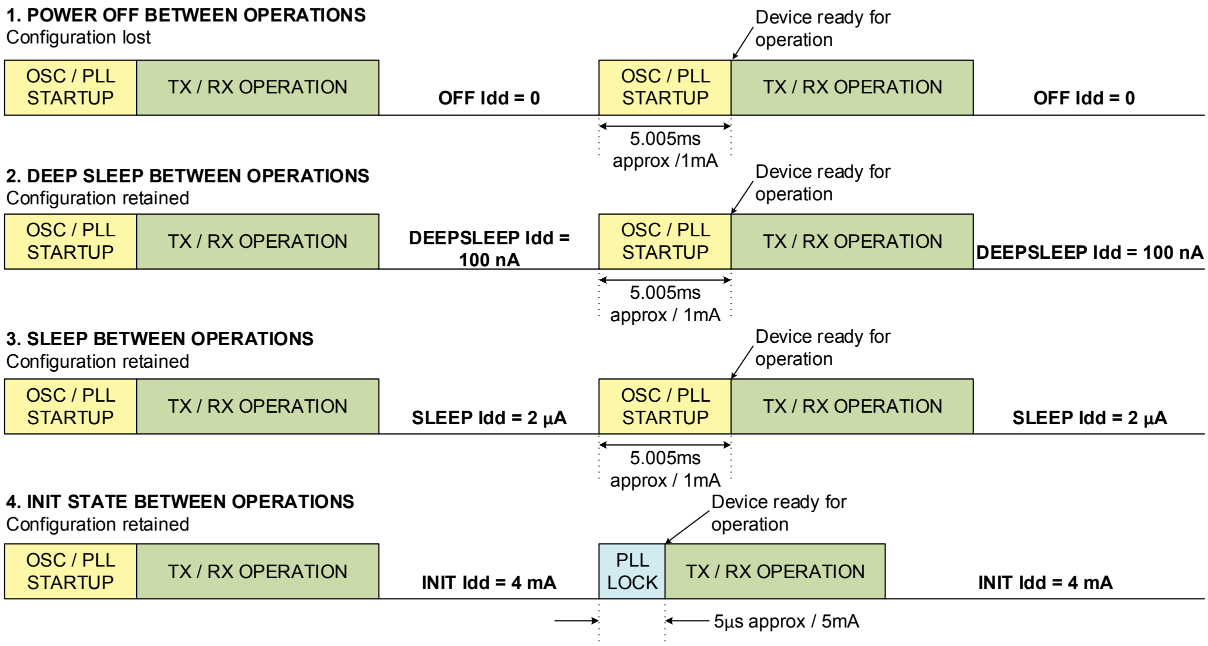


Figure 29: Sleep options between operations

The tables below show typical configurations of the DW1000 and their associated power profiles.

Mode	Data Rate	PRF (MHz)	Preamble (Symbols)	Data Length (Bytes)	Packet Duration (µs)	Typical Use Case (Refer to DW1000 user manual for further information)
Mode 1	110 kbps	16	1024	12	2084	RTLS, TDOA Scheme, Long Range, Low Density
Mode 2	6.8 Mbps	16	128	12	152	RTLS, TDOA Scheme, Short Range, High Density
Mode 3	110 kbps	16	1024	30	3487	RTLS, 2-way ranging scheme, Long Range, Low Density
Mode 4	6.8 Mbps	16	128	30	173	RTLS, 2-way ranging scheme, Short Range, High Density
Mode 5	6.8 Mbps	16	1024	1023	1339	Data transfer, Short Range, Long Payload
Mode 6	6.8 Mbps	16	128	127	287	Data transfer, Short Range, Short Payload
Mode 7	110 kbps	16	1024	1023	78099	Data transfer, Long Range, Long Payload
Mode 8	110 kbps	16	128	127	10730	Data transfer, Long Range, Short Payload
Mode 9	110 kbps	64	1024	12	2084	As Mode 1 using 64 MHz PRF
Mode 10	6.8 Mbps	64	128	12	152	As Mode 2 using 64 MHz PRF
Mode 11	110 kbps	64	1024	30	3487	As Mode 3 using 64 MHz PRF
Mode 12	6.8 Mbps	64	128	30	173	As Mode 4 using 64 MHz PRF
Mode 13	6.8 Mbps	64	1024	1023	1339	As Mode 5 using 64 MHz PRF
Mode 14	6.8 Mbps	64	128	127	287	As Mode 6 using 64 MHz PRF
Mode 15	110 kbps	64	1024	1023	78099	As Mode 7 using 64 MHz PRF
Mode 16	110 kbps	64	128	127	10730	As Mode 8 using 64 MHz PRF
Note: Other modes are possible						

Table 24: Operational Modes

T_{amb} = 25 ˚C, All supplies centered on typical values. All currents referenced to 3.3 V

Mode Name	TX I_{AVG} (mA)		RX I_{AVG} (mA)		Units
	Channel 2	Channel 5	Channel 2	Channel 5	
Mode 1	42	47	86	92	mA
Mode 2	52	58	115	122	mA
Mode 3	38	43	76	81	mA
Mode 4	52	58	115	123	mA
Mode 5	50	56	118	126	mA
Mode 6	51	57	116	125	mA
Mode 7	32	36	60	65	mA
Mode 8	33	38	64	70	mA
Mode 9	55	60	98	105	mA
Mode 10	73	79	114	122	mA
Mode 11	49	54	91	98	mA
Mode 12	76	81	115	123	mA
Mode 13	91	97	118	126	mA
Mode 14	83	88	116	124	mA
Mode 15	40	44	82	88	mA
Mode 16	42	47	85	91	mA

Table 25: Typical Current Consumption

6.3.1 Typical transmit profile

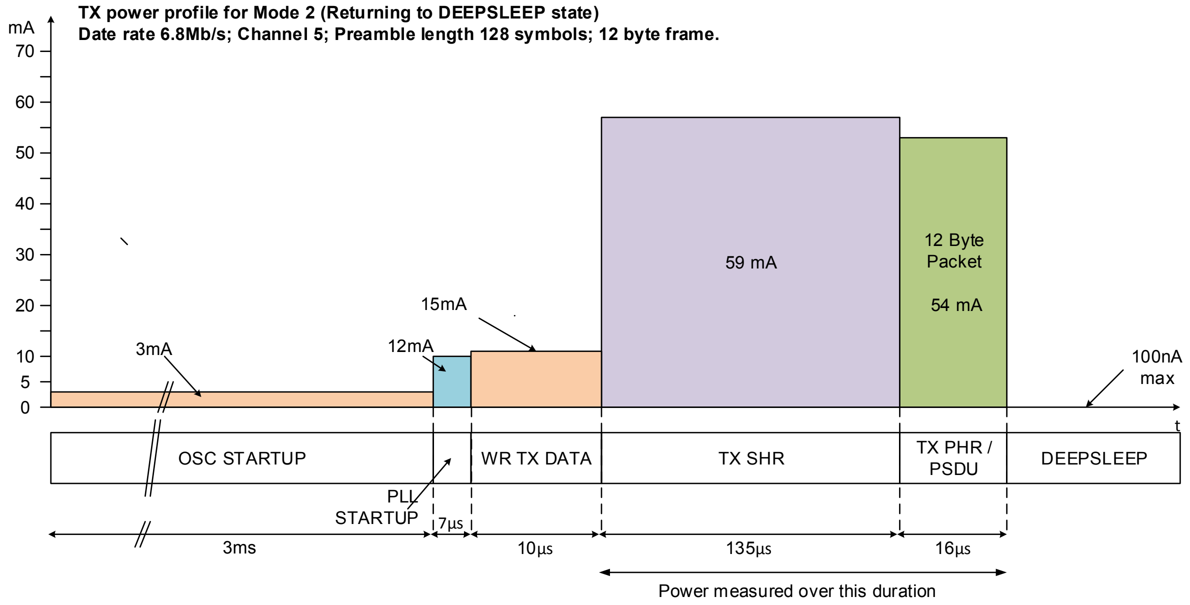


Figure 30: Typical TX Power Profile

6.3.2 Typical receive profiles

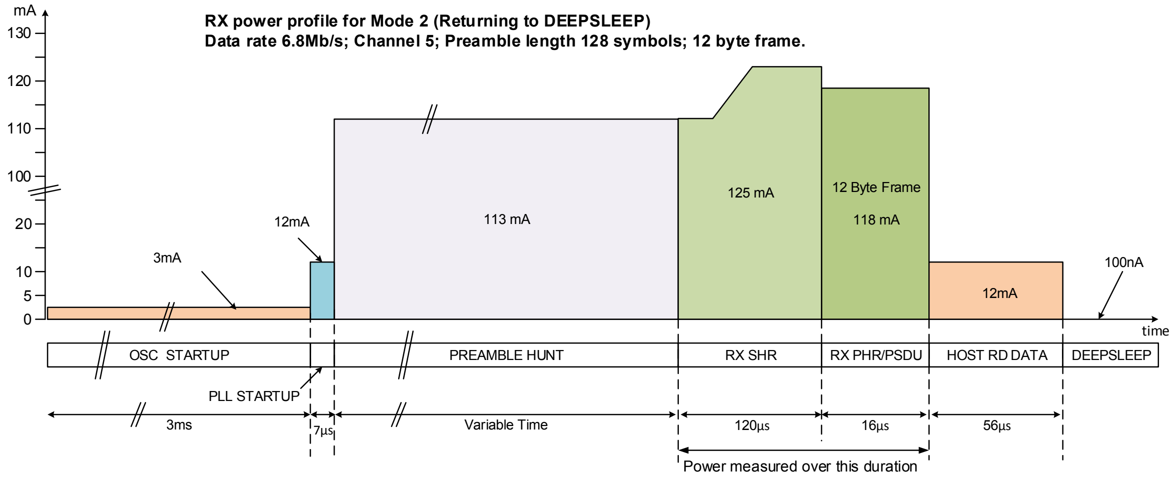


Figure 31: Typical RX Power Profile

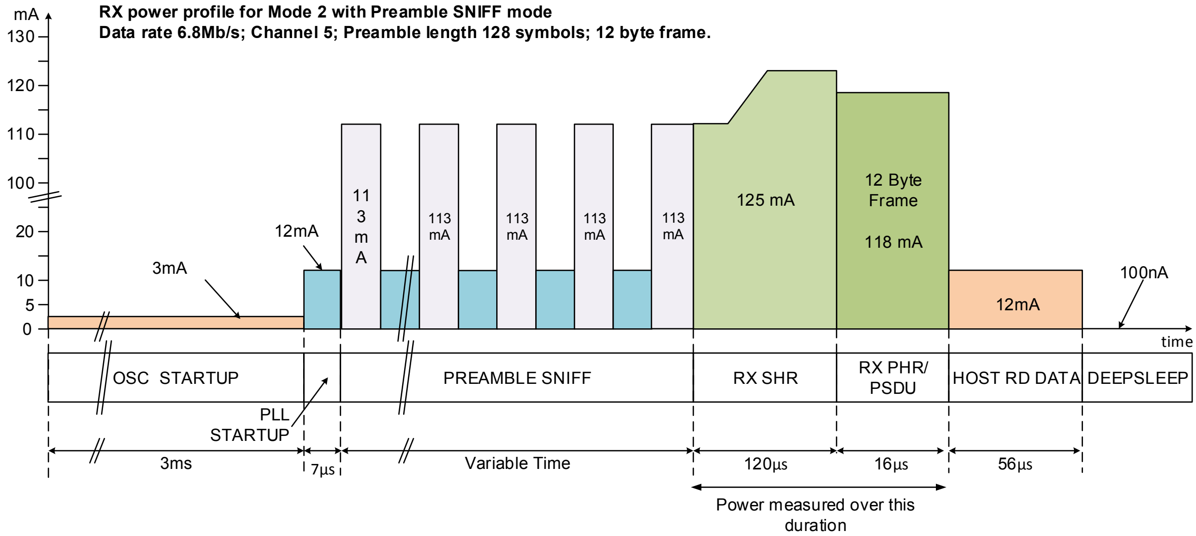


Figure 32: Typical RX Power Profile using SNIFF mode

7 Power Supply

7.1 Power Supply Connections

There are a number of different power supply connections to the DW1000.

The chip operates from a nominal 3.3 V supply. Some circuits in the chip are directly connected to the external 3.3 V supply. Other circuits are fed from a number of on-chip low-dropout regulators. The outputs of these LDO regulators are brought out to pins of the chip for decoupling purposes. Refer to Figure 33 for further details.

The majority of the supplies are used in the analog & RF section of the chip where it is important to maintain supply isolation between individual circuits to achieve the required performance.

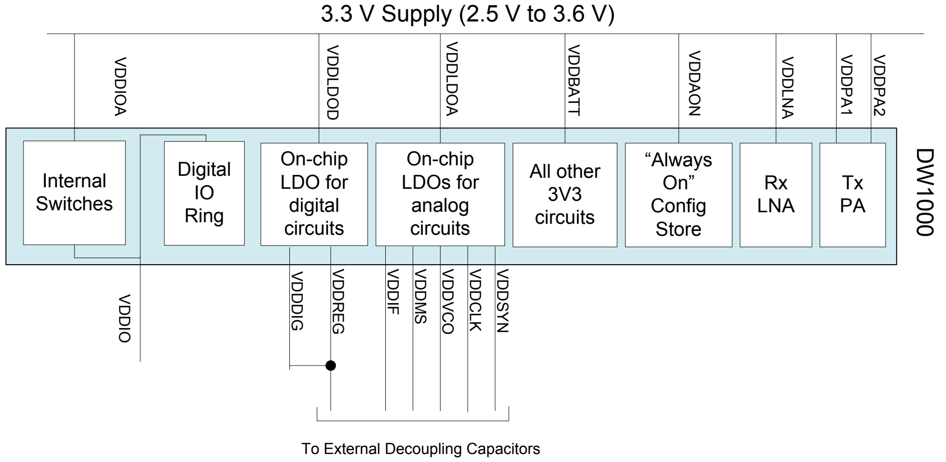


Figure 33: Power Supply Connections

7.2 Use of External DC / DC Converter

The DW1000 supports the use of external switching regulators to reduce overall power consumption from the power source. Using switching regulators can reduce system power consumption. The EXTON pin can be used to further reduce power by disabling the external regulator when the DW1000 is in the SLEEP or DEEPSLEEP states (provided the EXTON turn on time is sufficient).

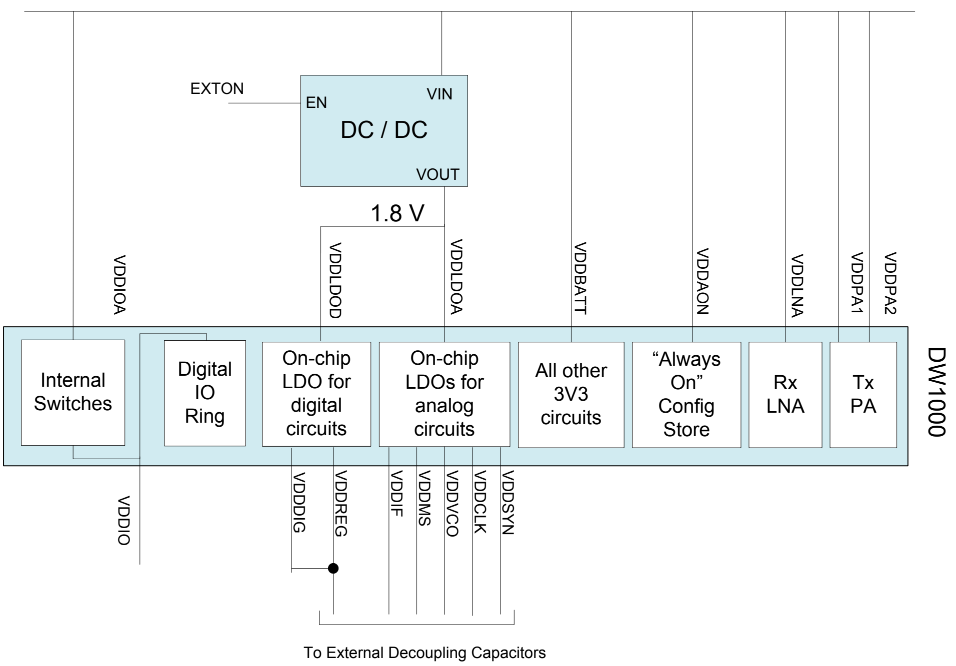


Figure 34: Switching Regulator Connection

8 APPLICATION INFORMATION

8.1 Application Circuit Diagram

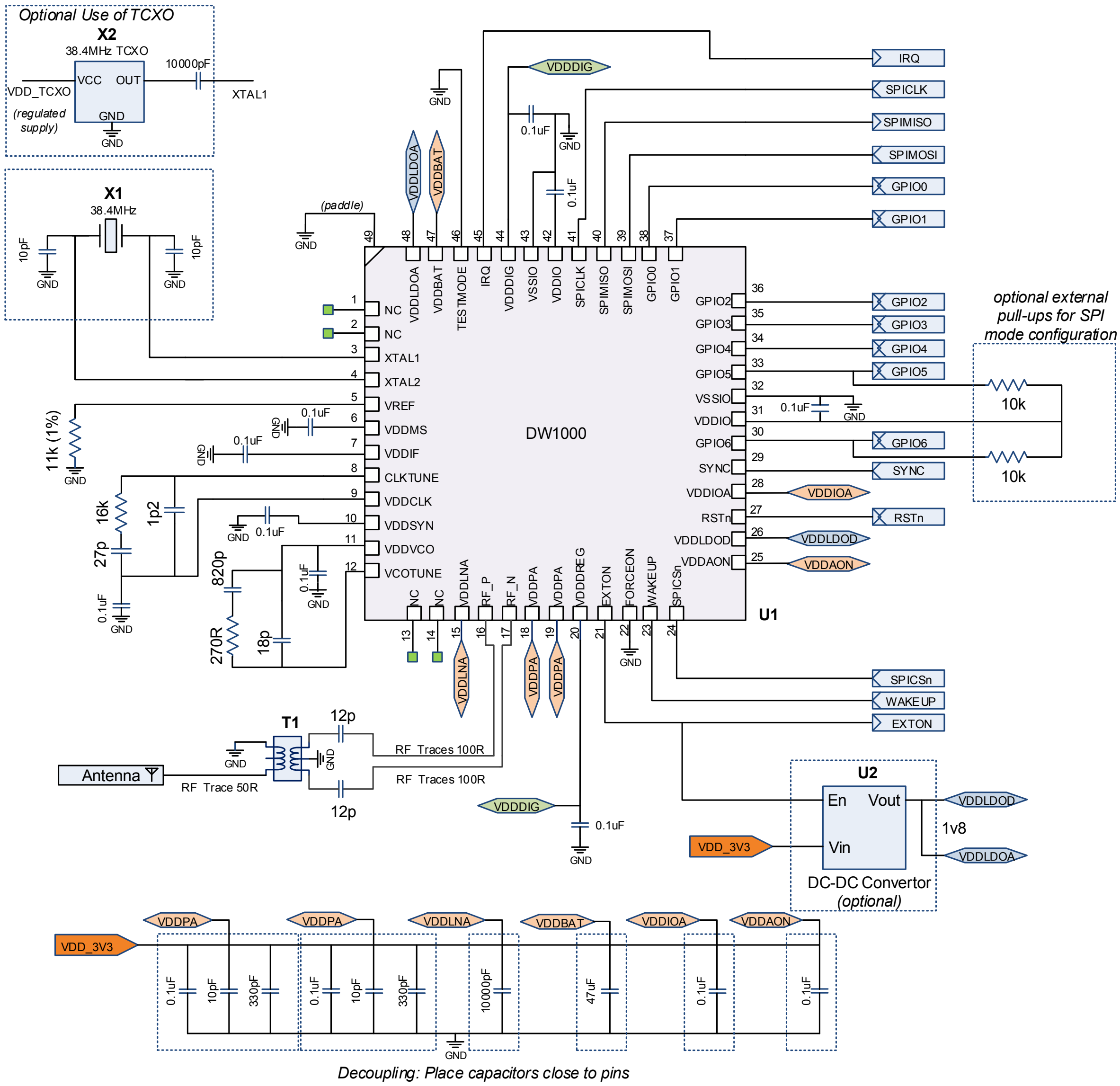


Figure 35: DW1000 Application Circuit

8.2 Recommended Components

Function	Manufacturer	Part No	Ref	Web Link
Antenna	Taiyo Yuden	AH086M555003		www.yuden.co.jp
SMT UWB Balun 3-8 GHz	TDK Corporation	HHM1595A1	T1	http://www.tdk.co.jp/
Capacitors (Non polarized)	Murata	GRM155 series		www.murata.com
	KEMET	C0805C476M9P ACTU	47 µF	capacitoredge.kemet.com
Crystal (38.4 MHz +/-10ppm)	Rakon	HDD10RSX-10 509344	X1	www.rakon.com
	Geyer	KX-5T (need to request tight tolerance option)		www.geyer-electronic.de
	TXC	7L Series		www.txccrystal.com

Function	Manufacturer	Part No	Ref	Web Link
DC/DC	Murata	LXDC2HL_18A	U2	www.murata.com
Resistors	ROHM	MCR01MZPF		www.rohm.com
TCXO (optional use in Anchor nodes. 38.4MHz)	Rakon	IVT2205AE	X2	www.rakon.com
	Geyer	KXO-84		www.geyer-electronic.de

8.3 Application Circuit Layout

8.3.1 PCB Stack

To achieve optimum performance a 4-layer PCB with the following layer-stack, copper deposition and thicknesses is recommended.

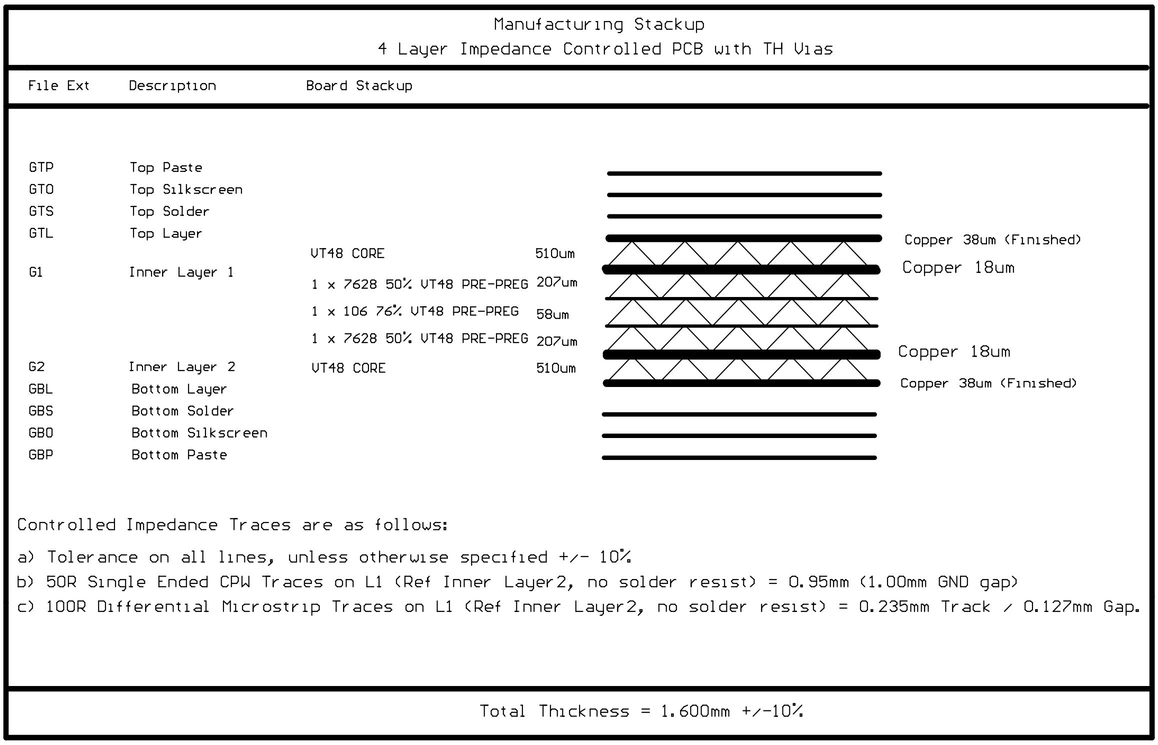


Figure 36: PCB Layer Stack for 4-layer board

8.3.2 RF Traces

As with all high frequency designs, particular care should be taken with the routing and matching of the RF sections of the PCB layout. All RF traces should be kept as short as possible and where possible impedance discontinuities should be avoided.

Poor RF matching of signals to/from the antenna will degrade system performance. A 100 Ω differential impedance should be presented to the RF_P and RF_N pins of DW1000 for optimal performance. This can be realised as either 100 Ω differential RF traces or as 2 single-ended 50 Ω traces depending on the PCB layout. In most cases a single-ended antenna will be used and a wideband balun will be required to convert from 100 Ω differential to 50 Ω single-ended.

Figure 37 gives an example of a suggested RF section layout. In this example traces to the 12 pF series capacitors from the RF_P and RF_N pins are realised as 100 Ω differential RF traces referenced to inner layer 1. After the 12 pF capacitors the traces are realized as 50 Ω micro-strip traces again referenced to inner layer 1. Using this method, thin traces can be used to connect to DW1000 and then wider traces can be used to connect to the antenna.

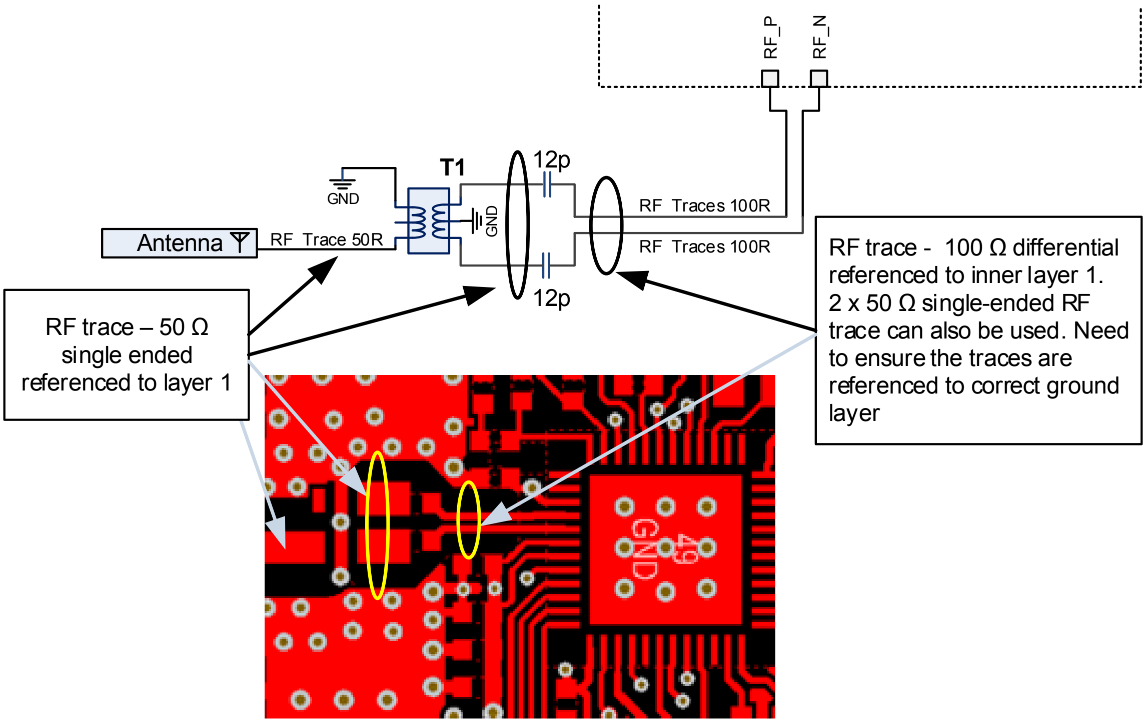


Figure 37: DW1000 RF Traces Layout

8.3.3 PLL Loop Filter Layout

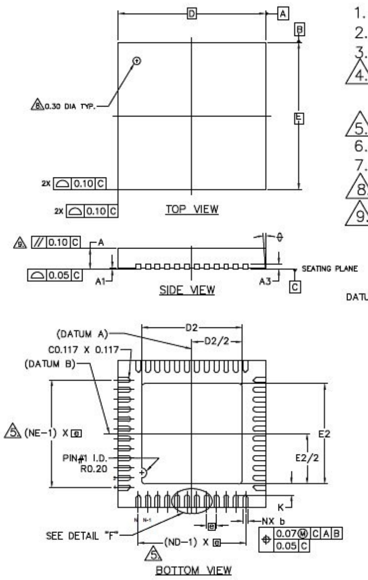
The components associated with the loop filters of the on-chip PLLs should be placed as close as possible to the chip connection pins to minimize noise pick-up on these lines.

8.3.4 Decoupling Layout

All decoupling capacitors should be kept as close to their respective pins of the chip as possible to minimize trace inductance and maximize their effectiveness.

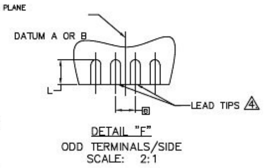
9 PACKAGING & ORDERING INFORMATION

9.1 Package Dimensions



NOTES :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.



SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
A3	0.203 REF.			
θ	0°	——	12°	2
K	0.20	——	——	10
e	0.40 BSC.			
N	48			3
ND	12			5
ND	12			5
L	0.45	0.50	0.55	11
b	0.15	0.20	0.25	4
D2	4.00	4.10	4.20	
E2	4.00	4.10	4.20	
D	6.00 BSC			
E	6.00 BSC			

Figure 38: Device Package mechanical specifications

9.2 Device Package Marking

The diagram below shows the package markings for DW1000.

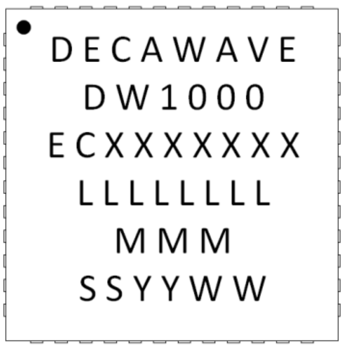


Figure 39: Device Package Markings

Legend:

ECXXXXXXX	10 digit product number
LLLLLLLL	8 digit lot ID
MMM	3 digit mask ID
SS	Assembly location
YY	2 digit year number
WW	2 digit week number

9.3 Tray Information

The general orientation of the 48QFN package in the tray is as shown in Figure 40.

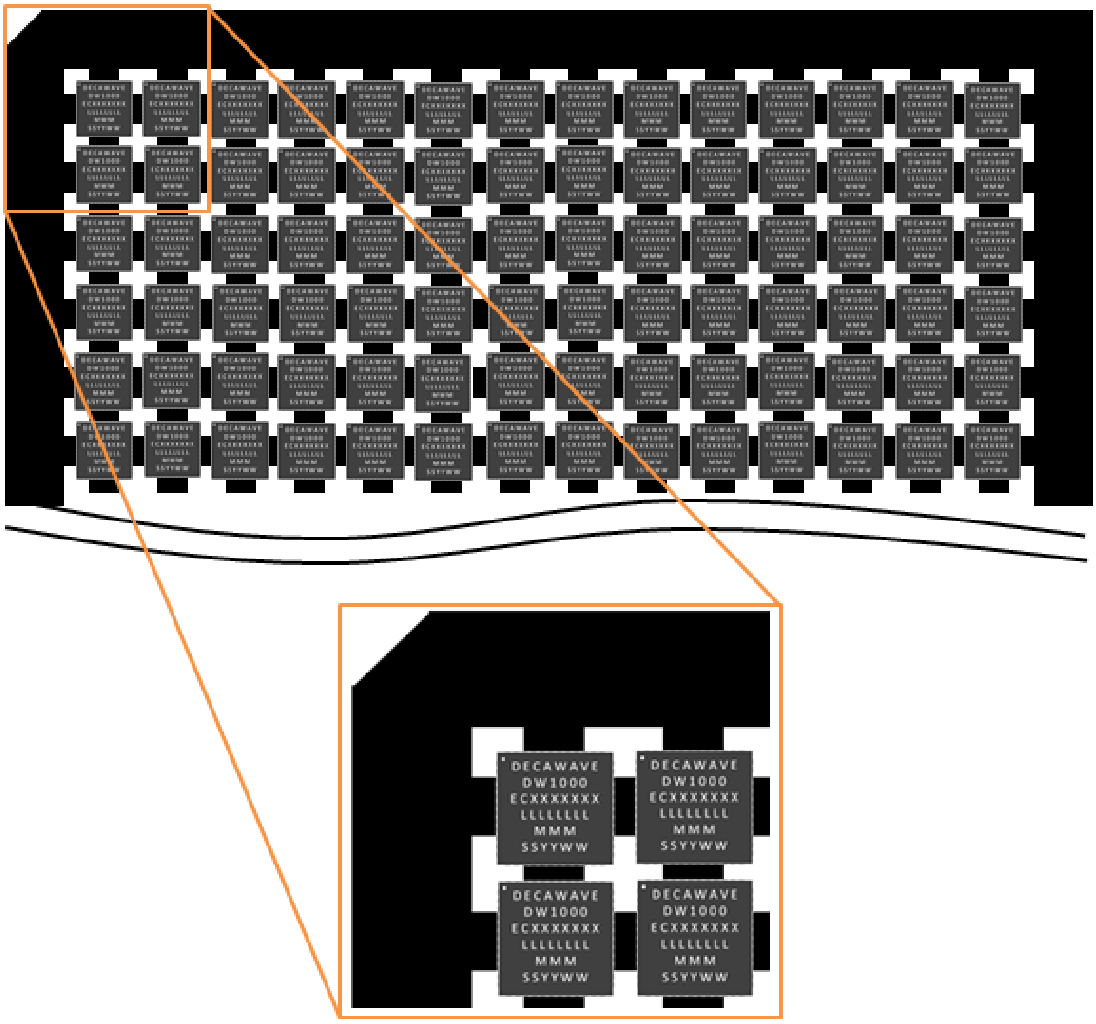


Figure 40: Tray Orientation

The white dot marking in the chips top left hand corner aligns with the chamfered edge of the tray.

9.4 Tape & Reel Information

9.4.1 Tape Orientation and Dimensions

The general orientation of the 48QFN package in the tape is as shown in Figure 41.

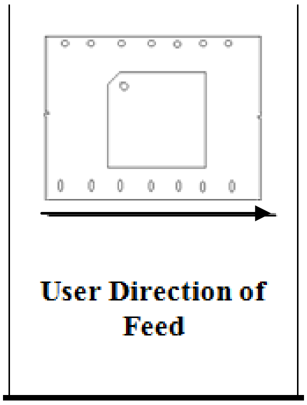


Figure 41: Tape & Reel orientation

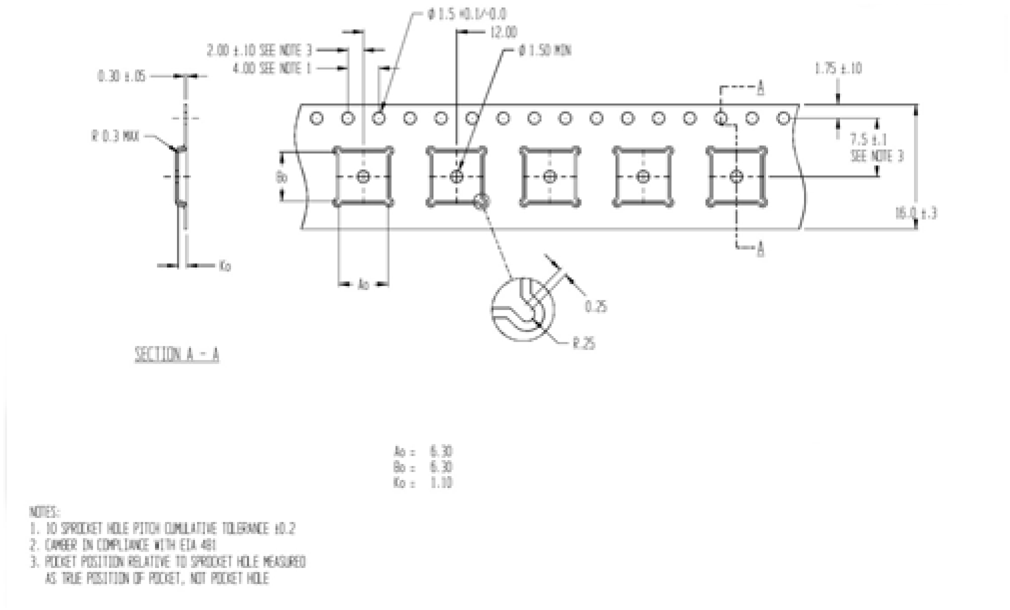


Figure 42: Tape dimensions

9.4.2 Reel Information: 330 mm Reel

Base material: High Impact Polystyrene with Integrated Antistatic Additive
Surface resistivity: Antistatic with surface resistivity less than 1 x 10e[12] Ohms per square

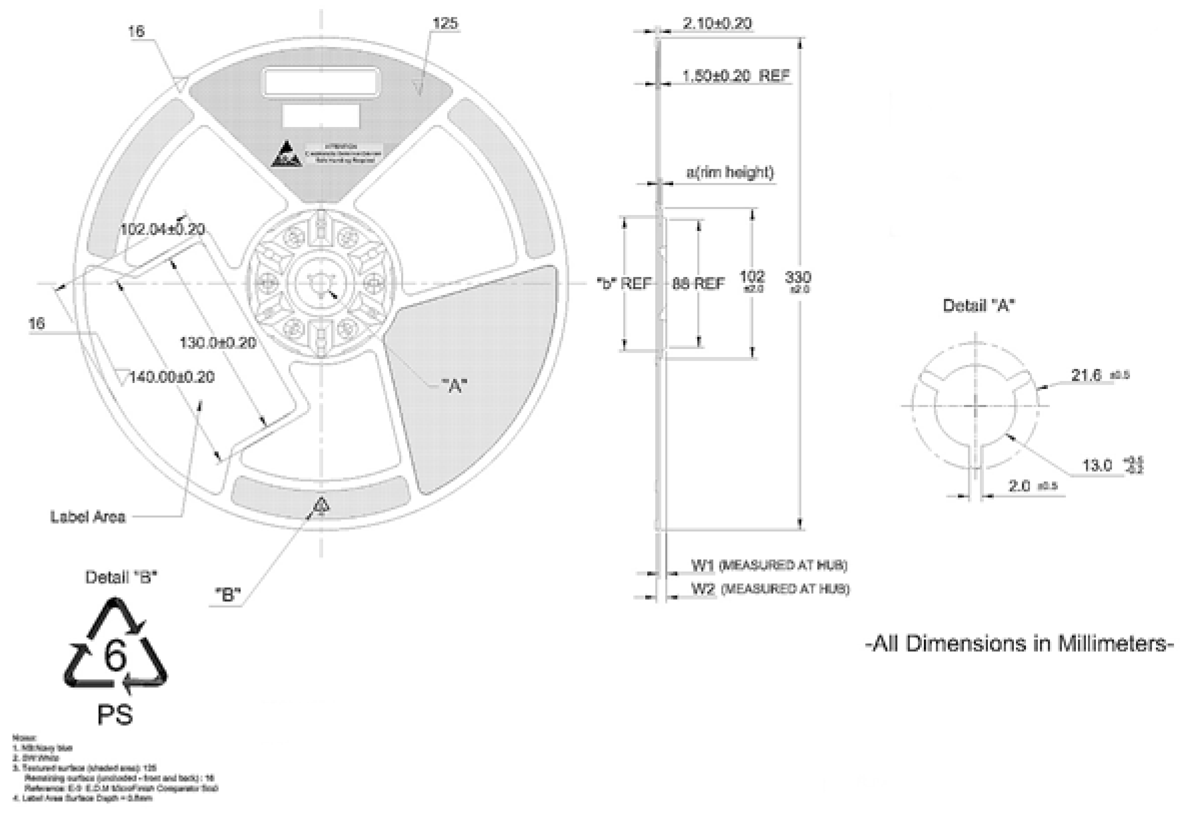


Figure 43: 330 mm reel dimensions

All dimensions and tolerances are fully compliant with EIA- 481-C and are specified in millimetres.

9.4.3 Reel Information: 180 mm reel

Base material: High impact polystyrene with integrated antistatic additive.
Surface resistivity: Antistatic with surface resistivity less than 1 x 10e^{12} Ohms per square.

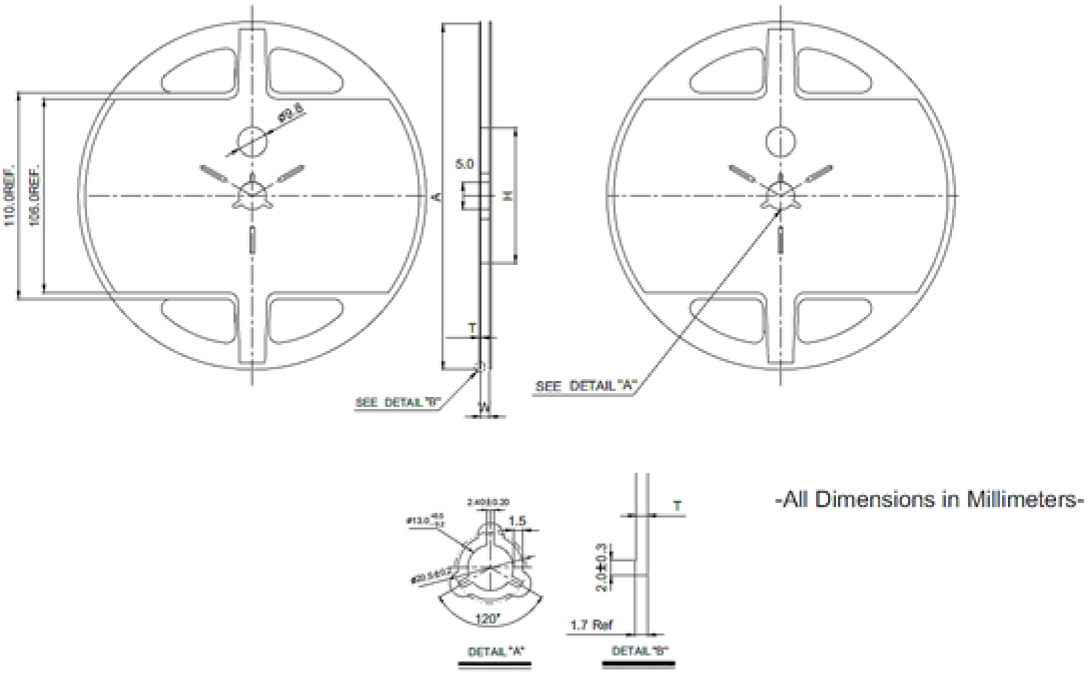


Figure 44: 180 mm reel dimensions

All dimensions and tolerances are fully compliant with EIA- 481-C and are specified in millimetres.

9.5 Ordering Information

The standard qualification for the DW1000 is industrial temperature range: -40 ºC to +85 ºC, packaged in a 48-pin QFN package.

Ordering Codes:

High Volume

Ordering code	Status	Package Type	Package Qty	Note
DW1000-I	Active	Tray	490	Available
DW1000-ITR7	Active	Tape & Reel	1000	Available
DW1000-ITR13	Active	Tape & Reel	4000	Available

Samples

Ordering Code	Status	Package Type	Package Qty	Note
DW1000-I	Active	Tray	10-490	Available
DW1000-ITR7	Active	Tape & Reel	100 - 1000	Available
DW1000-ITR13	Active	Tape & Reel	100 - 4000	Available

Table 26: Device ordering information

All IC's are packaged in a 48-pin QFN package which is Pb free, RoHS, Green, NiPd lead finish, MSL level 3
IC Operation Temperature -40 ºC to +85 ºC.

10 GLOSSARY

Abbreviation	Full Title	Explanation
EIRP	Equivalent Isotropically Radiated Power	The amount of power that a theoretical isotropic antenna (which evenly distributes power in all directions) would emit to produce the peak power density observed in the direction of maximum gain of the antenna being used
ETSI	European Telecommunication Standards Institute	Regulatory body in the EU charged with the management of the radio spectrum and the setting of regulations for devices that use it
FCC	Federal Communications Commission	Regulatory body in the USA charged with the management of the radio spectrum and the setting of regulations for devices that use it
FFD	Full Function Device	Defined in the context of the IEEE802.15.4-2011 [1] standard
GPIO	General Purpose Input / Output	Pin of an IC that can be configured as an input or output under software control and has no specifically identified function
IEEE	Institute of Electrical and Electronic Engineers	Is the world's largest technical professional society. It is designed to serve professionals involved in all aspects of the electrical, electronic and computing fields and related areas of science and technology
LIFS	Long Inter-Frame Spacing	Defined in the context of the IEEE802.15.4-2011 [1] standard
LNA	Low Noise Amplifier	Circuit normally found at the front-end of a radio receiver designed to amplify very low level signals while keeping any added noise to as low a level as possible
LOS	Line of Sight	Physical radio channel configuration in which there is a direct line of sight between the transmitter and the receiver
NLOS	Non Line of Sight	Physical radio channel configuration in which there is no direct line of sight between the transmitter and the receiver
PGA	Programmable Gain Amplifier	Amplifier whose gain can be set / changed via a control mechanism usually by changing register values
PLL	Phase Locked Loop	Circuit designed to generate a signal at a particular frequency whose phase is related to an incoming "reference" signal.
PPM	Parts Per Million	Used to quantify very small relative proportions. Just as 1% is one out of a hundred, 1 ppm is one part in a million
RF	Radio Frequency	Generally used to refer to signals in the range of 3 kHz to 300 GHz. In the context of a radio receiver, the term is generally used to refer to circuits in a receiver before down-conversion takes place and in a transmitter after up-conversion takes place
RFD	Reduced Function Device	Defined in the context of the IEEE802.15.4-2011 [1] standard
RTLS	Real Time Location System	System intended to provide information on the location of various items in real-time.
SFD	Start of Frame Delimiter	Defined in the context of the IEEE802.15.4-2011 [1] standard.
SIFS	Short Inter-Frame Spacing	Defined in the context of the IEEE802.15.4-2011 [1] standard.
SPI	Serial Peripheral Interface	An industry standard method for interfacing between IC's using a synchronous serial scheme first introduced by Motorola
TCXO	Temperature Controlled Crystal Oscillator	A crystal oscillator whose output frequency is very accurately maintained at its specified value over its specified temperature range of operation.
TWR	Two Way Ranging	Method of measuring the physical distance between two radio units by exchanging messages between the units and noting the times of transmission and reception. Refer to DecaWave's website for further information
TDOA	Time Difference of Arrival	Method of deriving information on the location of a transmitter. The time of arrival of a transmission at two physically different locations whose clocks are synchronized is noted and the difference in the arrival times provides information on the location of the transmitter. A number of such TDOA measurements at different locations can be used to uniquely determine the position of the transmitter. Refer to DecaWave's website for further information.
UWB	Ultra Wideband	A radio scheme employing channel bandwidths of, or in excess of, 500MHz
WSN	Wireless Sensor Network	A network of wireless nodes intended to enable the monitoring and control of the physical environment

Table 27: Glossary of Terms

11 REFERENCES

[1] IEEE802.15.4-2011 or “IEEE Std 802.15.4™-2011” (Revision of IEEE Std 802.15.4-2006). IEEE Standard for Local and metropolitan area networks - Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs). IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from http://standards.ieee.org/

[2] DecaWave DW1000 User Manual www.decawave.com

[3] www.etsi.org

[4] www.fcc.gov

[5] EIA-481-C Standard

Document History

Revision	Date	Description
2.00	7th November 2012	Initial release for production device.

Table 28: Document History

About DecaWave

DecaWave is a pioneering fabless semiconductor company whose flagship product, the DW1000, is a complete, single chip CMOS Ultra-Wideband IC based on the IEEE 802.15.4-2011 [1] UWB standard. This device is the first in a family of parts that will operate at data rates of 110 kbps, 850 kbps, 6.8 Mbps.

The resulting silicon has a wide range of standards-based applications for both Real Time Location Systems (RTLS) and Ultra Low Power Wireless Transceivers in areas as diverse as manufacturing, healthcare, lighting, security, transport, inventory & supply chain management.

Further Information

For further information on this or any other DecaWave product contact a sales representative as follows: -

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w: www.decawave.com

DOCUMENT INFORMATION

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