# CA HW 5

| Inst # | Original Code | Renamed Code | Spec. Reg Map | InQ | Issued | Completed | Commit | Committed Map Reg | Free Reg List |
|---|---|---|---|---|---|---|---|---|---|
| 1. | LD LR1, 0(LR2) | LD PR33, 0(PR2) | LR1 → PR33 | i | i+1 | i+7 | i+7 | LR1 → PR33 | PR1 |
| 2. | DADD LR1, LR1, LR3 | DADD PR34, PR33, PR3 | LR1 → PR34 | i | i+3 | i+8 | i+8 | LR1 → PR34 | PR33 |
| 3 | ST.D LR1, 0(LR5) | ST.D PR34, 0(PR5) | — | i | i+4 | i+10 | i+10 | — | — |
| 4 | DADD LR2, LR2, 8 | DADD PR35, PR2, 8 | LR2 → PR35 | i+1 ■ | i+2 | i+7 | i+10 ● | LR2 → PR35 | PR2 |
| 5 | DADD LR5, LR5, 8 | DADD PR36, PR5, 8 | LR5 → PR36 | i+1 | i+2 | i+7 | i+10 ● | LR5 → PR36 | PR5 |
| 6 | BNE LR2, LR4, line 1 | BNE PR35, PR4, line 1 | — | i+1 | i+3 | i+8 | i+11 ★ | — | — |
| 7 | LD LR1, 0(LR2) | LD PR37, 0(PR35) | LR1 → PR37 | i+2 ■ | i+3 | i+9 | i+11 ● | LR1 → PR37 | PR34 |
| 8 | DADD LR1, LR1, LR3 | DADD PR38, PR37, PR3 | LR1 → P38 | i+2 | i+5 | i+10 | i+11 ● | LR1 → PR38 | PR37 |
| 9 | ST.D LR1, 0(LR5) | ST.D PR38, 0(PR36) | — | i+2 | i+6 | i+12 | i+12 | — | — |
| 10 | DADD LR2, LR2, 8 | DADD PR1, PR35, 8 | LR2 → PR1 | i+8 ▲ | i+9 | i+14 | i+14 | LR2 → PR1 | PR35 |
| 11 | DADD LR5, LR5, 8 | DADD PR33, PR36, 8 | LR5 → PR33 | i+9 ▲ | i+10 | i+15 | i+15 | LR5 → PR33 | PR36 |
| 12 | BNE LR2, LR4, line 1 | BNE PR1, PR4, line 1 | — | i+9 | i+10 | i+15 | i+15 | — | — |

Logical Regs = 32
Physical Regs. = 38
Free list = PR33 – PR38

■ : Fetch width full, Fetched in next cycle
▲ : No free registers in Free Reg List: waiting till PR is free
● : Commit delayed in order to commit in order
★ : Commit width full, committed in next cycle.
→ : Represent dependencies