1 Loop Unnolling and SW Pipelining. gree LD > any : 3 Stalls

FPMUL + any: 6 stalls

FPMUL +ST : 5 stalls

INTALU → BR : 2 stalls

INTALU - any: Istall:

BR -> 1 delay slot.

4) Schedule for default code: -

LOOP: LD F2, O(RI)

LD F4, O(R2)

Stall Stall

. Stall

MUL.D F2, F2, F4

Stall

Stall "

Stall

Stall . .

Stall

5D F2, O(R1)

DADDUI RI, RI, #=8

DADDUI R2, R2, #-8

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BNE RI, R3, LOOP Stall

.. This takes a total of 17 cycles.

2) To minimize stalls, we can go for smart scheduling. LD F2; 0(R1) LOOP: LD F4, 0 (R2) DADDUI RI, RI, #-8 DADDUI R2, R2, # -8 Stall MUL. D F2, F2, F4 Stall Stall Stall Stall BNE RI, R3, LOOP SD FZ, 8(R1) This requires a total of 12 cycles. Hence, compared to the default schedule, we can save 5 cycles per iteration. 3> default cycle = 17 no. of cycles worth of work = 4 100p overheads = 3 Hence the min unrioll degree to eliminate stall eycles=4 : 4x4+3 = 19 cycles. LD F2, O(R) LOOP: LD FY, O(R2). 5D F2, 32(R1) LD P6, -8 (R1) SD F6, 24 (R) LD F8, -8(R2) SD FID, 16 (R1) D F10, -16(R1). BNE RI, R3, LOOP LD FIR , -16 (RZ) W FIM, -24(RI) SD F14, 8(R1) LD F16, -24(R2) MUL. D F2, F2, F4 MUL-D F6, F6, F8 MUL-D FID, FID, FIZ MUL D FIY, FIY, FI6 DADDUI RI, RI, #-32 DADDUI R2, R2, #-32

Software - pipelined version LOOP: 5D F2 , 16(R1) MUC. D F2, F2, F4 LD F4, O(R2) LD F2, 0(R1) DADDUI R2, R2, #-8 BNE RI, R3, LOOP DADDUI RI, RI, #-8 When this code executes, it won't experience any stalls. since each instruction is executed in a cycle and that it feeds to an instruction in the next cycle as different instructions belonging to differenct and execute in the same iteration. (2) Branch Predictors Ginen: Tournament branch predictors. capacity of selector = 32K x 3b = 98304 b - 96kb Capacity of global predictors = 3b x 215 = 983045 = 96kb capacity of local predictor = (12x27) + (21/x2b) = 1536 + 131072 = 132 608P = 129.5 kb Total capacity = 96+ 96+129.5 = [321.5 Kb]