CA HW7

1) Given: OS page size = 16kB, LLC size = 64MB, block size = 64B
32-way set-associative.

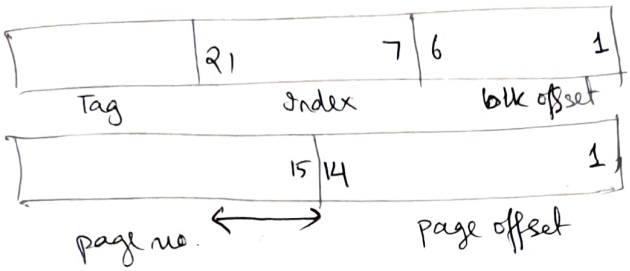
As page size = 16kB = 2^{14}B, page-offset will have 14 bits

Now size of 1 set = 64B × 32 = 2048B = 2^{11}B

Hence no. of sets = $\frac{64MB}{2048B} = \frac{2^{26}}{2^{11}} = 2^{15}$ sets = 32K sets.

⇒ no. of index bits for 2^{15} sets = 15 bits.

No. of block offset bits for block size of 64B i.e 2^6B = 6 bits



The bits 15-21 i.e 7 bits will give us the no. of tiles.
Hence the max no. of tiles such that OS has full flexibility in placing a page in a tile of its choosing = 2^7 = 128 tiles

2) Given - page size = 8KB, L1 → 4-way set associative.

Since page size is 8KB = 2^{13}B, the page offset will have 13 bits.

Now since it's a virtually indexed physically tagged cache, the sum of index and block offset bits should be equal to page offset bits. i.e. index + blk offset = 13.

Now the largest L1 cache size = #sets × blk size × #ways.

= $2^{13} \times 2^2 = 2^{15}$B = 32KB

3) Capacity = 1TB, ranks = 64, banks = 16
row in bank = 8KB, 50 ns to refresh each row.
refresh rate = 64ms, refresh command in every 7.8µs. (8192 cycle/64ms)

rows = $\frac{1TB}{8KB} = \frac{2^{40}}{2^3} = 2^{37}$ rows

We need # rows per bank.

Now rank size = $\frac{1TB}{64} = \frac{2^{40}}{2^6} = 2^{34}B$

$\Rightarrow$ bank size = $\frac{2^{34}}{16} = \frac{2^{34}}{2^4} = 2^{30}$ B.

Hence # rows = $\frac{\text{bank size}}{\text{row size}} = \frac{2^{30}}{8KB} = \frac{2^{30}}{2^{13}} = 2^{17}$

$\therefore$ There are 2^{17} rows in a bank.

$\Rightarrow$ No. of rows to be refreshed every command in a bank $= \frac{2^{17}}{2^{13}} = 2^4$ rows

$= 16$ rows.

Now time taken to refresh 16 rows = 16×50 ns.

$= 800$ ns.

Now fraction of time memory system is unavailable performing refresh = $\frac{800 \times 10^{-9}}{7.8 \times 10^{-6}} = 102.56 \times 10^{-3}$ = 10.256 % of time.

5)

Row being accessed	Arrival Time	Open-Page	Close-Page
X	15 ns.	55	55 → 75 (close)
X	65 ns	85	115
Y	90 ns.	150	195 → 215 (close)
X	95 ns.	210	135
Y	260 ns	320	300 → 320 (close)
Y	310 ns.	340	360

3) Given: 2 sockets, 4 DDR4 mem channels, each channel → 4 ranks

For max. capacity, we will consider DRAM chip with 8 Gb capacity and with data output width of 16.

Max capacity supported = 2 sockets × 4 mem channels × 4 ranks × 16 × 8 Gb

$= 2 \times 2^2 \times 2^2 \times 2^4 \times 2^{33} = 2^{42}$ Gb = 2^{39} B = 512 GB

Memory bandwidth = $2 \times 4 \times 1.2 GHz \times 2 \times 64 = 1228.8$ Gb/s

= 153.6 GB/s