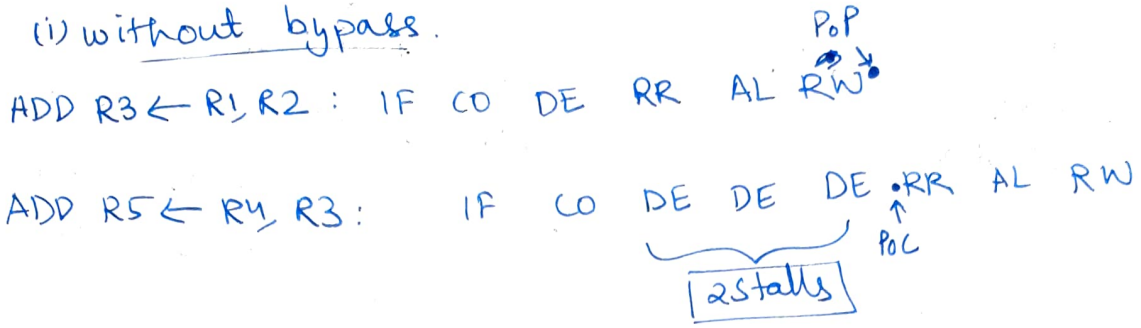
CA Assignment -3

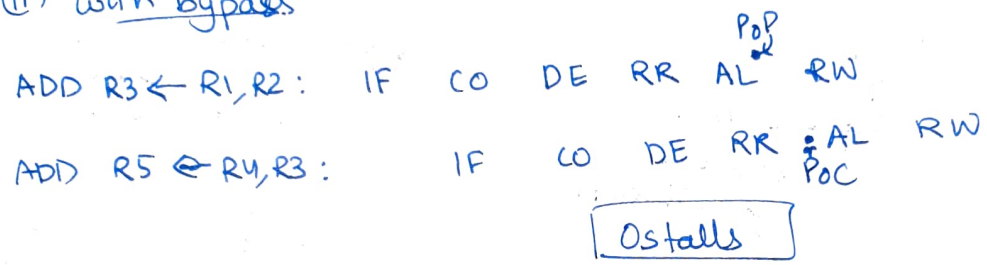
1. Data Dependences.

1) ADD R3 ← R1, R2
   ADD R5 ← R4, R3

(i) without bypass.

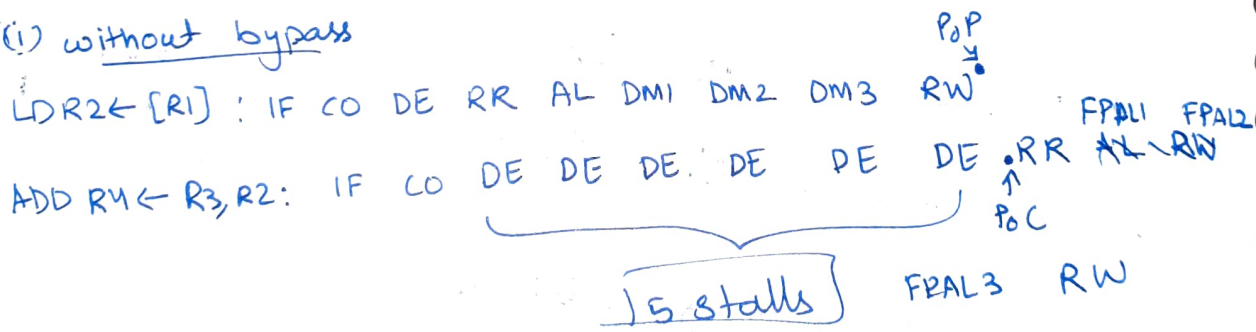


(ii) with bypass

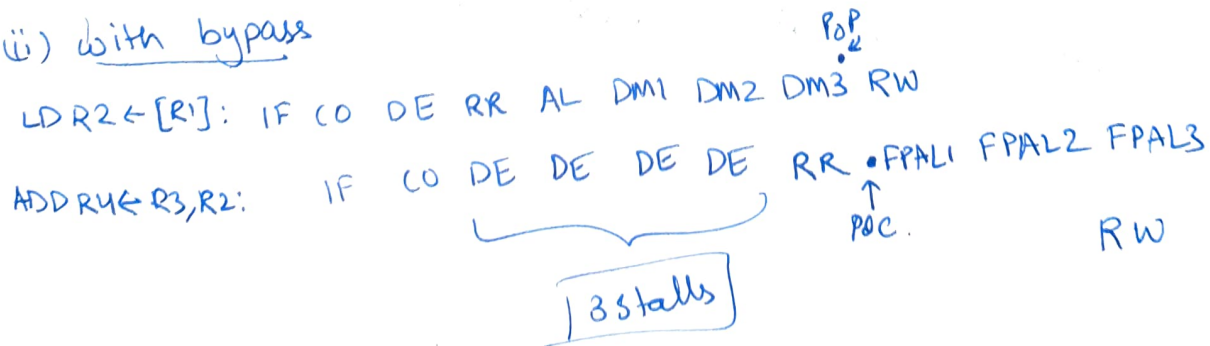


2) LD R2 ← [R1]
   ADD R4 ← R3, R2

(i) without bypass

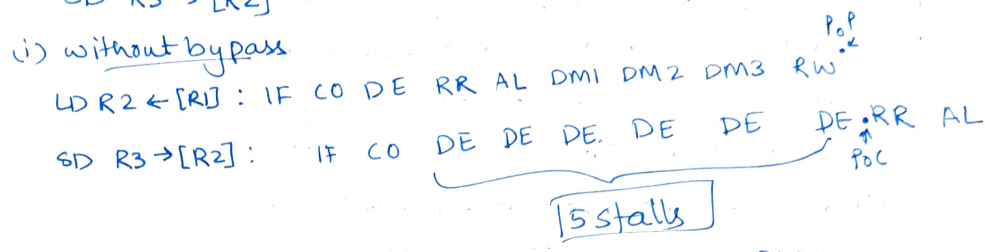


(ii) with bypass

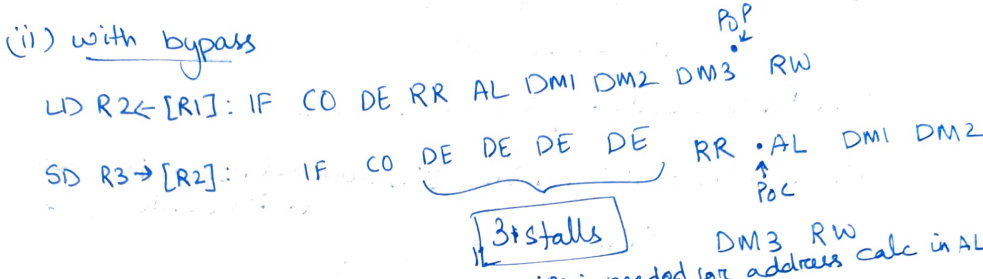


3) LD R2 ← [R1]
SD R3 → [R2]

(i) without bypass

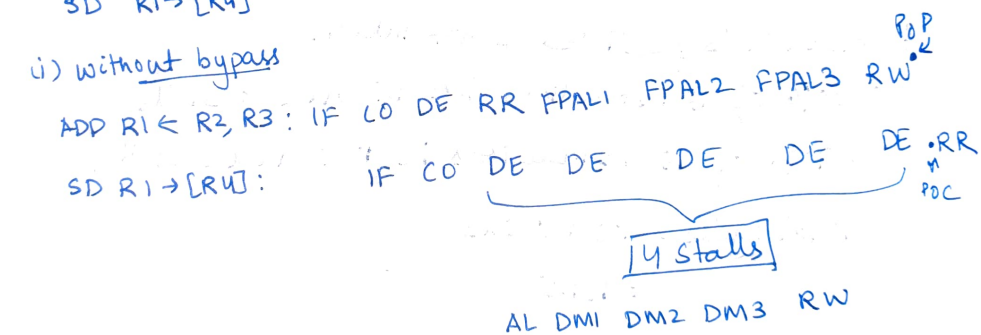


(ii) with bypass

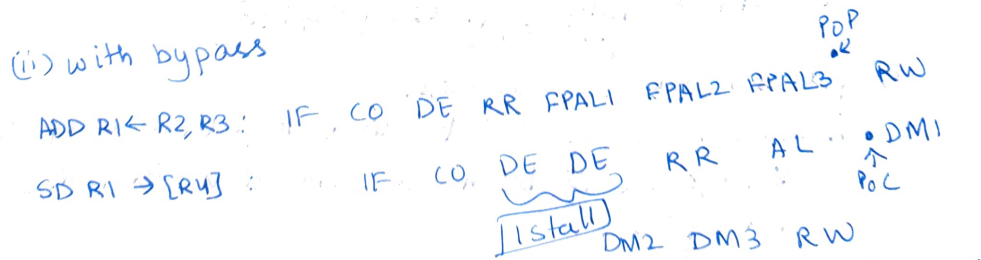


4) ADR R1 ← R2, R3
SD R1 → [R4]

(i) without bypass



(ii) with bypass



∵ R1 is needed to get data to be put in memory

2. Branch delay slots and stalls

Given:- 10-stage-in-order processor.

branch outcome after 4 stages - 3 stall cycles.

branches = 15% of all instructions

branch taken - 70%, not taken - 30%

total cycles = # of instructions + stall cycles

Let total # of instructions be 100.

1) avg CPI = $\frac{\text{total cycles}}{\text{total instructions}}$.

when fetch is stalled for every branch.

total cycles = 100 + 15×3 [∵ 15 branched instruction each having 3 stall cycles]

= 145

avg CPI = $\frac{145}{100}$ = 1.45 cycles/inst^n

2) branch is predicted as not taken.

⇒ 30% of 15 instructions i.e 4.5 have no stalls

& 70% of 15 instructions i.e. 10.5 have 3 stalls.

total cycles = 100 + 10.5×3

= 131.5

avg CPI = $\frac{131.5}{100}$ = 1.315 cycles/inst^n

3) processor has 3 delay slots.

(i) Since there are no instructions to fill the delay slots, each of the 15 branched instruction will have 3 stall cycles.

avg CPI = $\frac{100+45}{100}$ = 1.45 cycles/inst^n

② 3 instructions before the branch moved into delay slot

⇒ no stall cycles introduced for the branches.

∴ avg CPI = $\frac{100}{100}$ = 1 cycle/instn

③ 3 instructions from the taken block moved into delay slot

⇒ 10.5 instructions of the branch instructions won't have any stall cycles

but 4.5 instructions will have 3 stall cycles.

avg CPI = $\frac{100 + 13.5}{100} = \frac{113.5}{100}$ = 1.135 cycles/instn

④ 3 instructions from the not-taken block moved into delay slot.

⇒ 10.5 instructions will have 3 stall cycles

avg CPI = $\frac{100 + 10.5 \times 3}{100} = \frac{100 + 31.5}{100} = \frac{131.5}{100}$

= 1.315 cycles/instn

3. Deep Pipelines

Given: unpipelined processor. To find: throughput in BIPS.

cycle time = 20 ns

Latch Latency = 0.2 ns

PoP ⇔ PoC = 6 ns.

independent instructions = 40%

dependent instructions = 60%.

(i) for unpipelined processor.

cycle time = 20 + 0.2 = 20.2 ns.

since unpipelined ⇒ throughput = $\frac{1}{20.2}$ = 0.049 BIPS

(ii) 10-stage pipeline.

time per stage = $\frac{20}{10} = 2$ ns.

$\Rightarrow$ cycle time = $2 + 0.2 = 2.2$ ns.

$\therefore$ gap between independent instructions = 2.2 ns

# of cycle shifts for gap between PoC & PoP = $\frac{6}{2} = 3$ stages.

$\therefore$ gap between dependent instructions = $3 \times 2.2 = 6.6$ ns

avg gap = $0.4 \times 2.2 + 0.6 \times 6.6 = 4.84$ ns.

$\therefore$ throughput = $\frac{1}{4.84}$ = **0.206 BIPS**

(iii) 20-stage pipeline

time per stage = $20/20 = 1$ ns

$\Rightarrow$ cycle time = 1.2 ns.

$\therefore$ gap between independent instructions = 1.2 ns

# of cycle shifts = $\frac{6}{1} = 6$ stages.

$\therefore$ gap between dependent instructions = $6 \times 1.2 = 7.2$ ns

avg gap = $0.4 \times 1.2 + 0.6 \times 7.2$

$= 4.8$ ns

$\therefore$ throughput = $\frac{1}{4.8}$ = **0.208 BIPS**