

CA Assignment -3

1. Data Dependences.

1) $\text{ADD } R3 \leftarrow R1, R2$
 $\text{ADD } R5 \leftarrow R4, R3$

(i) without bypass.

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ADD R3 ← R1, R2 : IF CO DE RR AL ^{POP} RW

ADD R5 ← R4, R3: IF CO DE DE DE ^{RR} AL RW
 ↑
 POC
 [2 stalls]

(ii) with bypass

ADD R3 \leftarrow R1, R2: IF CO DE RR AL^{POP} RW

ADD R5 ← R4, R3: IF CO DE RR AL POC RW

Ostalls

2) LD R2 ← [R1]
ADD R4 ← R3, R2

(i) without bypass

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LDR R2 ← [R1] : IF CO DE RR AL DM1 DM2 DM3 RW

LDR R2 ← [R1] : IF CO DE RR AL DM1 DM2 DM3 RW FPAL1 FPAL2
ADD R4 ← R3, R2: IF CO DE DE DE DE DE RR AL RW
5 stalls
FPAL3 RW

(ii) with bypass

ii) with bypass

LDR R2 ← [R1]: IF CO DE RR AL DM1 DM2 DM3 RW

Pop
↓

$LD R2 \leftarrow [R1]:$ IF CO DE DE DE DE RR \bullet FPAL1 FPAL2 FPAL3
 $ADD R4 \leftarrow R3, R2:$ IF CO DE DE DE DE RR \bullet FPAL1 FPAL2 FPAL3
 \uparrow
POC RW

3 stalls

3) LD R2 ← [R1]
SD R3 → [R2]

i) without bypass

LD R2 ← [R1] : IF CO DE RR AL DM1 DM2 DM3 RW $\overset{P_oP}{\uparrow}$
SD R3 → [R2] : IF CO DE DE DE DE DE $\overset{P_oC}{\uparrow}$ DE RR AL

[5 stalls]

DM1 DM2 DM3 RW.

(ii) with bypass

LD R2 ← [R1] : IF CO DE RR AL DM1 DM2 DM3 RW $\overset{P_oP}{\uparrow}$
SD R3 → [R2] : IF CO DE DE DE DE RR AL DM1 DM2 $\overset{P_oC}{\uparrow}$

[3 stalls]

DM3 RW $\overset{P_oC}{\uparrow}$
∴ R2 is needed for address calc in AL

4) ADD R1 ← R2, R3
SD R1 → [R4]

i) without bypass

ADD R1 ← R2, R3 : IF CO DE RR FPAL1 FPAL2 FPAL3 RW $\overset{P_oP}{\uparrow}$
SD R1 → [R4] : IF CO DE DE DE DE DE DE $\overset{P_oC}{\uparrow}$ DE RR

[4 stalls]

AL DM1 DM2 DM3 RW

(ii) with bypass

ADD R1 ← R2, R3 : IF CO DE RR FPAL1 FPAL2 FPAL3 RW $\overset{P_oP}{\uparrow}$
SD R1 → [R4] : IF CO DE DE DE RR AL DM1 $\overset{P_oC}{\uparrow}$
[1 stall]
DM2 DM3 RW

∴ R1 is needed to get data to be put in memory

2. Branch delay slots and stalls

Given:- 10-stage in-order processor.

branch outcome after 4 stages - 3 stall cycles.

branches = 15% of all instructions

branch taken - 70% , not taken - 30%

total cycles = # of instructions + stall cycles

let total # of instructions be 100.

$$\Rightarrow \text{avg CPI} = \frac{\text{total cycles}}{\text{total instructions}}$$

when fetch is stalled for every branch.

$$\text{total cycles} = 100 + 15 \times 3 \quad [\because 15 \text{ branched instructions each having 3 stall cycles}]$$
$$= 145$$

$$\text{avg CPI} = \frac{145}{100} = \boxed{1.45 \text{ cycles/inst}^n}$$

2) branch is predicted as not taken.

\Rightarrow 30% of 15 instructions i.e. 4.5 have no stalls

Δ 70% of 15 instructions i.e. 10.5 have 3 stalls.

$$\text{total cycles} = 100 + 10.5 \times 3$$
$$= 131.5$$

$$\text{avg CPI} = \frac{131.5}{100} = \boxed{1.315 \text{ cycles/inst}^n}$$

3) processor has 3 delay slots.

(i) Since there are no instructions to fill the delay slots, each of the 15 branched instructions will have 3 stall cycles.

$$\text{avg CPI} = \frac{100 + 45}{100} = \boxed{1.45 \text{ cycles/inst}^n}$$

- ② 3 instructions before the branch moved into delay slot
 \Rightarrow no stall cycles introduced for the branches.

$$\therefore \text{avg CPI} = \frac{100}{100} = \boxed{1 \text{ cycle/inst}}$$

- ③ 2 instructions from the taken block moved into delay slot
 \Rightarrow 10.5 instructions of the branch instructions won't have any stall cycles

but 4.5 instructions will have 3 stall cycles.

$$\text{avg CPI} = \frac{100 + 13.5}{100} = \frac{113.5}{100} = \boxed{1.135 \text{ cycles/inst}}$$

- ④ 3 instructions from the not-taken block moved into delay slot.

\Rightarrow 10.5 instructions will have 3 stall cycles

$$\text{avg CPI} = \frac{100 + 10.5 \times 3}{100} = \frac{100 + 31.5}{100} = \frac{131.5}{100}$$

$$= \boxed{1.315 \text{ cycles/inst}}$$

3. Deep Pipelines

Given: unpipelined processor.

cycle time = 20 ns

latch latency = 0.2 ns

POP \leftrightarrow POC = 6 ns.

independent instructions = 40%

dependent instructions = 60%.

(i) for unpipelined processor.

cycle time = 20 + 0.2 = 20.2 ns.

$$\text{since unpipelined throughput} = \frac{1}{20.2} = \boxed{0.049 \text{ BIPS}}$$

To find: throughput in BIPS.

(ii) 10-stage pipeline.

$$\text{time per stage} = \frac{20}{10} = 2 \text{ ns.}$$

$$\Rightarrow \text{cycle time} = 2 + 0.2 = 2.2 \text{ ns.}$$

$$\therefore \text{gap between independent instructions} = 2.2 \text{ ns.}$$

$$\# \text{ of cycle shifts for gap between PC & PCP} = \frac{6}{2} = 3 \text{ stages.}$$

$$\therefore \text{gap between dependent instructions} = 3 \times 2.2 = 6.6 \text{ ns}$$

$$\text{avg gap} = 0.4 \times 2.2 + 0.6 \times 6.6 = 4.84 \text{ ns.}$$

$$\therefore \text{throughput} = \frac{1}{4.84} = \boxed{0.206 \text{ BIPS}}$$

(iii) 20-stage pipeline

$$\text{time per stage} = 20/20 = 1 \text{ ns}$$

$$\Rightarrow \text{cycle time} = 1.2 \text{ ns.}$$

$$\therefore \text{gap between independent instructions} = 1.2 \text{ ns}$$

$$\# \text{ of cycle shifts} = \frac{6}{1} = 6 \text{ stages.}$$

$$\therefore \text{gap between dependent instructions} = 6 \times 1.2 = 7.2 \text{ ns}$$

$$\text{avg gap} = 0.4 \times 1.2 + 0.6 \times 7.2 = 4.8 \text{ ns}$$

$$\therefore \text{throughput} = \frac{1}{4.8} = \boxed{0.208 \text{ BIPS}}$$