Electrical Engineering Department

RTL to GDS implementation and verification of UART using UVM and OpenLane

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Introduction

- The universal asynchronous receiver/transmitter (UART) receives the data as bytes and sends the bits sequentially.
- The received bits are put back together into whole bytes at the destination side using a second UART. A shift register is present in each UART and is essentially used to translate serial data into parallel data.

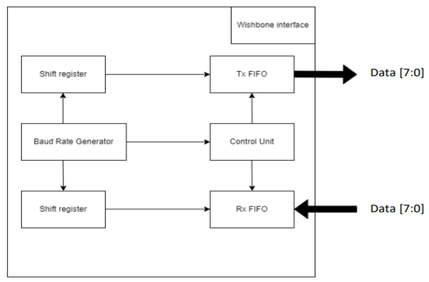

Figure 1: Proposed UART Design

- To avoid race circumstances, UVM offers systematic, orderly control over simulation behavior. This control will be carried out in sequence.

Methodology

Designing of UART:

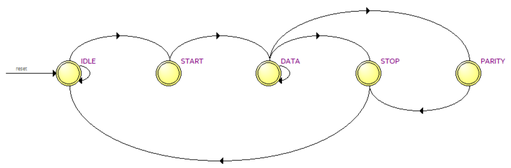

Figure 2: Transmitter FSM

- By default, it starts with the IDLE state before the Tx_enable signal is switched ON.
- Then it goes to the START state. Here, the transmitter adds the start bit to the shift register and shifts the data left.
- Then it goes into the DATA state.
- Finally, the FSM enters the last stage which is the STOP bit.
- If the parity_enable signal is turned ON, the transmitter adds a parity bit before entering the STOP bit.

Methodology

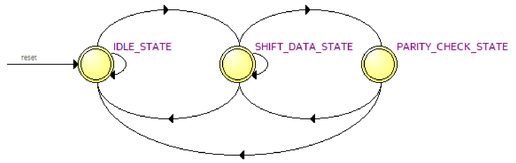

Figure 3: Receiver FSM

- The state machine starts by waiting for the start bit to be received in the IDLE_STATE.
- The state machine switches to the SHIFT_DATA_STATE after detecting the start bit.
- The state machine switches to PARITY_CHECK_STATE after receiving all the data bits and the parity bit.

Verification of UART:

1. Test Bench: It replicates the environment. The test bench verifies whether the RTL fits the design specs..
2. Test Cases: Test cases are generated for several scenarios that encompass the functionality and corner cases.

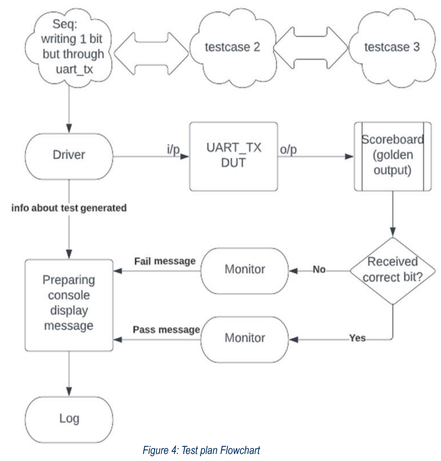

Figure 4: Test plan Flowchart

3. DUT: The hierarchal layering of the verification facilitates the maintenance and reuse of the DUT.

4. Virtual Interface: It offers a technique for separating abstract models and test programs from the actual signals that comprise the design.

5. Scoreboard: The data and control information at the output of the DUT are collected and compared to those at the output on the scoreboard.

Analysis and Results

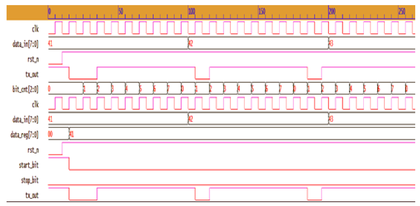

Figure 5: Simulation Results of Tx

- After running the tests and simulations on the DUT on both the transmitter and receiver side, the results have been satisfactory for ideal conditions.
- In some corner cases where the design is not expected to return any value, the DUT produces garbage values. Producing garbage values is expected as the spec that is defined by the team is pretty basic and just for educational purposes.
- In that case, the DUT and the verification environment work in perfect sync and show no anomalies during the runtime simulations.

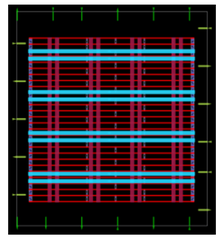

Figure 6:: Floor-planning

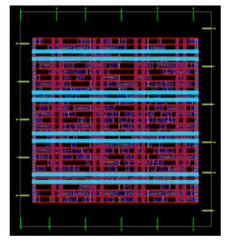

Figure 7: Placement

- Floor-planning is the process of allocating space for blocks/modules in a chip. Placement is the process of positioning the modules on the allocated space to optimize performance and reduce wirelength.

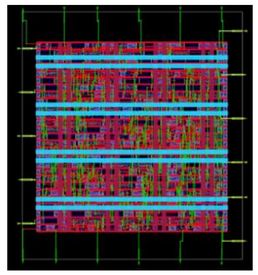

Figure 8: Routing

- Routing is the process of connecting the previously placed components in a chip design with wires to create a physical path for data flow.

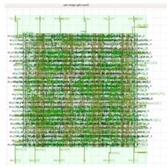

Figure 9: Sign-off

- Signoff refers to the final stage of a chip design where the design is checked against specifications and criteria to ensure functionality and manufacturability. GDSII is the file format used to transfer the finalized design data to a foundry for manufacturing.

Summary/Conclusions

- UART is a serial communication protocol that allows devices to communicate without the use of a clock signal. It sends parallel data that has been converted to serial format.
- It is a full duplex system that can transmit and receive data at the same time.
- This project proposes a methodology for the Design and Verification of a UART block along with physical implementation from the RTL to GDS flow using Open-Lane.

Key References

[1] Xi Jianbo, Xia Jijin, Luo Chuanhui, Deng Qingyong and Zhu Peng, “Verification method of FPGA universal configurable UART protocol based on UVM”, Date published: 06/29/2016. [Online]. Available: https://patents.google.com/patent/CN105718344A/en

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Acknowledgements

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