ECE 402

EE DESIGN PROJECTS

Fall 2015

**FINAL DESIGN REVIEW REPORT**

HI-FI Stereo System

by

Team Hi-Potential

Section 8, Team 3, Bench 4

|  |  |  |
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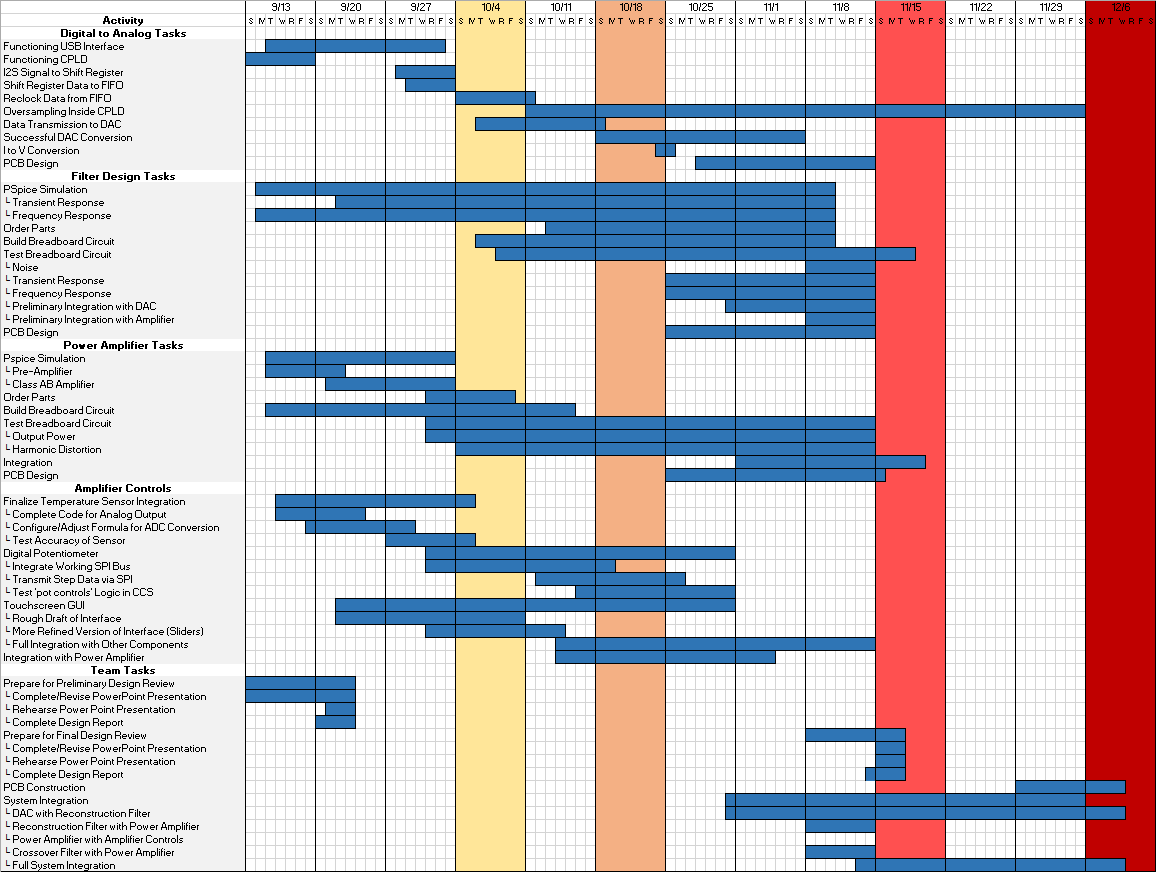
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# **Gantt Chart**

**Table 1:** Gantt chart for the team.



# **Final Acceptance Test**

The FAT for the Overall System with overall progress is as follows:

The customer should:

1. Be able to connect your system using a USB cable to a PC running windows

**Current progress:** Complete. The DAC subsystem has built a prototype for the USB input to the system, which is able to receive digital data, and output an I2S signal. The I2S is then manipulated using a CPLD and output to a DAC which then outputs the original digital data in an analog waveform.

2. Play music on the PC out of the speaker system

**Current progress:** This requirement encompasses all of the subsystems. The DAC subsystem has achieved success in outputting an analog waveform from a digital input. This signal is then able to pass through the Reconstruction Filter successfully and onto the Power Amplifier. The Power Amplifier has been able to amplify the reconstructed signal to eight watts RMS. This amplified signal is then split into the three, eight ohm speakers with the aid of the Crossover Filter, and from there output successfully on the subwoofer, midrange, and tweeter speakers. The Amplifier Controls subsystem is able to adjust the treble, midrange, and bass levels through the use of a touchscreen and GUI.

**Total Team Progress: 85%**

3. Control the volume, treble, midrange and bass using a touchscreen GUI

**Current progress:** The Amplifier Controls subsystem has successfully been able to adjust treble, midrange, and bass levels during full integration of the subsystems. Level adjustments are audible and almost completely noiseless.

4. Be provided with a calibration certificate with the following:

1. The THD+N of the overall system (0dB @ 1 kHz)

**Current progress:** THD+N measurements have begun being tested but with a 1 KHz sine wave at -15dB. Current values are around .452% or -46.89dB.

2. The THD+N after the reconstruction filter (0dB @ 1 kHz) before the amplifier

**Current progress:** THD+N measurements have begun being tested but with a 1 KHz sine wave at -15dB. Current values are around .2354% or -52.56dB.

3. An assessment of how to improve audio quality

**Current progress:** As of right now the digital interpolation is still being completed, so the team believes achieving that will greatly improve the audio quality.

# 

# **System Summary**

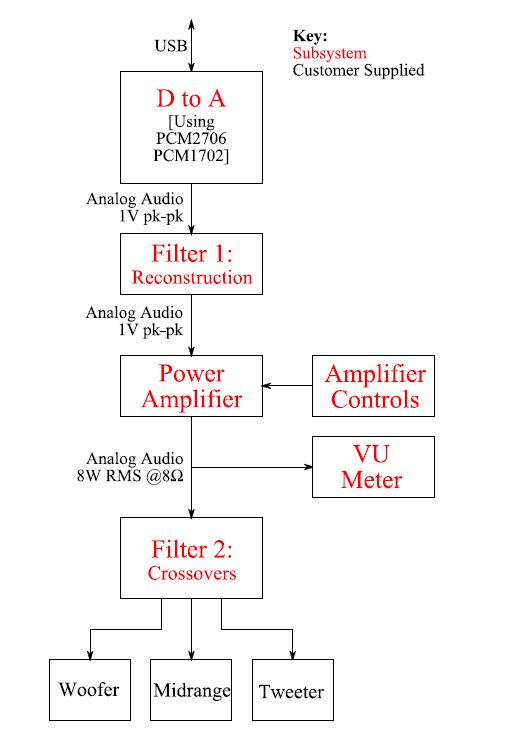
The goal of this project is to design a high fidelity stereo system. As described in the Course Handbook [1]:

The customer wishes to prototype a top performing integrated audio system that would amplify signals provided by means of USB digital audio (16 bit 44.1 kHz) to three 8Ω loudspeakers. Physically the system is to create one integrated package controlled via a touchscreen interface.

*Whole System Specification / Constraints*

1. All subsystems, unless specified, to be built from basic op-amps (LF356, LM358, etc.), programmable logic devices (PLD 16V8 or 22V10), timers (LM555, 74HC123, etc.), 74HCxx and CD4xxx series logic and other support chips. If in doubt please consult with your TA or Dr. Matthew Swabey.

2. All subsystems should be capable of being demonstrated and powered separately.

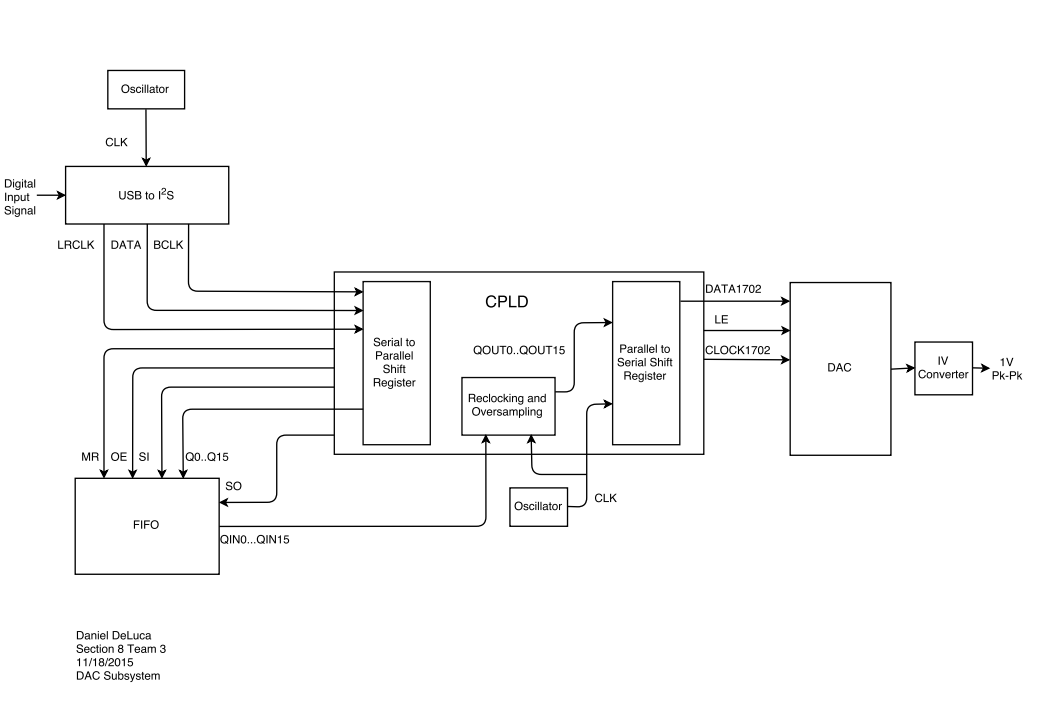
The overall block diagram comes from [1] and is shown in **Figure 1**.

**Figure 1:** The whole-system block diagram for the HI-FI stereo system.

# **Digital to Analog Converter Subsystem**

## **Subsystem Requirements and Block Diagram**

The main requirement for the Digital to Analog subsystem, as denoted in the ECE 402 Course Handbook [1], is to create a minimum one volt peak-to-peak signal for the Reconstruction Filter subsystem. To achieve that, there are several issues this subsystem must resolve. The PCM2706 USB Interface outputs a 16 bit I2S signal, but the PCM1702 DAC only accepts inputs of 20 bits. Another issue is these two ICs have different timing clocks. The bit clock of the I2S signal is 2.822 MHz, while the speed the DAC is expecting in order to achieve an 8x oversampling is 7.056MHz. Aligning these clocks is critical in creating a smooth sound.

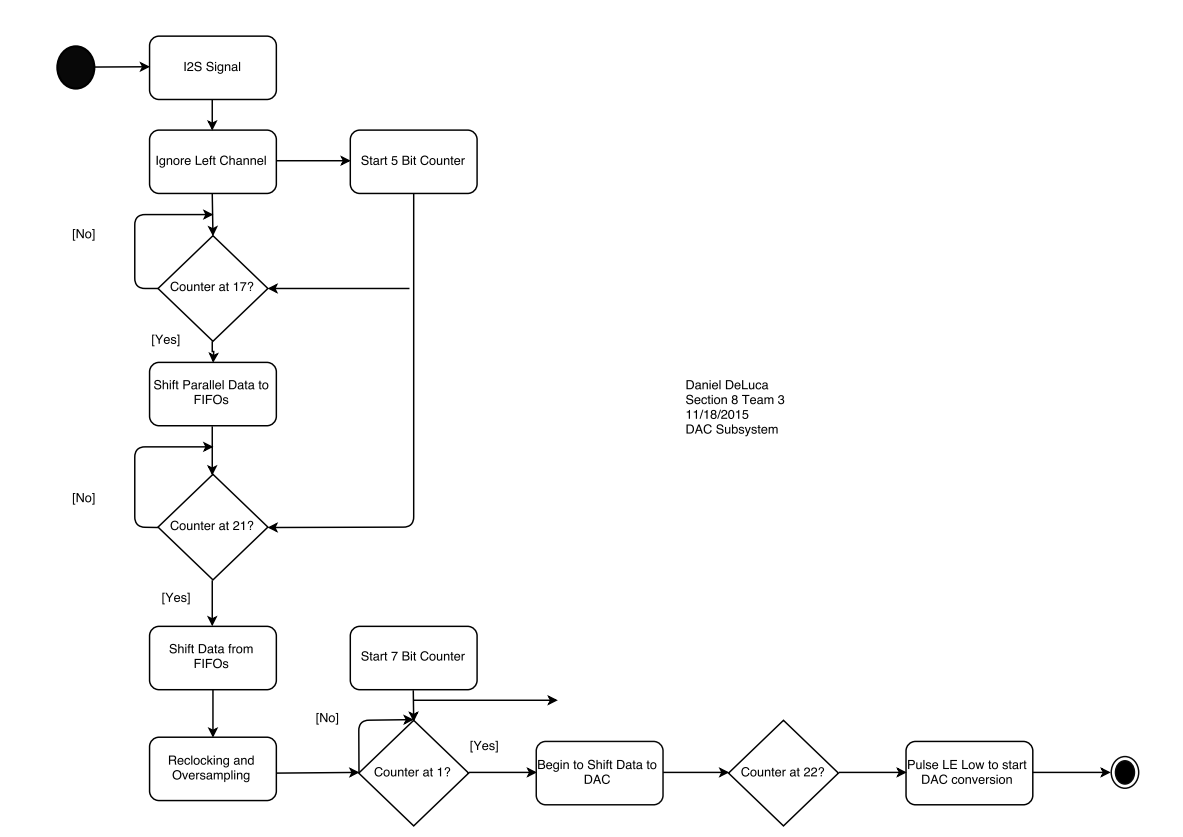
The final issue is that the DAC outputs a current signal, but the Reconstruction Filter subsystem requires a voltage signal. An operational amplifier will be utilized for this I-to-V conversion. To resolve the 16 to 20 bit conversion the ispMACH4256ZE CPLD will send the Latch Enable signal four clock cycles after the 16 bit signal in order to pad the sample with zeros. The clocking synchronization will be accomplished using shift registers, 4 FIFO chips, and the CPLD. One shift register will be used to convert the serial data into parallel data, which will then be input into the FIFO chips and then clocked out using the CPLD at the speed the DAC requires. The data signal will then be converted back to serial format using a parallel to serial shift register within the CPLD. From there it will be oversampled by a factor of eight and linearly interpolated within the CPLD before being zero padded, and fed into the DAC. The DAC will output a current signal, which will then be converted to at least a one volt peak-to-peak voltage signal using an inverting op amp circuit. The corresponding block diagram is shown below in **Figure 2**.

**Figure 2:** DAC subsystem block diagram

## **Design**

The subsystem utilizes several elementary components. Shift registers and FIFO chips are far from complex systems, but can meet the subsystem requirements if implemented properly. The CPLD is a powerful device that was chosen due to its ability to quickly and efficiently run an ABEL program. The CPLD serves two main functions in this subsystem. One, it will assist in the completion of clock matching between the PCM2706 and PCM1702. Second, it will be entirely responsible for completing the 8x oversampling that the team has chosen for its design.

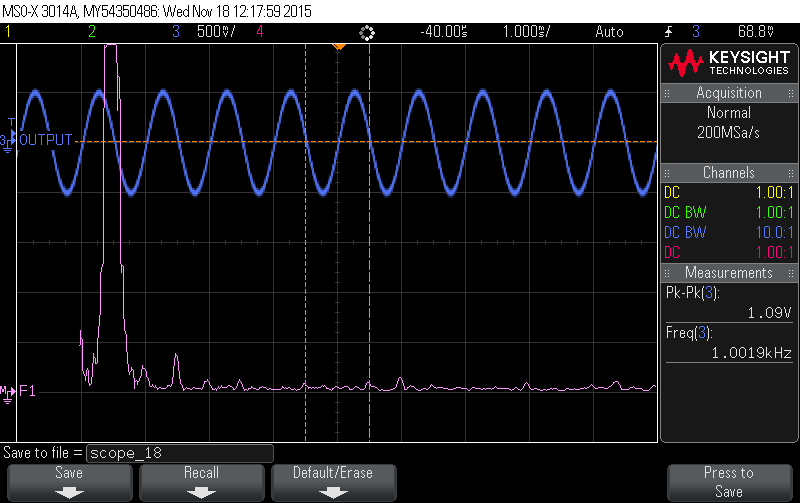
The linear interpolation itself will be utilized with simple add and divide logic. Taking the mean of two points and inserting the result in between the two original points creates a new data point, or 2x oversampling. Computing that arithmetic a total of seven times between each of the new points will create an 8x oversampling. The software in the CPLD is written in the ABEL programming language. Resources from [2] were used. A flow diagram of the software is displayed in **Figure 3.** The four FIFO chips also assist in matching the timing domains between the PCM2706 and the PCM1702. The FIFOs hold their input values at the outputs until the inputs change. Since the inputs only change when the LRCLK is high, there is ample time to clock out the data from the FIFOs at the new frequency.



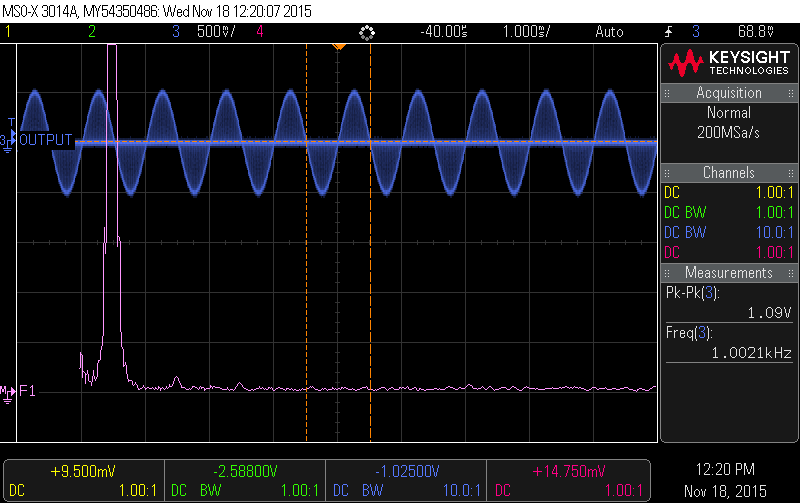
**Figure 3:** Activity Diagram of ABEL Software



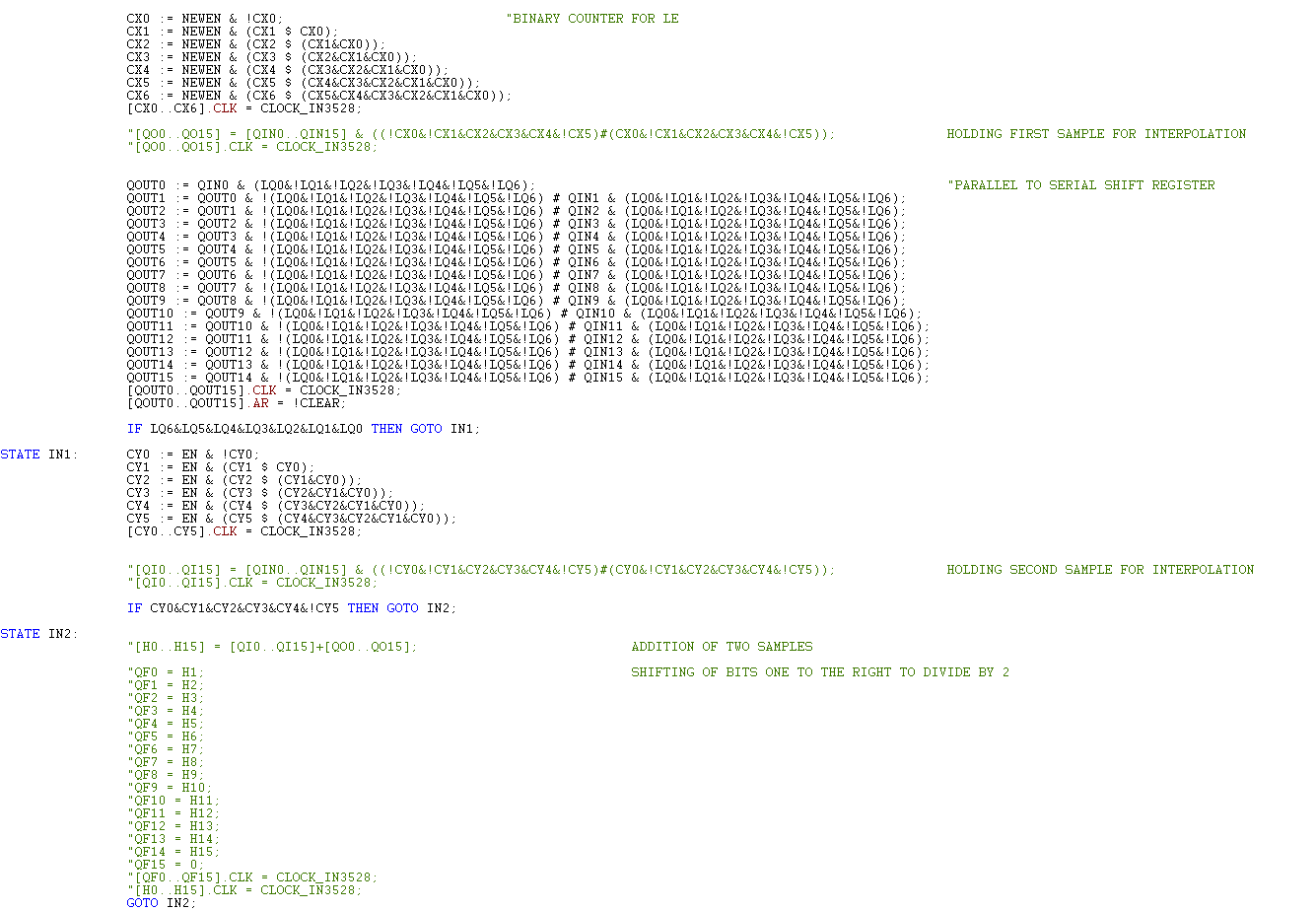
**Figure 4:** DATA signal represents data from the PCM2706. DATA1702 is the reclocked data that is being sent to PCM1702 at the CLK1702 frequency. LE is also shown 4 clock cycles past DATA1702 to pad the signal with 4 zeros. The second LE pulse is used to send 20 zeros to the PCM1702 for decimation.



**Figure 5:** A 1 KHz sine wave without the use of interpolation or decimation. The accompanying FFT shows some peaks in the 2nd, 3rd, and 4th harmonics. This signal is then sent to the Reconstruction Filter.



**Figure 6:** Decimated 1 KHz sine wave through the method of zero stuffing. The CPLD accomplishes this by sending 20 zeros to the PCM1702 between every 16 bit sample. The FFT of this signals shows less harmonic distortion than without the decimation.





**Figure 7**: CPLD code for DAC Subsystem

## **Testing Requirements**

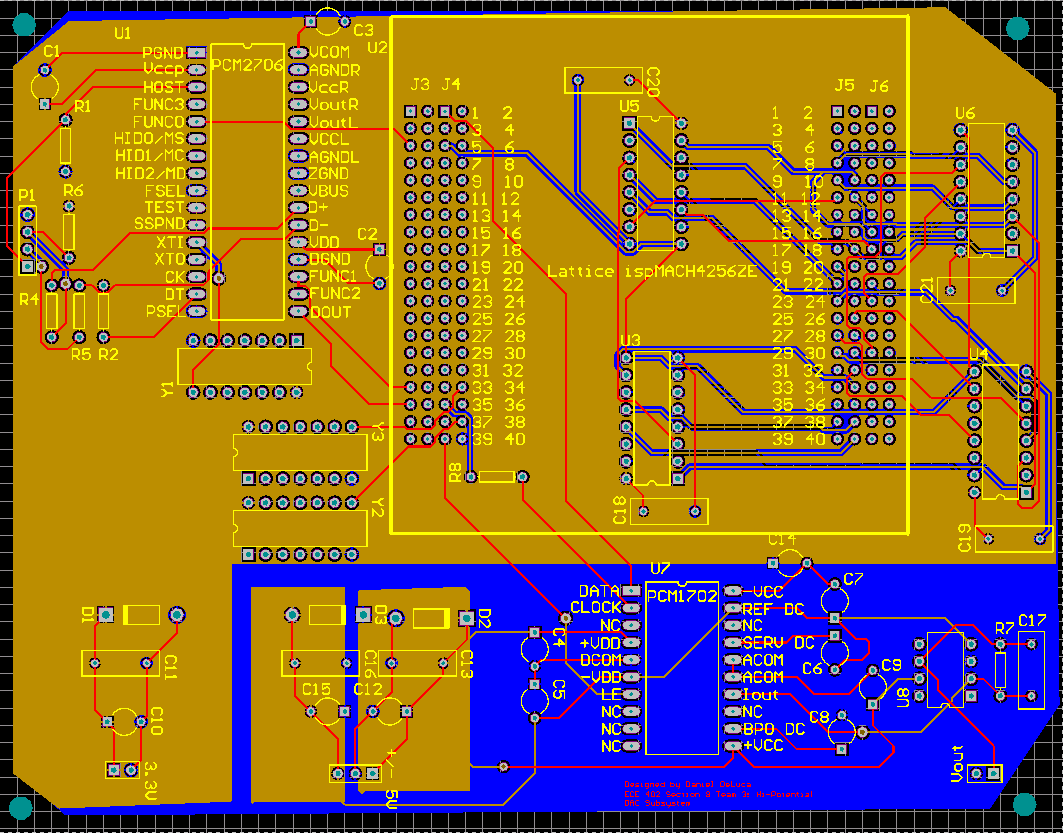
To meet the requirements of the DAC subsystem, several tests must be completed. As the design nears completion, there are several ways to test its functionality. The interpolation will be tested by using an oscilloscope to see if there in fact seven more samples in between the two original 44.1 KHz samples. Sending waveforms of varying frequencies will ensure that all audio will be passed through the subsystem and eventually heard through the speakers. Frequencies that will be tested are 40 Hz, 100 Hz, 315 Hz, 1 KHz, 5 KHz, 10 KHz, and 18 KHz. The oscilloscope can again be used to view any glitches in the output waveforms. An FFT analysis of these waveforms will show any distortion as well. From there, integration between all the subsystems will be the next test. The output from the DAC will be sent to the Reconstruction Filter subsystem to ensure that the filter is working properly, and meeting its requirements. An FFT again will be useful for the THD+N measurements after the Reconstruction Filter. A full system integration to the 8 ohm speakers will be the final test to verify that any music file can be played over the 3 speakers, with a final THD+N calculation.



## **Prototype**

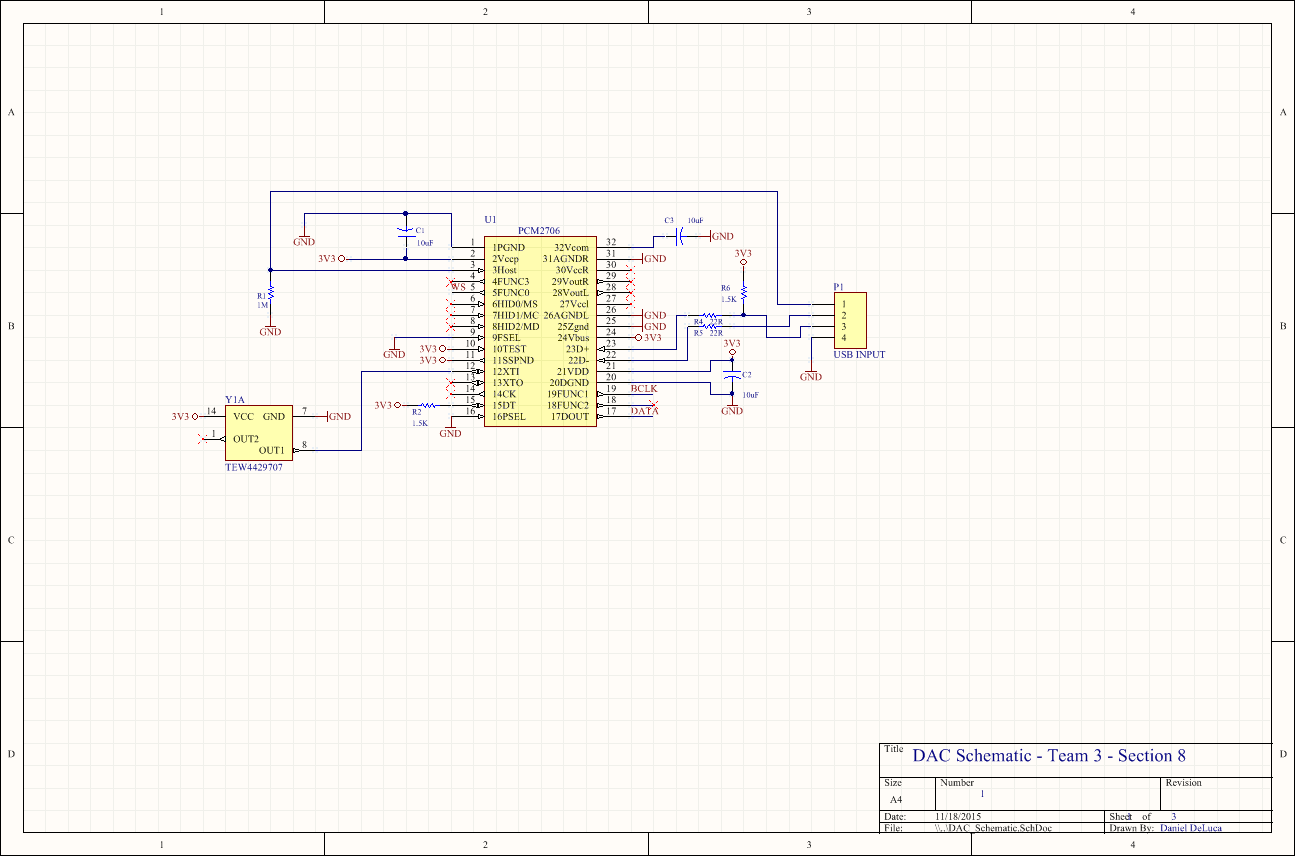
**Figure 8:** Prototype of DAC Subsystem

## **PCB**

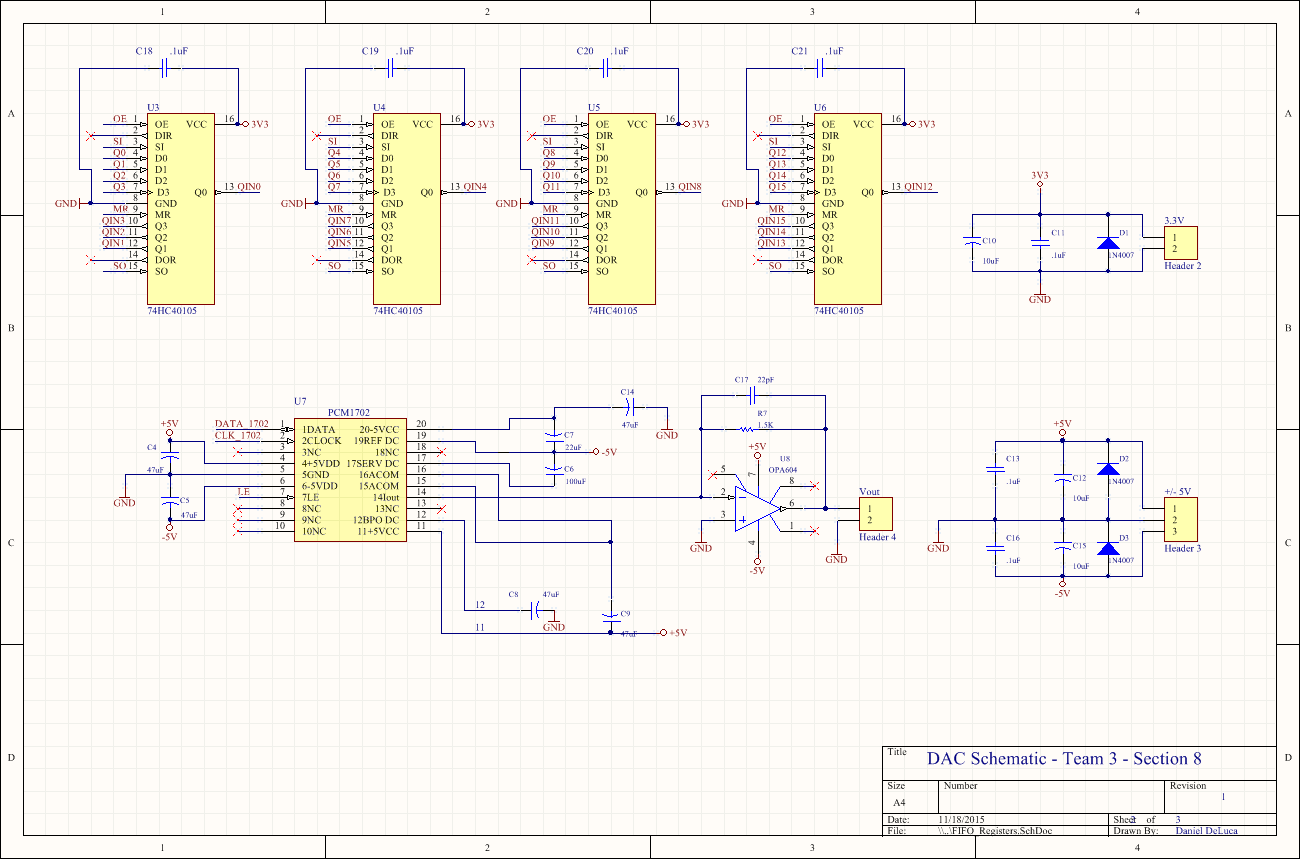


**Figure 9:** Three layer PCB Design for the DAC Subsystem

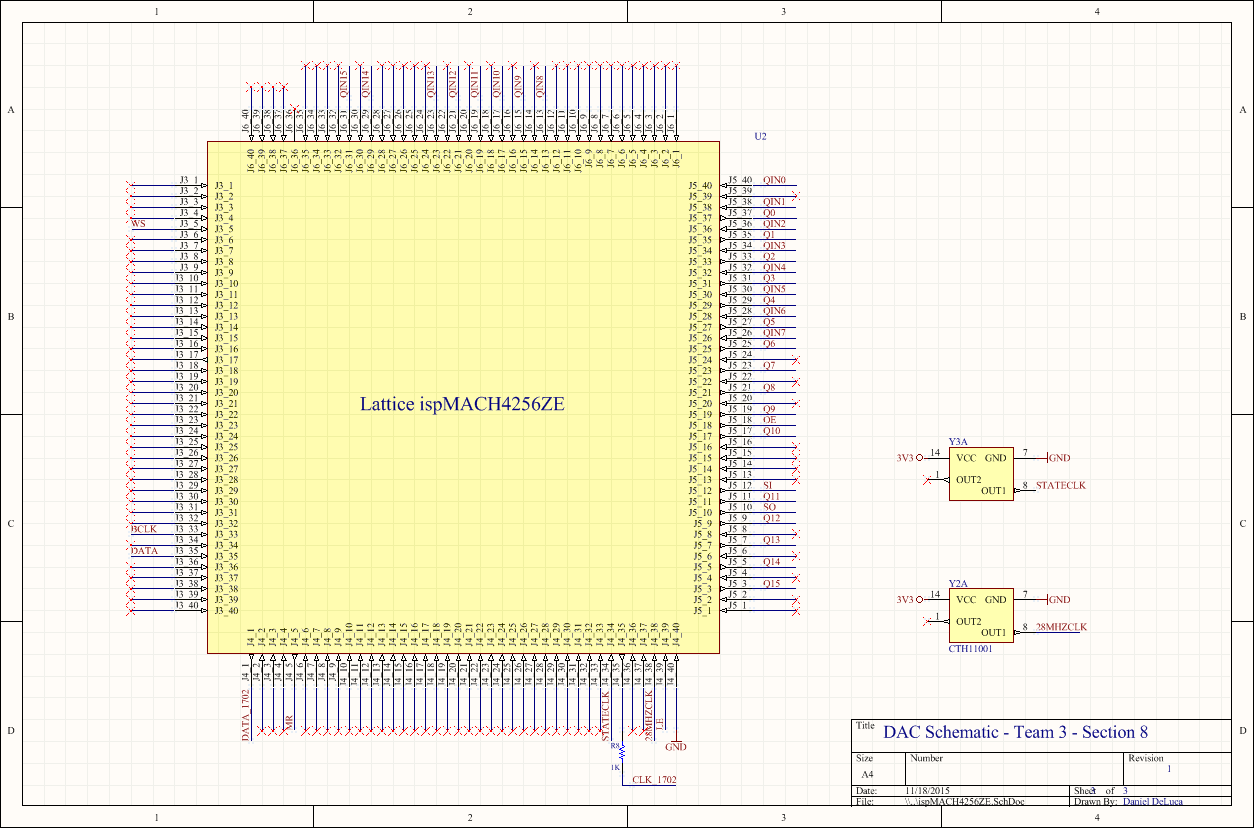
## **Schematics**



**Figure 10a:** Schematics for DAC Subsystem



**Figure 10b:** Schematics for DAC Subsystem



**Figure 10c:** Schematics for DAC Subsystem

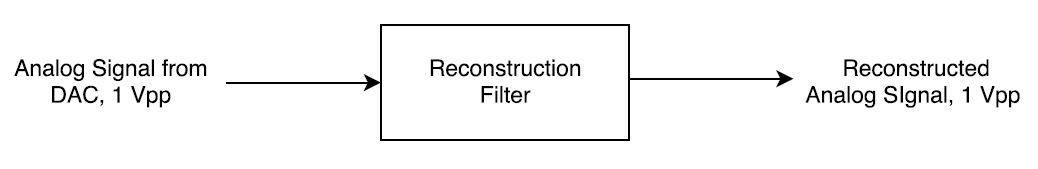
# **Reconstruction Filter and Crossover Filter Subsystem**

## **Subsystem Requirements and Block Diagram**

As described in [1], the system requires several different filters. Filter 1 is a reconstruction filter for the DAC and its parameters depend on the design of the DAC subsystem. Filter 2 is a bank of three filters that separate the audio frequency band into the different sets that drive each type of speaker correctly.

### *Filter 1, Reconstruction*

If the sampling frequency of the digital audio gets to a tweeter with enough bandwidth, it could damage it by overloading it. In addition, high frequencies have the potential to create sub harmonics in the final output of the system by the means of intermodulation distortion. It is this why a high quality filters are required. The order and type of the filter can vary but non-oversampled systems need a more aggressive-high order filter in contrast to the oversampled system which can obtain the same results with more simple and relaxed filters. The output of the system must be a minimum of 1V pk-pk and have enough slew rate to drive the next stage, as shown in **Figure 11**. These requirements come from the ECE402 Course Handbook, [1].

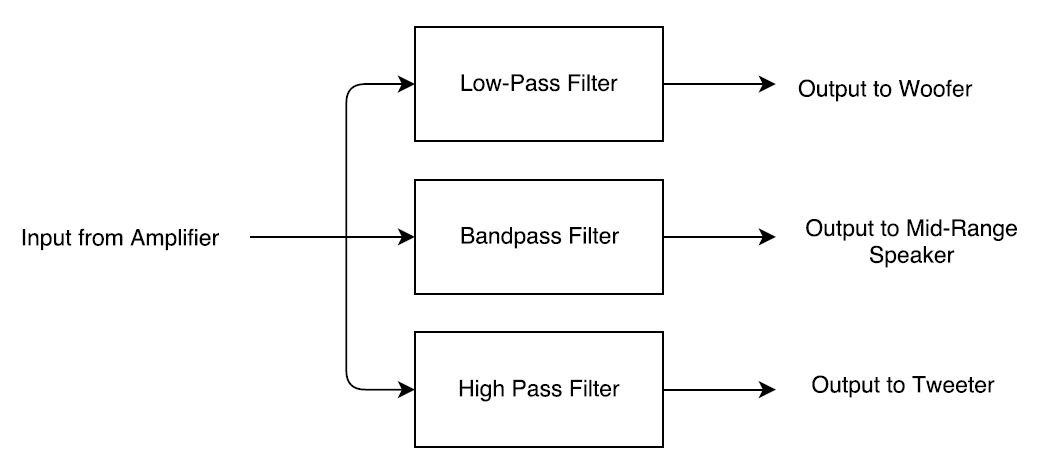


**Figure 11:** The reconstruction filter takes an analog signal of at least one volt pk-pk, filters out the higher frequency repetitions of the frequency response, and outputs the reconstructed signal at a minimum of one volt pk-pk.

### *Filter 2, Crossovers*

Finally, the customer desires a system with a tweeter, a midrange speaker and a woofer. Thus the filter engineer is to design three passive filters to be coupled with the speakers in the final stage. This is depicted in **Figure 12.** All filters need to be simulated. Harmonic distortion and frequency response plots are expected. Comparison measurements to the real design also need to be measured.

The filters must match the phase and amplitude curves supplied by the customer to match their speaker cabinet and speaker choices. The designer must be aware of the power requirement – excess energy at unwanted frequencies will be substantially converted to heat in the components of the system so be sure to keep the ratings sufficient. These requirements come from the ECE402 Course Handbook, [1].

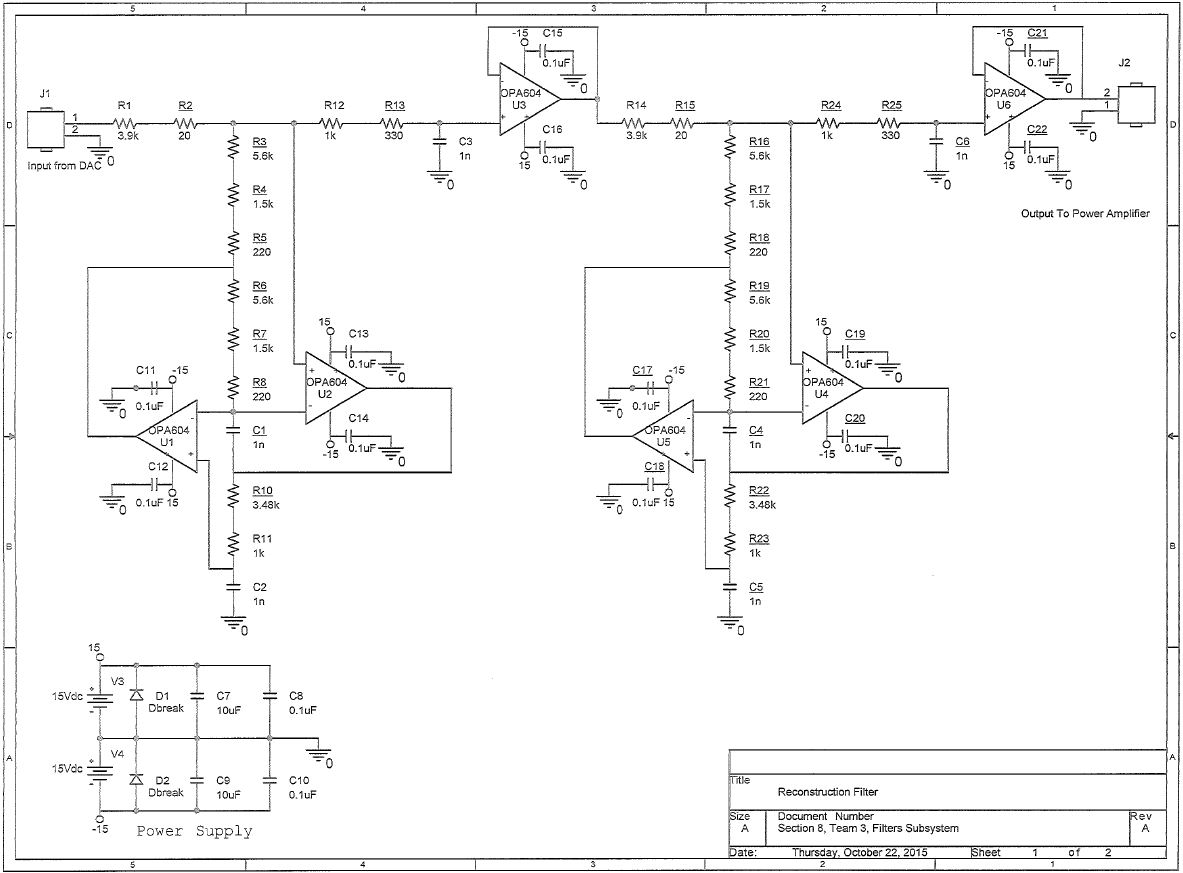


**Figure 12:** The crossover filter is a filter bank that splits the output from the amplifier and routes the appropriate frequency range to the correct speaker.

## **Filter Design and Schematics**

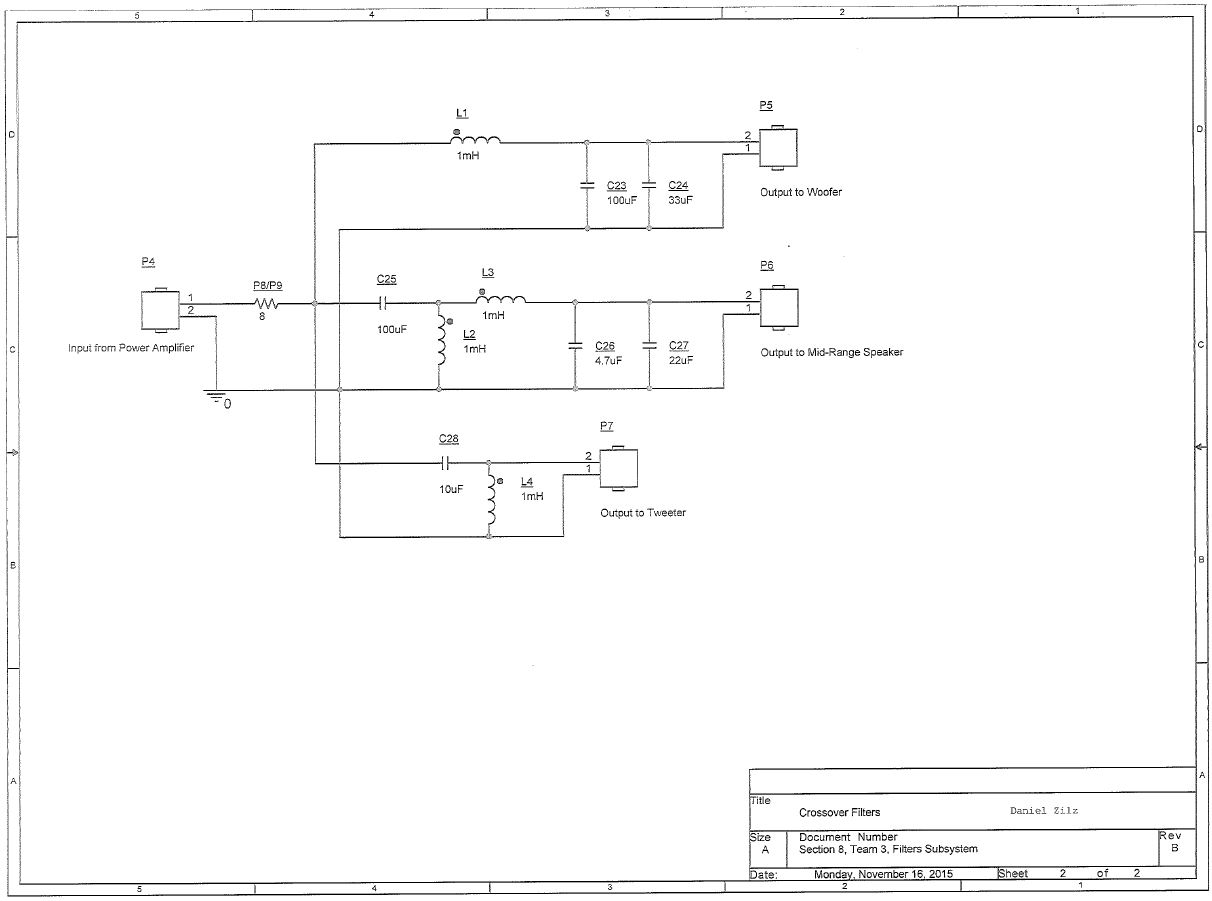
A sixth order Bessel filter is used for the reconstruction filter. The characteristic for this filter is ideal because it can be designed to have uniform phase delay over the auditory frequency range. Initially, it was assumed that the DAC could achieve 8x oversampling, thereby stretching out the sinc envelope in the frequency domain while also spreading the images. Consequently, it was desired that the Bessel filter roll off significantly (in this case -68dB) by 330.7 kHz, where the next highest frequency image would occur. Currently, oversampling via interpolation has not been achieved, so the following design may be altered to have a lower cutoff frequency to filter out more high frequency images. The current design is shown in **Figure 13** and is based on [3], with a change of op-amp. Tests of the frequency response have been done on the reconstruction filter and are shown in **Figure 15**. The frequency and phase response match very well to simulations. A printed circuit board (PCB) was designed to implement this solution and is shown in **Figure 25.** The PCB uses two ground planes.

The crossover filter is consists of a low-pass, band-pass, and high-pass filter. Three main considerations needed to made for the crossover filter design: cost, frequency response performance, and ability to handle high power. Numerous iterations were needed to optimize these considerations. Bi-polar capacitors with 50V rating were used to meet this specification. The hardest task was modifying the filter design while also finding inductors which could withstand the current necessary to drive the speakers. Eventually, a 1 mH inductor with a current rating of 1.9A was chosen. Initially, the current rating was not sufficiently high enough, but adding an 8 ohm power resistor between the power amplifier and the rest of the filters limited the current so that the max current drawn through any inductor was less than 1.9A. The schematic for the crossovers is shown in **Figure 14**. Tests of the frequency responses for all three filters have been done and are shown in **Figure 16**, **Figure 17**, and **Figure 18**. The phase shifts are very close to the simulations where the filters are most effective. The magnitudes match well too. The THD+N of the filters were also measured with an audio analyzer and are shown in **Figure 19**, **Figure 20**, and **Figure 21**. A PCB was designed to implement this solution and is shown in **Figure 26**. The PCB was designed to handle two different types of inductors, hence the interesting design for the inductors on the PCB. The PCB uses two ground planes.

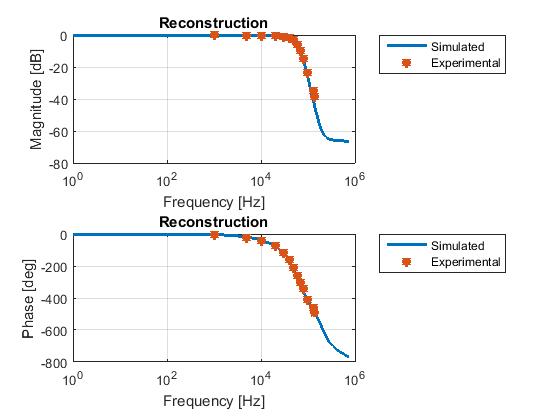


Daniel Zilz

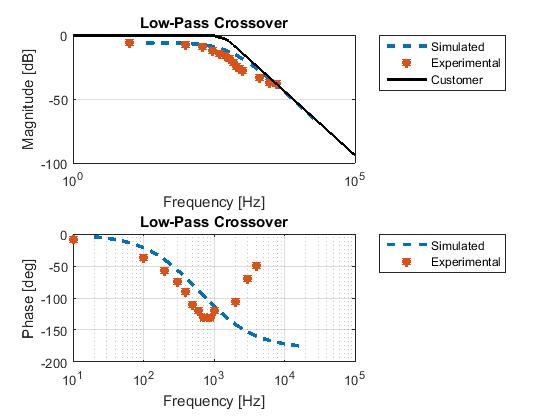
**Figure 13:** Sixth order Bessel Filter that is used for the reconstruction filter.



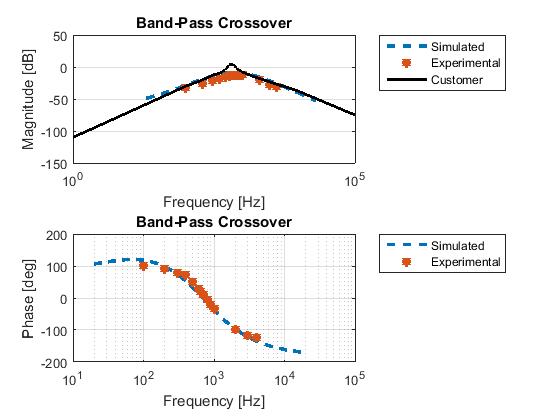
**Figure 14:** Crossover filter schematic.



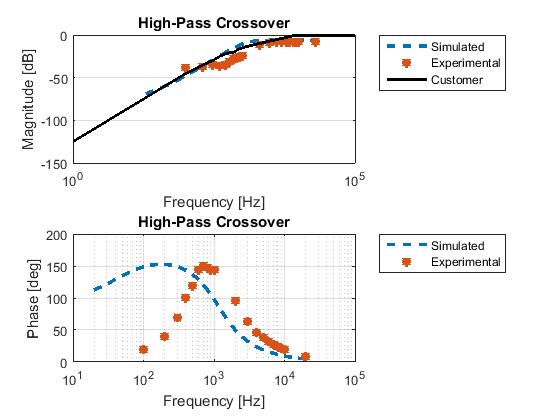
**Figure 15:** Frequency response for the reconstruction filter.



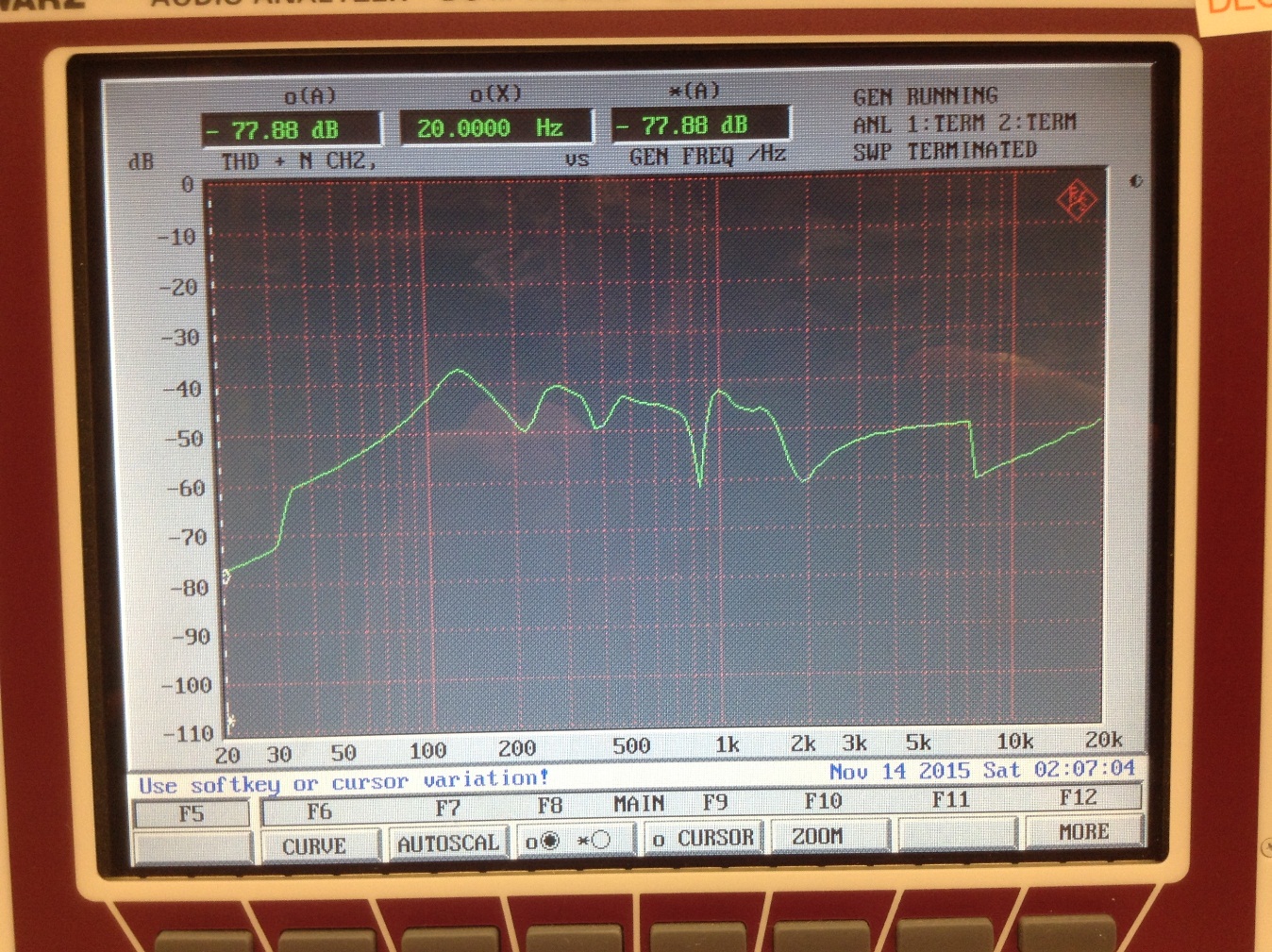
**Figure 16:** Frequency response for the low-pass filter.



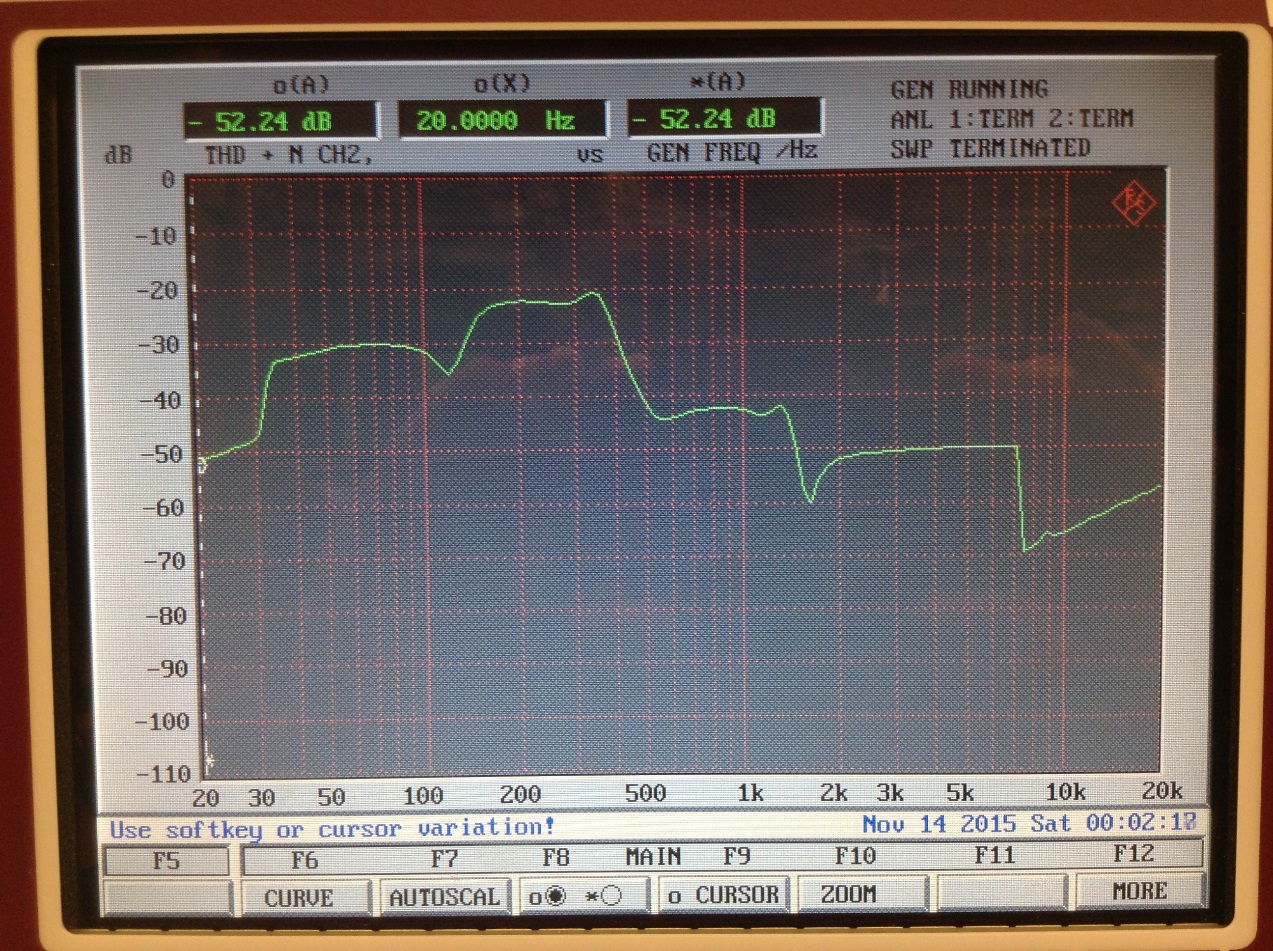
**Figure 17:** Frequency response for the band-pass filter.



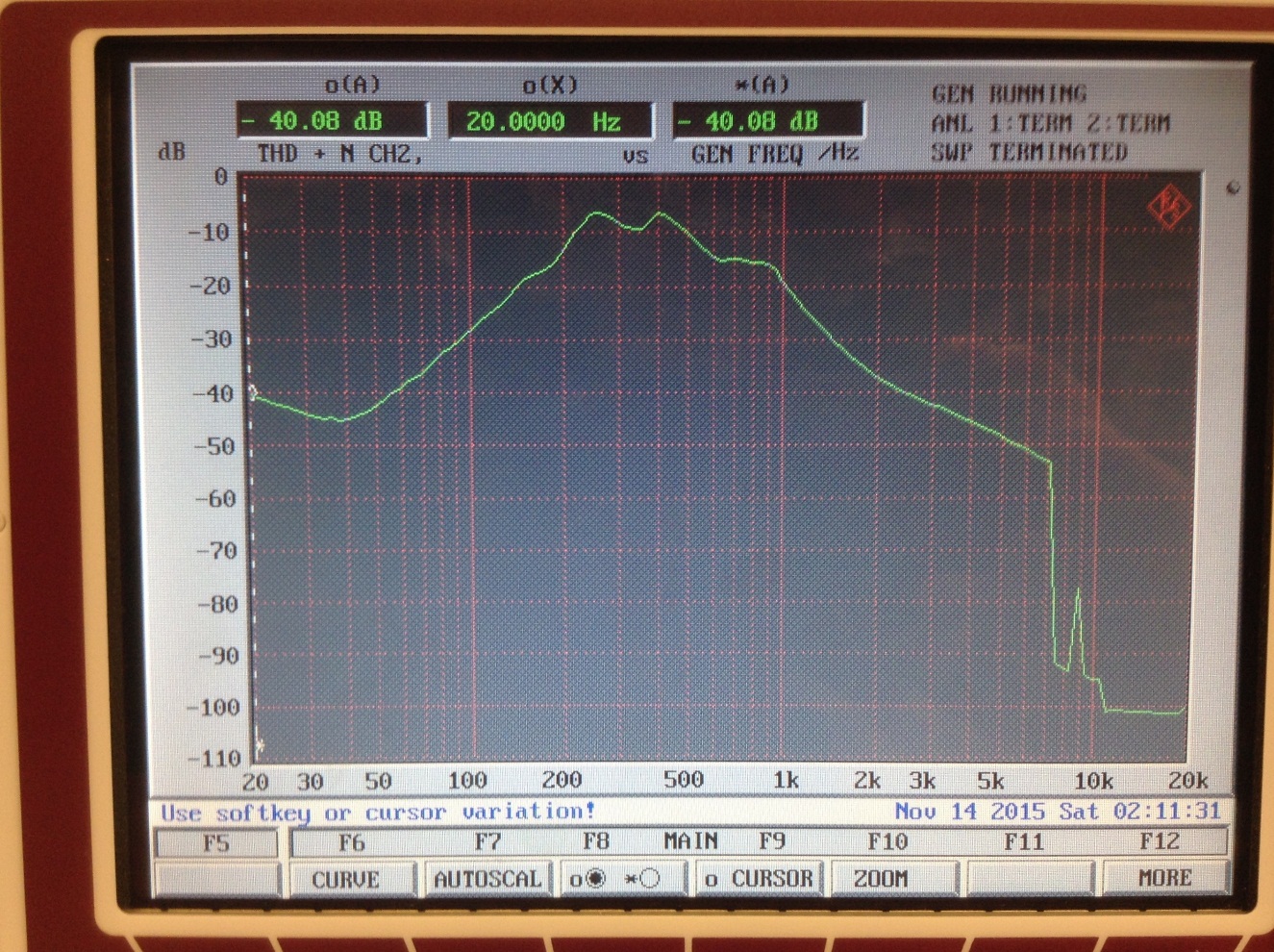
**Figure 18:** Frequency response for the high-pass filter.



**Figure 19:** THD+N of the low-pass filter.



**Figure 20:** THD+N of the band-pass filter.



**Figure 21:** THD+N of the high-pass filter.

## **Testing Plan**

**Table 3** shows the testing plan for the filter subsystem.



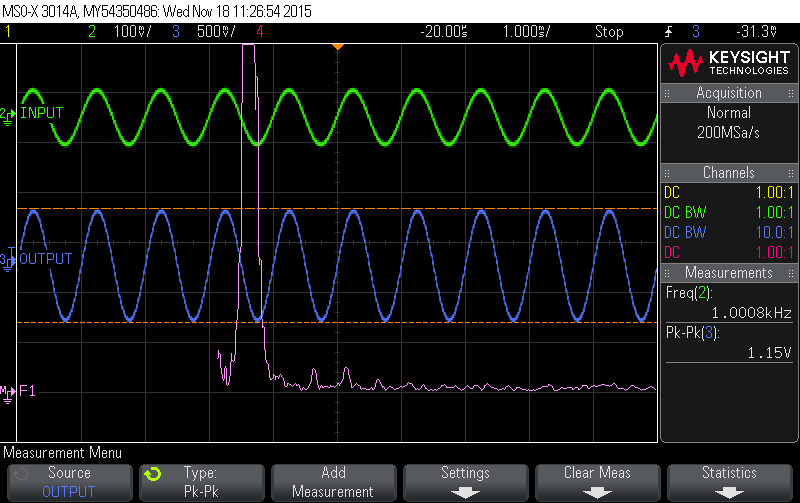
The OPA604 op-amp was selected for its high quality performance in audio applications. It has a slew rate 25V/microsecond. For a 1 volt peak-to-peak sinewave, this indicates that it has a sufficient slew rate up to 7.95MHz, which is more than enough. Indeed, it was observed that it has sufficient slew rate on the oscilloscope. See the following equation:

The output peak-to-peak voltage of the reconstruction filter was measured using the oscilloscope. As seen from the frequency response, the filter should pass a 1 volt peak-to-peak sinewave when given a 1 volt peak-to-peak sinewave. We observed that this was the case.

Harmonic distortion for the three filters was measured using the audio analyzer’s THD+N capability, which gave an output in dB. General procedures and settings provided by the audio analyzer manual were used.

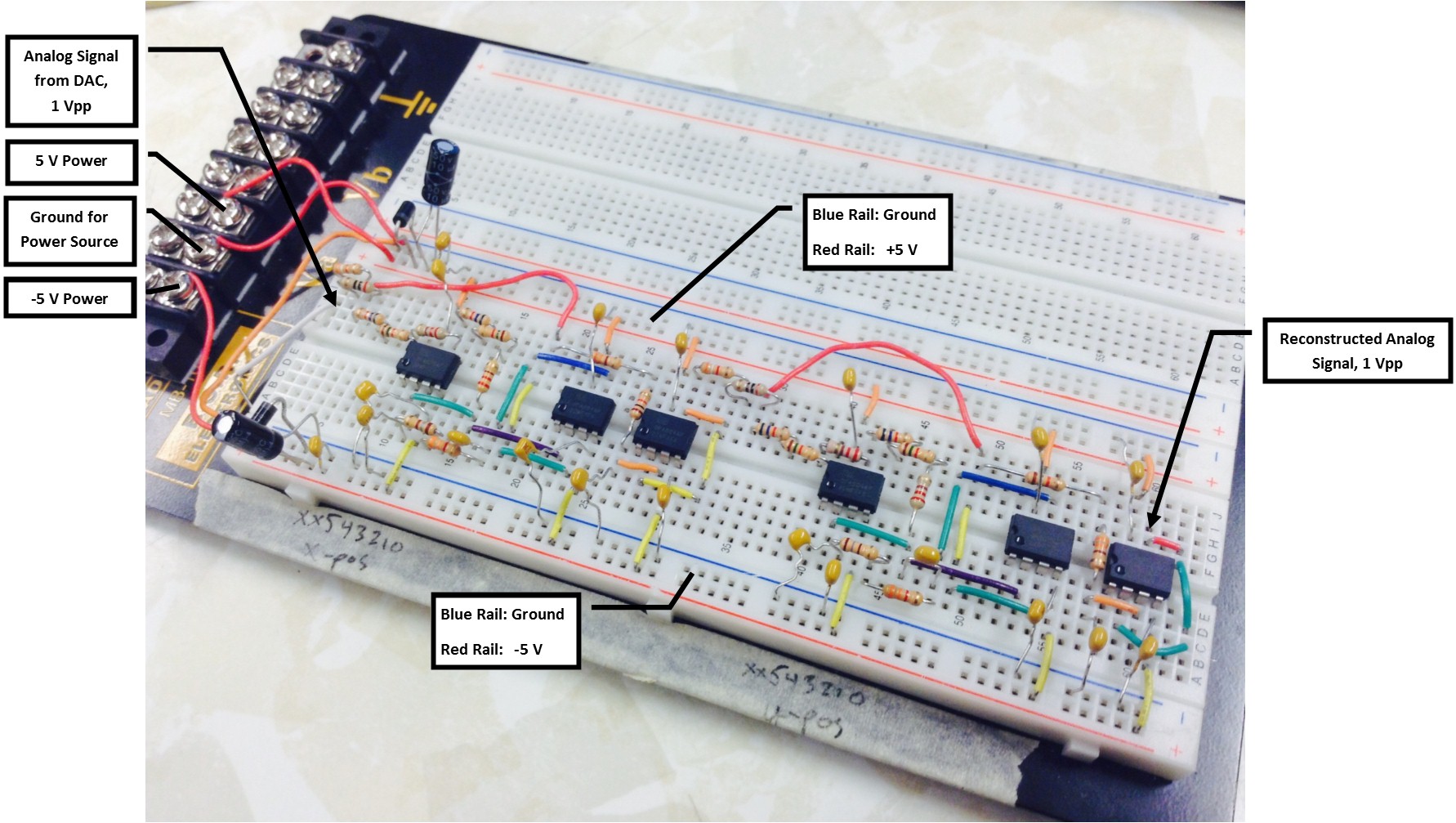
The frequency responses of all the filters were measured using a function generator and oscilloscope, since the desired measureable frequency range exceeds that which the audio analyzer can measure. In order to test this circuit, the filter was given a one volt peak-to-peak sinewave at its input. At various frequencies, the peak-to-peak amplitudes of the input sinewave and resulting output sinewave were measured, as well as the phase shift between the two sinewaves. From this data, attenuation could be calculated in dB. It was decided not to use an input buffer on the crossover filters to eliminate the function generator’s effect on the passive elements. This decision was made because some sinewaves exiting from the buffer were distorted, making it impossible to measure the true peak-to-peak voltage. Consequently, decibel calculations were made from the output sinewave of the filter and the actual sinewave going into the filter, not what the function generator said it should be outputting.

## **Integration with other Sub-Systems**

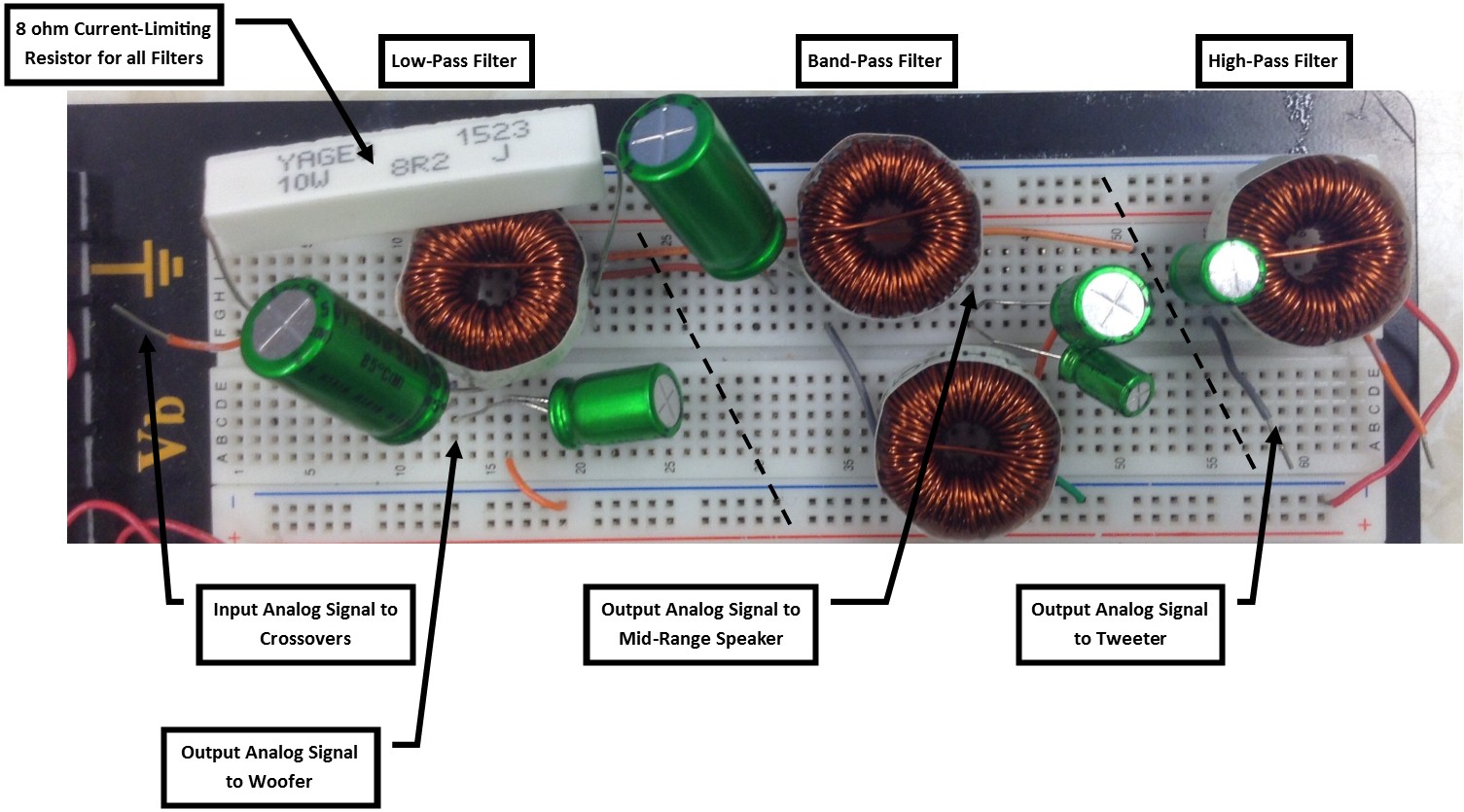


**Figure 22:** Integration with the DAC subsystem. Input measured at signal coming from DAC. Output is measured at the output of the reconstruction filter. The THD+N of the output of the reconstruction filter is .2354% or -52.56dB.

## **Prototypes**

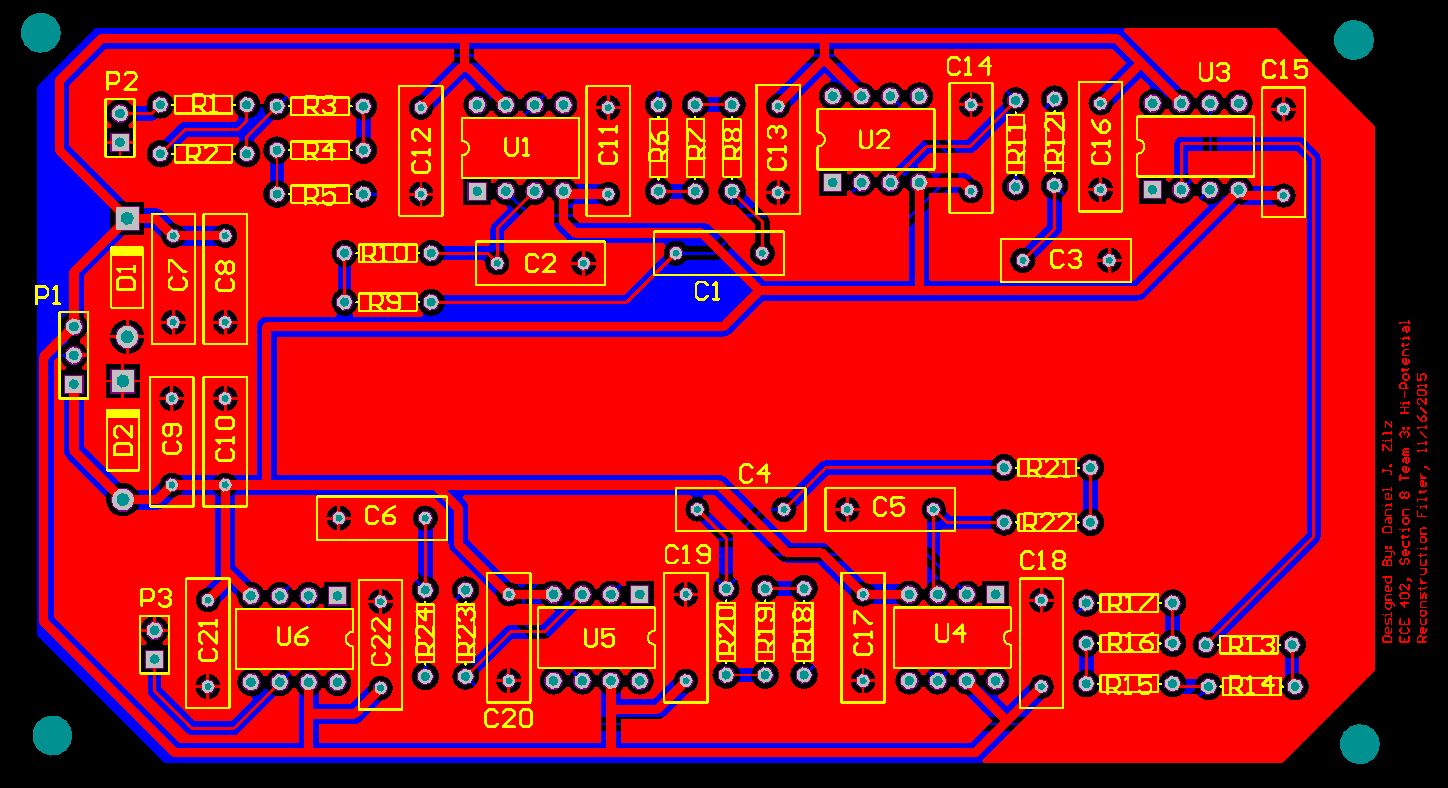


**Figure 23:** Reconstruction filter as built on a breadboard.



**Figure 24:** Crossover filter bank as built on a breadboard.

## **PCBs**



**Figure 25:** Reconstruction filter PCB.



**Figure 26:** Crossover filter bank PCB.

# **Power Amplifier Subsystem**

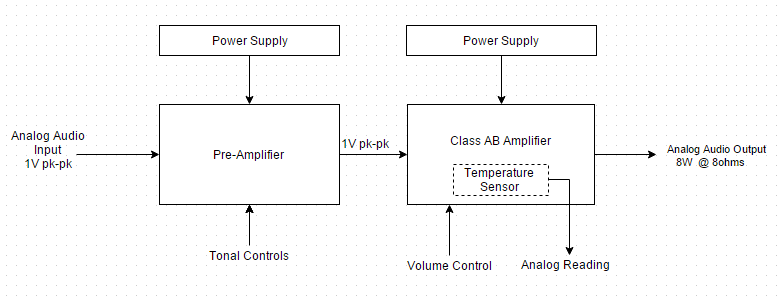
## **Subsystem Requirements and Block Diagram**

The client wants to explore several topologies and technologies for the amplifier. The requirements are a minimum of 8W RMS per channel power to 8Ω speakers with maximum 1% second harmonic distortion and 0.2% third harmonic distortion. Single chip integrated IC amplifiers are not allowed. Impulse response, frequency response, harmonic distortion plots and equations to justify the systems and components are expected. Designing in collaboration with amplifier controls is required. Tonal controls are typically implemented before the power amplification however the volume control is typically a control on the gain of the amplifier. These requirements come from the ECE402 Course Handbook, [1].

Requirements

1. Minimum of 8W to 8Ω speaker
2. Maximum 1% 2nd harmonic distortion
3. Maximum 0.2% 3rd harmonic distortion

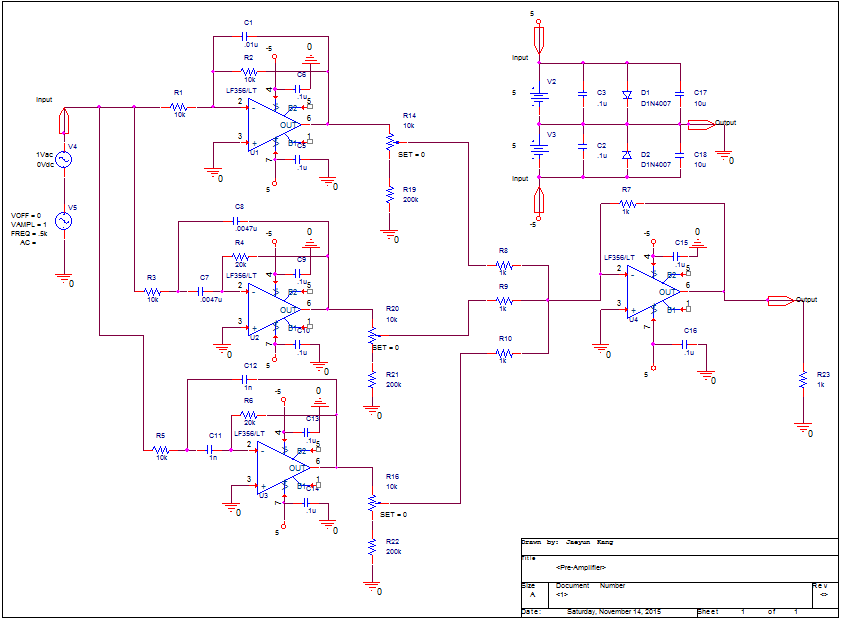
**Figure 27** shows the pre-amplifier taking an analog input of 1V pk-pk. In the pre-amplifier, the signal goes into three different op-amps to filter each frequency range to the woofer, midrange, and tweeter speakers. Since the woofer plays low frequencies, a low pass filter is suitable. For the mid-range speaker and tweeter, band pass filters can be used. At this stage, each tone can be controlled through a touch screen interface. The gain of each tone is controlled by digital potentiometers. Then the three filtered signals go into a summing op-amp. Output of the summing amplifier is still 1V pk-pk and goes to a Class AB amplifier. The signal will be amplified to meet required peak voltage and load current. The volume will be controlled by a touch screen and temperature can be monitored by a temperature sensor that is connected to a heat sink. Output will be a minimum of 8W at the speaker. Power will be supplied to both the pre-amplifier and the class AB amplifier.



**Figure 27:** Power amplifier subsystem block diagram.

## **Pre-amplifier Design and Schematics**

There are three different active filters and a summing op-amp to control each tone. Since the woofer plays low frequencies, a low pass filter is suitable. For the mid-range speaker and tweeter, band pass filters can be used. The schematic used for the pre-amplifier is shown below in **Figure 28**.



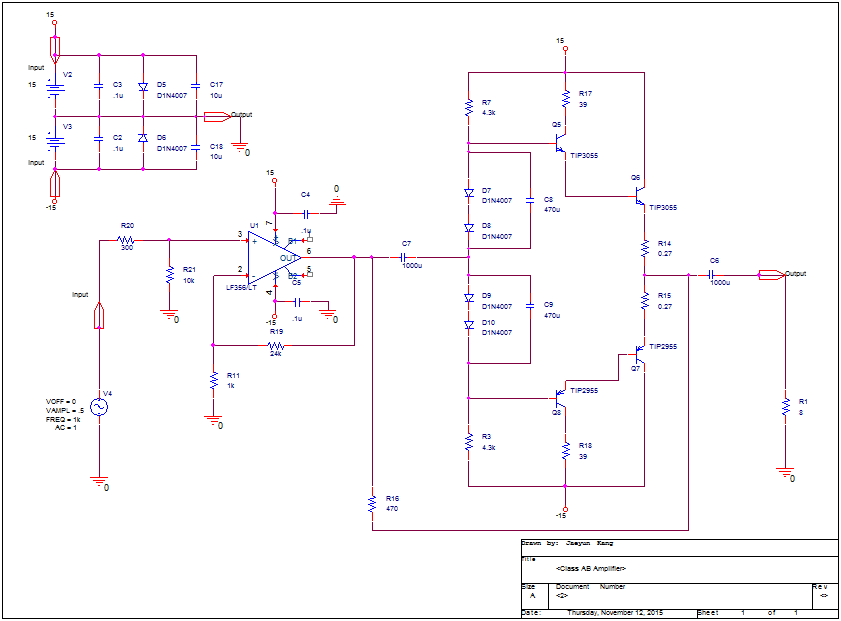
**Figure 28:** Three active filter and one summing op-amp for the pre-amplifier stage.

## **Class AB Amplifier and Schematics**

A class AB amplifier is a combination of Class A and Class B amplifier topologies. A Class AB amplifier provides the sound quality of the Class A topology with the efficiency of Class B. This is achieved by diode biasing and bypass capacitors. This small diode biasing voltage causes both transistors to slightly conduct even when no input signal is present. For small signals, both transistors are active, thus functioning like a Class A amplifier. For large-signals, only one transistor is active for each half of the waveform, thereby operating like a Class B amplifier. This is an ideal choice for high-fidelity speakers.

In the design, as seen from **Figure 29**, Darlington pairs are used. The Darlington pair is a compound structure consisting of two bipolar transistors connected in such a way that the current amplified by the first transistor is amplified further by the second one. This configuration gives a much higher current gain than each transistor taken separately. In addition, an op-amp is used in the design in order to produce high voltage gain and receive feedback.

In the end, the design will meet minimum of 8W RMS because the output Vpp is over 23V in the design of the class AB amplifier. Simply from calculation, the required output Vpp to meet 8W is 22Vpp.



**Figure 29:** Schematic of Class AB amplifier using PNP and NPN transistors by Darlington pairs.

## **Evidence of the Pre-Amplifier**

Vpp at output of each tone control and summing amplifier were measured by changing frequency. Then, dB Magnitude was calculated and plotted on the frequency domain.

**Figure 30:** dB plot of woofer from the prototype.

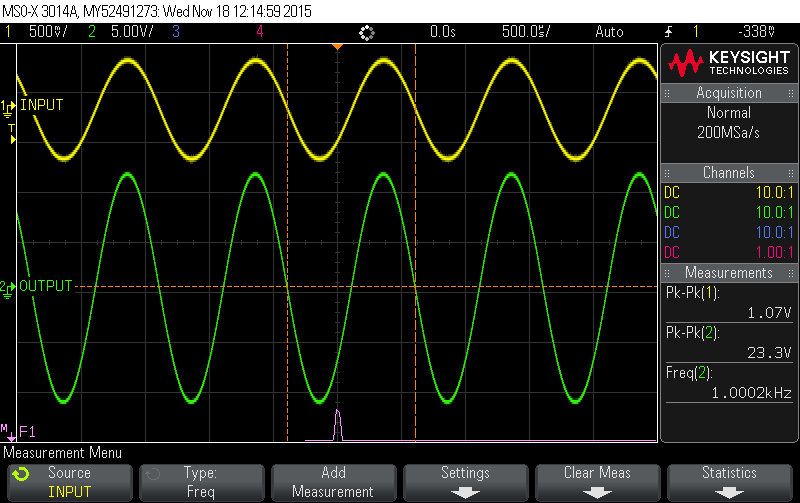
**Figure 31:** dB plot of mid-range from the prototype.

**Figure 32:** dB plot of tweeter from the prototype.

**Figure 33:** dB plot of summing amplifier from the prototype.

## **Evidence of Class AB Amplifier**

**Figure 34** shows the output plot of Class AB amplifier. The input is 1Vpp and the output is 23.3Vpp. This satisfies the power requirement of 8W RMS.



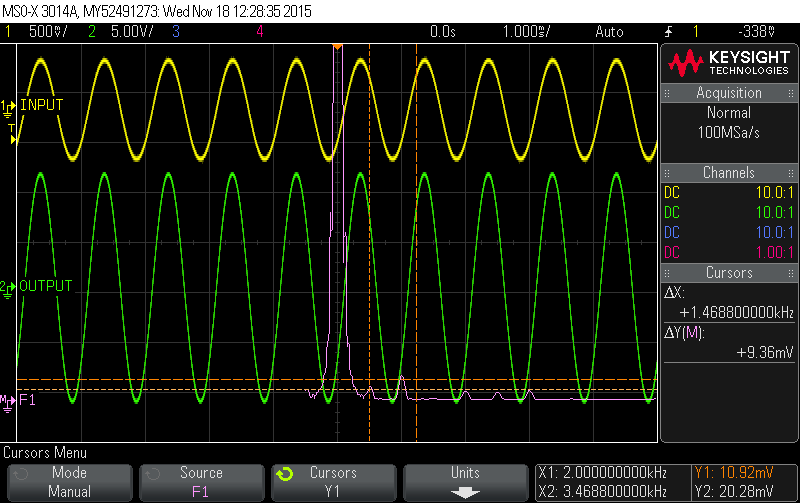
**Figure 34:** Scope plot of Class AB amplifier

**Figure 35** shows FFT plot of Class AB amplifier. Voltage is 10.92mV at 2kHz and 20.28mV at 3kHz with input frequency of 1kHz. Thus, calculation of harmonic distortion is shown below.

2nd harmonic distortion = (0.01092 / 11.65) \* 100% = 0.0937%

3rd harmonic distortion = (.02028 / 11.65) \* 100% = 0.174%

Thus, both 2nd harmonic distortion and 3rd harmonic distortion meet the requirements which are 1% 2nd harmonic distortion and 0.2% 3rd harmonic distortion.



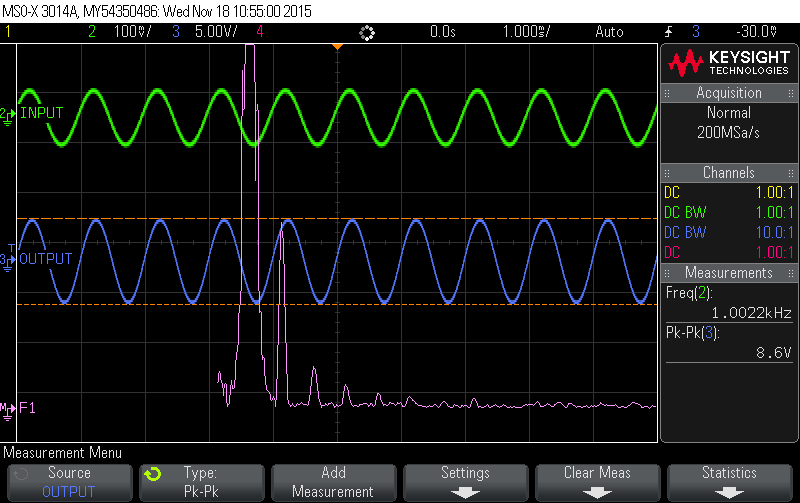
**Figure 35:** Scope plot of Class AB amplifier showing FFT.

## **Integration with other Sub-Systems**

Integrations with reconstruction filter and crossover filter have been examined. The signal coming out of the reconstruction filter was used to as input to the pre-amplifier. This was measured and recorded. The output of the pre-amplifier was also measured and recorded. **Table XX4** shows the results. They are no more than

|  |  |  |  |
| --- | --- | --- | --- |
| **Table XX4:** Integration with Reconstruction Filter | | | |
| Bass (Low Pass) | | | |
| **Frequency (Hz)** | **Input Voltage (V)** | **Output Voltage (V)** | **dB** |
| 50 | 1.02 | 1.01 | -0.08557596 |
| 170 | 1.02 | 1.01 | -0.08557596 |
| 1100 | 1.02 | 79 | 37.78053839 |
| 3500 | 1.04 | 0.36 | -9.214616771 |
| 5100 | 1.04 | 0.257 | -12.14200432 |
|  |  |  |  |
| Mid-Range (Band Pass) | | | |
| **Frequency (Hz)** | **Input Voltage (V)** | **Output Voltage (V)** | **dB** |
| 50 | 1.02 | 0.04 | -28.13080361 |
| 1200 | 1.05 | 0.7 | -3.521825181 |
| 2400 | 1.05 | 1 | -0.423785981 |
| 4800 | 1.07 | 0.68 | -3.9374973 |
| 10000 | 1.04 | 0.334 | -9.86573745 |
|  |  |  |  |
| Tweeter (Band Pass) | | | |
| **Frequency (Hz)** | **Input Voltage (V)** | **Output Voltage (V)** | **dB** |
| 1000 | 1.03 | 0.132 | -17.84526587 |
| 7000 | 1.04 | 0.78 | -2.498774732 |
| 11000 | 1.04 | 0.97 | -0.605232101 |
| 14000 | 1.04 | 0.93 | -0.971007815 |
| 18000 | 1.03 | 0.81 | -2.087044117 |

Integrating from reconstruction filter to crossover filter through the whole power amplifier sub-system is as good as testing the individual sub-system. The FFT is shown in **Figure 36.**



**Figure 36:** The input is the signal coming from the output of the DAC. The output is the signal coming out of the power amplifier with a mid-range values on the tonal controls, which is the normal mode of operation. The output signal has also passed through the reconstruction filter and is integrated with the tonal controls. The THD+N of the output is 0.452% or -46.89dB.

Integrating with amplifier control sub-system have been examined. By connecting wires on prototypes of the pre-amplifier and Class AB amplifier with digital potentiometers on amplifier control prototype as well as all other sub-systems, it was tested through the speaker. The result was that the bass, mid-range, tweeter and total volume could be controlled by TIVA.

## **Testing Plan**

**Table 5** shows the testing plan for the power amplifier subsystem. That is, it lists the requirements and briefly describes how each requirement will be tested.



## **Prototype of the Pre-Amplifier**

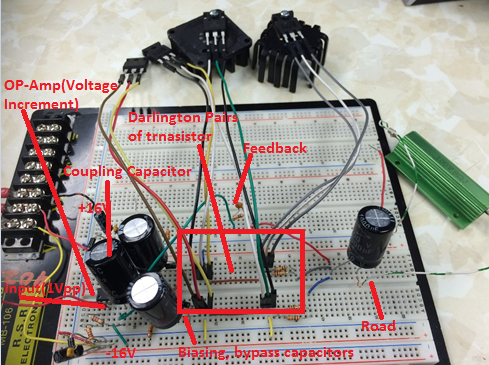
The prototype for the pre-amplifier is shown below in **Figure 37**.



**Figure 37:** Prototype for the pre-amplifier.

## **Prototype of the Class AB Amplifier**

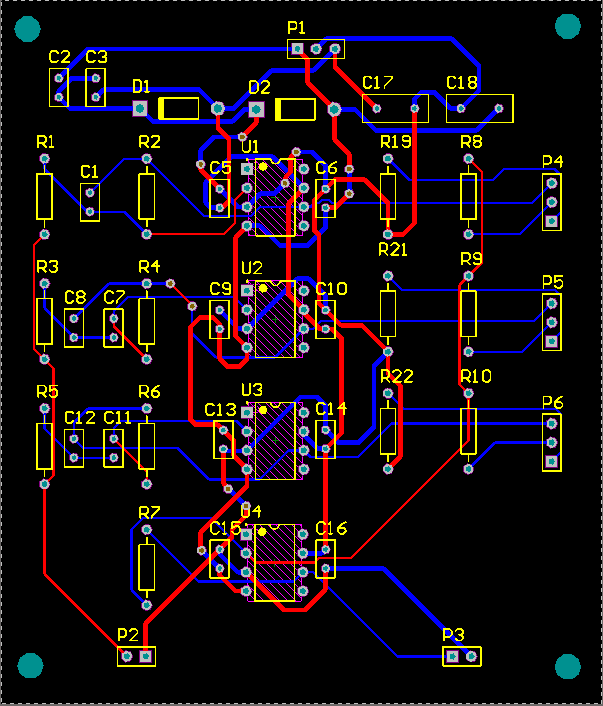
The prototype for Class AB amplifier is shown below in **Figure 38**.



**Figure 38:** Prototype for Class AB amplifier.

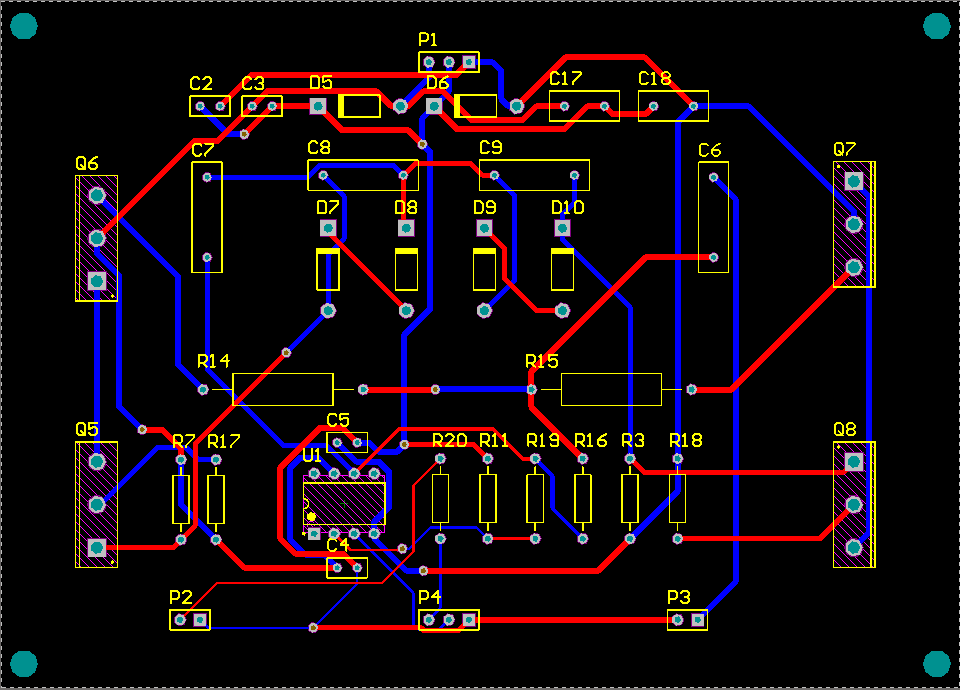
## **PCBs**

PCB design for the pre-amplifier is shown below in **Figure 39**.



**Figure 39:** PCB design for the pre-amplifier.

PCB design for Class AB amplifier is shown below in **Figure 40**.



**Figure 40:** PCB design for Class AB amplifier.

# **Amplifier Controls Subsystem**

## **Subsystem Introduction and Requirements**

Introduction:

The amplifier controls subsystem is responsible for producing a fully functional touch screen display that will allow the user to interface four digital potentiometers while monitoring feedback from the temperature sensor. In the context of the overall Hi-Fi amplifier design, the amplifier controls subsystem must integrate with the power amplifier subsystem. Of the core components, the temperature sensor and the digital potentiometers must reside directly within the power amplifier. They will be required to connect to the TIVA Microcontroller as well as provide constant feedback for display on the Touch Screen GUI. **Figure 40** provides a visual representation of how the components are connected.

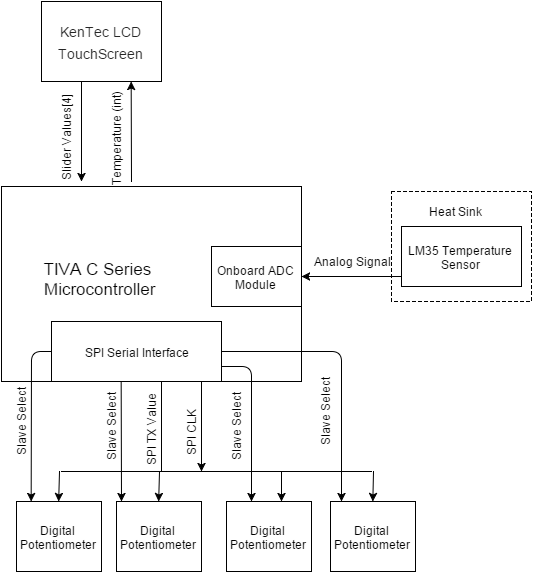
Requirements:

The requirements for this subsystem are

1. Properly monitor and display the reading from the temperature sensor in real time
2. Allow user to adjust the values of the digital potentiometers from the touch screen with high accuracy and minimal delay
3. Create a visually appealing yet functional touch screen GUI for the user to interface
4. Integrate seamlessly into the Amplifier Controls Subsystem

These requirements have been verified through thorough testing of the individual components of the amplifier controls subsystem. Additionally, testing has been done on the integration of the amplifier controls and power amplifier subsystems. The full testing requirements and results can be found in **Figure 49** while integration details can be found the integration section.

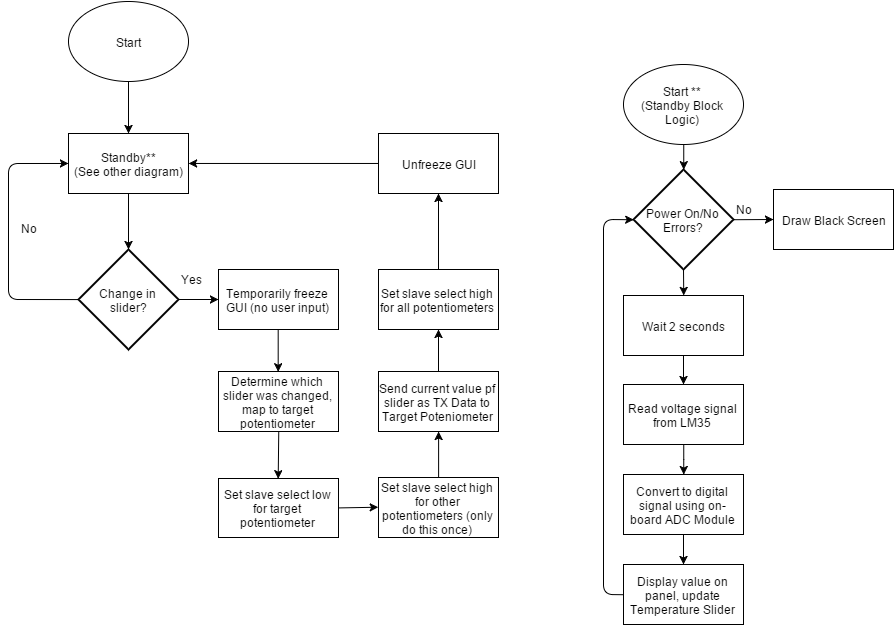
As seen above, requirement 1 relating to the temperature sensor is achieved via..the LM35 temperature sensor connected to the power amplifier heat sink and interfacing the TIVA via an analog variable-voltage signal. Requirement 2 is met by interfacing the four digital potentiometers with both the TIVA Microcontroller as well as with the power amplifier circuit. **Figure 47** demonstrates that the digital potentiometers are both incredibly responsive to user input as well as accurate. Requirement 3 relates to the LCD Touchscreen design. Meeting requirements 1 and 2 indirectly satisfies the ‘functionality’ aspect of requirement three while the visually appealing aspect can be verified in **Figures 45 and 46**. Finally, the fourth requirement for successful and seamless integration with the amplifier controls subsystem is met and described in detail in the “Integration” section of the report.



**Figure 40:** Subsystem block diagram representing the interaction of the primary components

### *TIVA Microcontroller Logic:*

The primary logic required for this subsystem is the logic that converts the user input on the KenTec LCD Touchscreen to corresponding adjustments for the digital potentiometers. **Figure 41** illustrates this particular algorithm in the form of a block diagram while **Figure 42** depicts the algorithm for the temperature sensor.

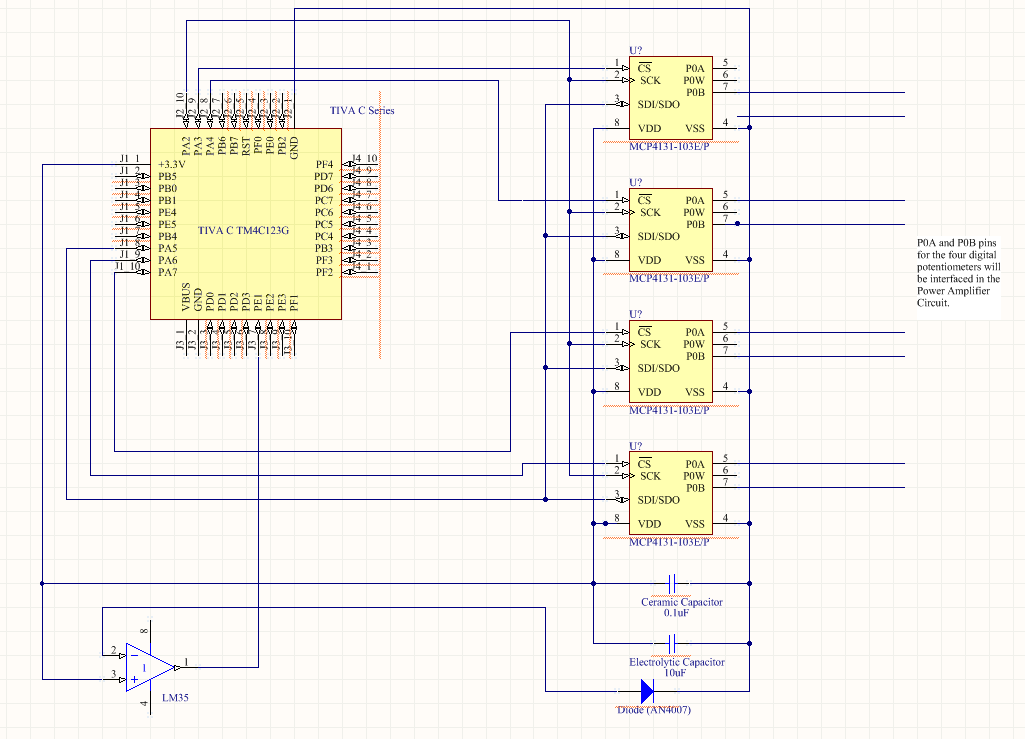


Slider-Potentiometer Mapping Flowchart

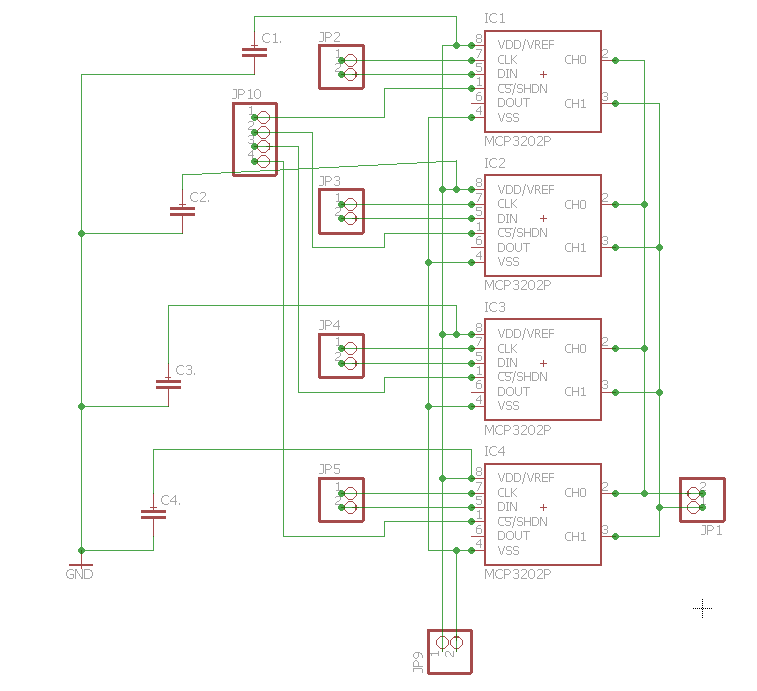
Temperature Sensor Flowchart

**Figures 41 and 42:** Flowcharts for digital potentiometer and temperature sensor logic

## **Schematics**

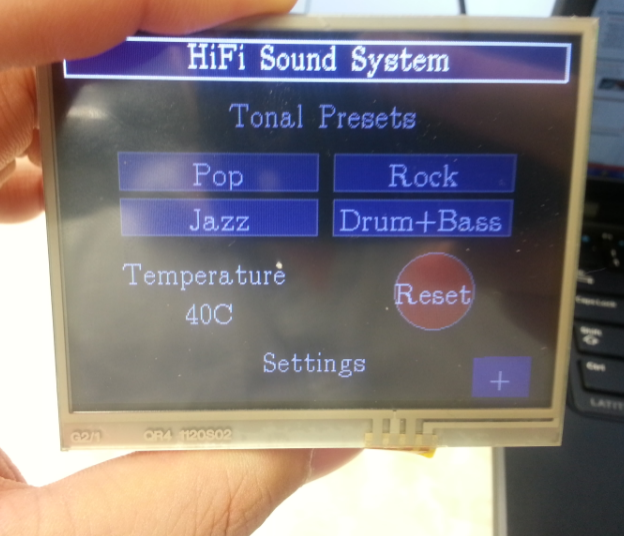


**Figure 43:** Original schematic with TIVA microcontroller included.

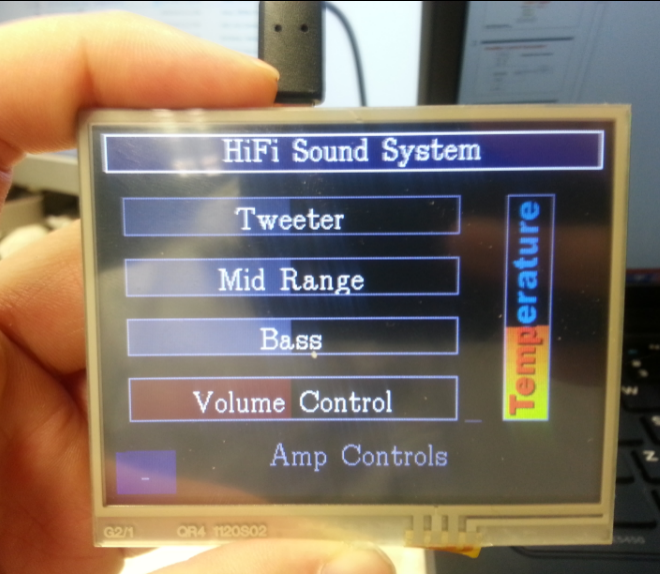


**Figure 44:** Revised schematic (in EAGLE) with only digital potentiometers, served as basis for PCB design (Figure X)

## **Touchscreen GUI Completion Evidence**

****

**Figure 45:** Touchscreen GUI Settings.



**Figure 46**: Touchscreen GUI Amplifier Control.

## **Temperature Sensor**

After integrating the temperature sensor, verification of accuracy was done by comparing it with a handheld laser thermometer. Based on measurements done between 20 degrees Celsius and 30 degrees Celsius, we observed that the LM35 temperature sensor was reading roughly 1.4 degrees under the measured temperature of the laser thermometer on a consistent basis. This meets the metric of keeping the temperature under a +/-2 degree Celsius difference from a reliable standard. Also, since the sensor reading is consistently the same differential from the actual temperature, we are able to consider simply adding 1.4 degrees to our reading prior to displaying it to the touchscreen.

Full integration with the Power Amplifier subsystem has not been completed yet due to the inability to accurately simulate the heatsink without a printed circuit board. Once the PCB for the class AB amplifier arrives, we will make sure to attach the temperature sensor to the heatsink appropriately and verify functionality. For now, however, we are satisfied with our consistent temperature reading as well as the tests we have run with both ambient temperature as well as ‘touching’ the sensor with various objects to simulate contact.

## **Digital Potentiometer Completion Evidence**

In figure 47 below, we verify the functionality of the capability of the TIVA to transmit a correct SPI bus. D15 corresponds to the SPI clock signal while D14 is the SPI Data to be written to all four digital potentiometers. D12 and D13 are directed at the chip select for two of the digital potentiometers. Since chip select is an active low signal, the writing is done only to the chip with a 0 being written to its Chip Select pin. As you can see, D12 is active low while D13 is high, meaning D13 will ignore the SPI Data being written at the time. The inverse is true in the next cycle as D13 becomes an active low signal.

In figure 48, we have a table for the measured resistances of the digital potentiometers at different ‘steps’ as well as comparisons to the ‘expected’ resistances. Our measurements not only verify a high level of accuracy, but also demonstrate that the digital potentiometers are linear (as expected). The largest differential between measured and expected resistance is at the absolute upper limit (near 10KΩ) while the difference at the lower limit is relatively unnoticeable.



Figure 47 – SPI Clock and TX Data w/ Functioning Chip Select

Figure 48 – Measured resistances from digital potentiometers compared to expected values

|  |  |  |
| --- | --- | --- |
| Potentiometer Step Value | Expected Resistance | Measured Resistance |
| 0/128 | 0 KΩ | ~0 KΩ |
| 32/128 | 2.5 KΩ | 2.5 KΩ |
| 64/128 | 5 KΩ | 4.97 KΩ |
| 96/128 | 7.5 KΩ | 7.45 KΩ |
| 128/128 | 10 KΩ | 9.89 KΩ |

## **Integration with other Sub-Systems**

After verifying the functionality of the individual components as well as the subsystem as a whole, the next step was to work towards full integration with the Power Amplifier ISS. This involved taking the four digital potentiometers and replacing the potentiometers in the preamplifier circuit. Since the functionality of the digital potentiometers was already verified before integration, the goal here was to look out for unintended distortion or noise when actively changing resistances. Another test that was conducted was having the preamplifier and the digital potentiometers on the same power source (5V) and ground. Testing indicated that there was virtually no discernable difference in the output when using the digital potentiometers compared to the manual potentiometers used previously in the Power Amplifier subsystem. 

Figure 51 depicts the rough prototypes of both subsystems and how they were connected for integration purposes. In the final product, both PCBs will have appropriate jumpers that will allow us to connect the pins of the potentiometers to the Power Amplifier circuit. Figure Y shows the same input sine wave being run through the Power Amplifier circuit with two different resistances for one of the digital potentiometers. As of now, the only other integration-related task is to verify that the temperature sensor will be reading the heatsink properly. Since the heatsink needs to be integrated with the PCB, which has only been ordered at this point, this test will not be conductible until later. However, the temperature sensor has already been tested very thoroughly at a wide range of temperatures and integration with the heatsink is estimated to take under an hour.

## 

## **Testing Plan/Results**

The testing protocol for the amplifier controls subsystem is shown below in **Figure 49.**

**Figure 49:** Original subsystem performance requirements and testing protocol

|  |  |  |
| --- | --- | --- |
| Component/Function | Testing Plan/Procedure | Target Values/Metrics |
| Temperature sensor | Compare with traditional thermometer or other tool with pre-tested capacity to measure temperature accurately | +/- 2 degrees Celsius in ‘normal’ operation, allowance up to +/- 3 degrees for temperatures on the high end. |
| Digital Potentiometers | Verify resistance value is correct and that potentiometer can handle ‘rapid’ input from the TIVA | Resistance value should have less than a 1% margin for error, ‘rapid’ input is described as ~two changes/second per potentiometer |
| KenTec Touch Screen | Create responsive forms that successfully adjust digital potentiometers | No freezing of GUI, input forms should be able to properly control their respective potentiometers |
| TIVA Microcontroller | No errors with ‘pin sharing’, TIVA able to handle SPI bus to pots without significant lag on screen | Should not be any lag or critical errors relating to resource sharing on TIVA |

### *Detailed Results*

No target metrics or testing requirements have been changed since the preliminary design review. Optimization of the amplifier controls subsystem has allowed numerous original target values to be surpassed. The summary of the results can be viewed in **Figure 50** below.

LM35 Temperature Sensor – Consistently reading a temperature 1.4 degrees Celsius below what a laser thermometer reads at a wide range of temperatures. The 1.4 degree offset is very consistent to the point of being nearly exact, so it would be suitable to simply add 1.4 to the calculated result before displaying it to the touchscreen.

Digital Potentiometers - Resistance is correctly changing at all 128 predefined steps. Steps have been verified to be linear and the TIVA is able to send the SPI bus fast enough to keep up with user input. Exact timing results are not available due to a lack of precise timing tools, but the digital potentiometers are able to go from the max step (128/128) to the lowest step (1/128) with a swipe of a finger (under a half second in time). This means the TIVA is able to handle digital pot changes of roughly 128 steps in under a half second, which is significantly better than the original target metric.

Touchscreen and TIVA – Significant optimization of pin declarations and logic has eliminated concerns relating to resource and pin sharing as well as ‘laggy’ elements on the touchscreen. Therefore, the original criteria to avoid these issues has been satisfied.

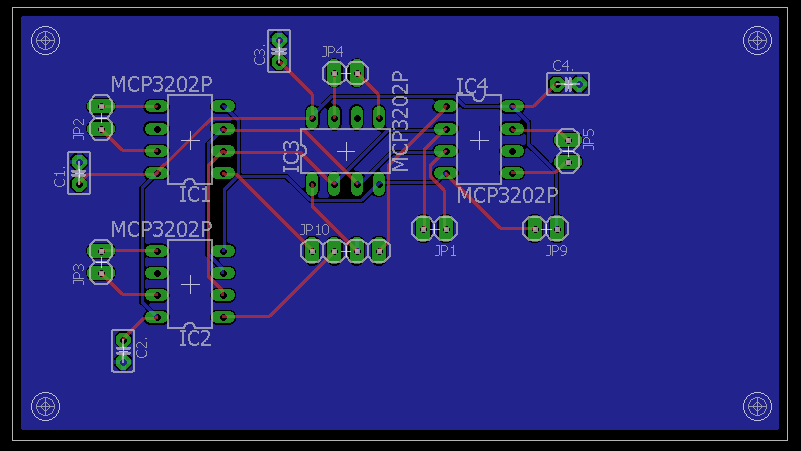
**Figure 50:** Summary of original metrics for testing as well as the results

|  |  |  |
| --- | --- | --- |
| Component/Function | Original Target Metric | Actual Result |
| Temperature sensor | +/- 2 degrees Celsius in ‘normal’ operation | LM35 is reading a temperature that is consistently -1.4 degrees Celsius when compared to laser thermometer |
| Digital Potentiometers | Resistance value should have less than a 1% margin for error, ‘rapid’ input is described as ~two changes/second per potentiometer | Resistance is accurate and linear in the range of 0.3K to 9.89K (consistent with spec sheet). Able change values significantly faster than two changes per second (estimated performance of > 128 values/second) |
| KenTec Touch Screen | No freezing of GUI, input forms should be able to properly control their respective potentiometers | Slight GUI pauses and freezes are very rare to the point of being almost completely unreplaceable |
| TIVA Microcontroller | Should not be any lag or critical errors relating to resource sharing. | Optimized code does not share any GPIO resources so resource/pin sharing is a complete non-issue. |



**Figure 51:** Prototype of amplifier control design on breadboard, integrated with the pre-amplifier prototype.

## **PCB**



**Figure 52**: Completed and submitted PCB. Includes four MCP4131 Digital Potentiometers, jumpers for interfacing with the TIVA and power amplifier subsystem, power and ground pins, and decoupling capacitors.

# **References**

[1] *ECE 40200 EE Design Projects Fall 2015 Course Handout*, 3rded., Purdue University, West Lafayette, IN, 2015, pp. 13-16*.*

[2] *Introduction to Digital System Design: Module 3, Sequential Logic Circuits*, Purdue University, West Lafayette, IN, 2015, pp. 206-340.

[3] R. Downs, “A low noise, low distortion design for antialiasing and anti-imaging filters,” Burr Brown, Tucson, AZ, 2000.

[4] Robert Nicoletti, “How to Select the Best Audio Amplifier for Your Design,” Audio Solution Group, Maxim Integrated, May 24, 2013.

# **Appendix A – List of Known Costs**



# **Appendix B – Specification Sheets**

Specification sheets are provided for the major devices used:

* PCM2706 USB Interface
* 74F675A Shift Register
* 74HC40105 FIFO Chip
* ispMACH4256ZE CPLD
* PCM1702 DAC
* OPA604 Op-Amp
* Tiva C Series TM4C123G LaunchPad
* LM35 Temperature Sensor
* MCP4131 Digital Potentiometer
* KenTec LCD Touchscreen Display
* TIP2955/3055 Transistor
* LM356N Op-Amp