ULN2003V12 7-Channel Relay and Inductive Load Sink Driver

1 Features

- 7-Channel High Current Sink Drivers
- Supports Up to 20-V Output Pullup Voltage
- Low Output V_{OL} of 0.6 V (Typical) With:
  - 100-mA (Typical) Current Sink per Channel at 3.3-V Logic Input(1)
  - 140-mA (Typical) Current Sink per Channel at 5-V Logic Input(1)
- Compatible to 3.3-V and 5-V Microcontrollers and Logic Interface
- Internal Free-Wheeling Diodes for Inductive Kick-Back Protection
- Input Pulldown Resistors Allows Tri-Stating the Input Driver
- Input RC-Snubber to Eliminate Spurious Operation in Noisy Environment
- Low Input and Output Leakage Currents
- ESD Protection Exceeds JESD 22:
  - 2-kV HBM, 500-V CDM

(1) Total current sink may be limited by the internal junction temperature, absolute maximum current levels, and so forth (see *Electrical Characteristics* for details).

2 Applications

- Relay and Inductive Load Driver
- White Goods
- Factory and Home Automation
- Lamp and LED Displays
- Logic Level Shifter

3 Description

The ULN2003V12 device is a low-power upgrade of TI's popular ULN2003 family of 7-channel Darlington transistor array. The ULN2003V12 sink driver features 7 low-output impedance drivers that minimize on-chip power dissipation. When driving a typical 12-V relay coil, a ULN2003V12 can dissipate up to 12 times lower power than an equivalent ULN2003A. The ULN2003V12 driver is pin-to-pin compatible with ULN2003 family of devices.

The ULN2003V12 supports 3.3-V to 5-V CMOS logic input interface thus making it compatible to a wide range of microcontrollers and other logic interfaces. The ULN2003V12 also supports other logic input levels, like TTL or 1.8 V. Each output of the ULN2003V12 features an internal free-wheeling diode connected in a common-cathode configuration at the COM pin.

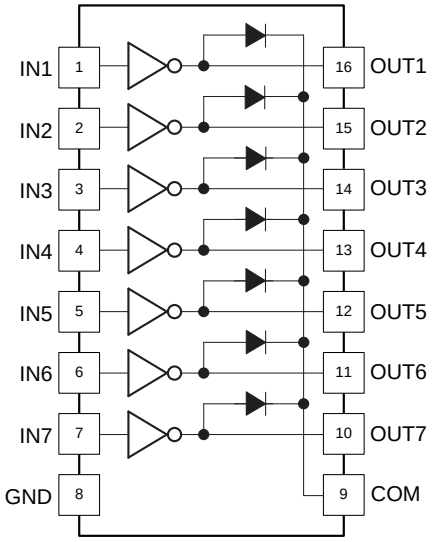
The ULN2003V12 provides flexibility of increasing current sink capability through combining several adjacent channels in parallel. Under typical conditions the ULN2003V12 can support up to 1 A of load current when all 7-channels are connected in parallel.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ULN2003V12D	SOIC (16)	9.90 mm × 3.91 mm
ULN2003V12PW	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2012) to Revision C **Page**

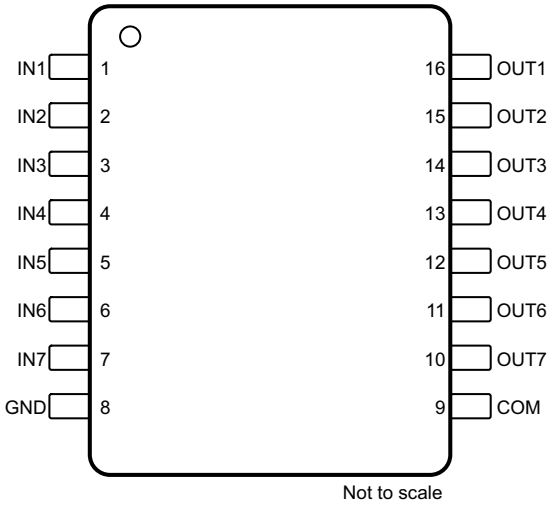
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed θ_{JA} values From: 75°C/W To: 104.8°C/W (D) and From: 95°C/W To: 130.6°C/W (PW) ... 4
- Changed θ_{JC} values From: 46°C/W To: 63.7°C/W (D) and From: 49°C/W To: 62.7°C/W (PW) ... 4

Changes from Revision A (July 2012) to Revision B **Page**

- Added Details to Switching Parameters ... 5

5 Pin Configuration and Functions

D and PW Packages
16-Pin SOIC and TSSOP
Top View



Not to scale

Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	IN1	I	Channel 1 input
2	IN2	I	Channel 2 input
3	IN3	I	Channel 3 input
4	IN4	I	Channel 4 input
5	IN5	I	Channel 5 input
6	IN6	I	Channel 6 input
7	IN7	I	Channel 7 input
8	GND	—	Supply ground
9	COM	—	Common cathode node for flyback diodes (required for inductive loads)
10	OUT7	O	Channel 7 output
11	OUT6	O	Channel 6 output
12	OUT5	O	Channel 5 output
13	OUT4	O	Channel 4 output
14	OUT3	O	Channel 3 output
15	OUT2	O	Channel 2 output
16	OUT1	O	Channel 1 output

(1) I = Input and O = Output

6 Specifications

6.1 Absolute Maximum Ratings

Specified at T_J = –40°C to 125°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pins IN1 – IN7 to GND voltage, V_{IN}		–0.3	5.5	V
Pins OUT1 – OUT7 to GND voltage, V_{OUT}			20	V
Pin COM to GND voltage, V_{COM}			20	V
Maximum GND-pin continuous current, I_{GND}	100ºC < T_J < 125°C		700	mA
	T_J < 100°C		1	A
Operating virtual junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{OUT}	Channel off-state output pullup voltage			16	V
V_{COM}	COM pin voltage			16	V
$I_{OUT(ON)}$(1)	Per channel continuous sink current	VINx = 3.3 V		100(1)	mA
		VINx = 5 V		140(1)	
T_J	Operating junction temperature		–40	125	ºC

(1) See *Absolute Maximum Ratings* for T_J dependent absolute maximum GND-pin current.

6.4 Thermal Information

THERMAL METRIC(1)		ULN2003V12		UNIT
		D (SOIC)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104.8	130.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.7	62.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.3	76.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.1	15.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.1	75.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values are at T_J = 25°C, minimum and maximum values over the recommended junction temperature range T_J = –40°C to 125°C, and over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUTS IN1 THROUGH IN7 PARAMETERS						
$V_{I(ON)}$	IN1–IN7 logic high input voltage	V_{pullup} = 3.3 V, R_{pullup} = 1 kΩ, I_{OUTX} = 3.2 mA	1.65			V
$V_{I(OFF)}$	IN1–IN7 logic low input voltage	V_{pullup} = 3.3 V, R_{pullup} = 1 kΩ, I_{OUTX} < 20 µA			0.6	
$I_{I(ON)}$	IN1–IN7 ON state input current	V_{pullup} = 12 V, VIN_x = 3.3 V		12	25	µA
$I_{I(OFF)}$	IN1–IN7 OFF state input leakage	V_{pullup} = 12 V, VIN_x = 0 V			250	nA
OUTPUTS OUT1 THROUGH OUT7 PARAMETERS						
$V_{OL(VCE-SAT)}$	OUT1–OUT7 low-level output voltage	V_{INX} = 3.3 V, I_{OUTX} = 20 mA		0.12	0.15	V
		V_{INX} = 3.3 V, I_{OUTX} = 100 mA		0.6	0.75	
		V_{INX} = 5 V, I_{OUTX} = 20 mA		0.09	0.11	
		V_{INX} = 5 V, I_{OUTX} = 140 mA		0.6	0.75	
$I_{OUT(ON)}$	OUT1–OUT7 ON-state continuous current at V_{OUTX} = 0.6 V (1)(2)	V_{INX} = 3.3 V, V_{OUTX} = 0.6 V	80	100		mA
		V_{INX} = 5 V, V_{OUTX} = 0.6 V	95	140		
$I_{OUT(OFF)(ICEX)}$	OUT1–OUT7 OFF-state leakage current	V_{INX} = 0 V, V_{OUTX} = V_{COM} = 16 V		0.5		µA
SWITCHING PARAMETERS (3)(4)						
t_{PHL}	OUT1–OUT7 logic high propagation delay	V_{INX} = 3.3 V, V_{pullup} = 12 V, R_{pullup} = 1 kΩ		50	70	ns
t_{PLH}	OUT1–OUT7 logic low propagation delay	V_{INX} = 3.3V, V_{pullup} = 12 V, R_{pullup} = 1 kΩ		121	140	ns
$t_{CHANNEL}$	Channel-to-channel delay	Over recommended operating conditions and with same test conditions on channels.		15	50	ns
R_{PD}	IN1–IN7 input pulldown resistance		210	300	390	kΩ
ζ	IN1–IN7 input filter time constant			9		ns
C_{OUT}	OUT1–OUT7 output capacitance	V_{INX} = 3.3 V, V_{OUTX} = 0.4 V		15		pF
FREE-WHEELING DIODE PARAMETERS (4)(5)						
VF	Forward voltage drop	$I_{F\text{-}peak}$ = 140 mA, VF = V_{OUTx} – V_{COM}		1.2		V
$I_{F\text{-}peak}$	Diode peak forward current			140		mA

(1) The typical continuous current rating is limited by V_{OL}= 0.6 V. Whereas, absolute maximum operating continuous current may be limited by the Thermal performance parameters listed in the *Thermal Information* and other reliability parameters listed in *Recommended Operating Conditions*.
(2) See *Absolute Maximum Ratings* for T_J dependent absolute maximum GND-pin current.
(3) Rise and fall propagation delays, t_{PHL} and t_{PLH}, are measured between 50% values of the input and the corresponding output signal amplitude transition.
(4) Specified by design only. Validated during qualification. Not measured in production testing.
(5) Not rated for continuous current operation. For higher reliability, use an external freewheeling diode for inductive loads resulting in more than specified maximum free-wheeling. Diode peak current across various temperature conditions.

6.6 Typical Characteristics

T_A = 25ºC

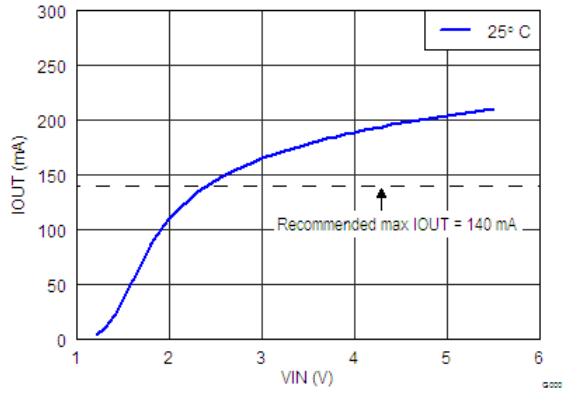


Figure 1. Load Current, 1-Channel at V_{OL} = 0.6 V

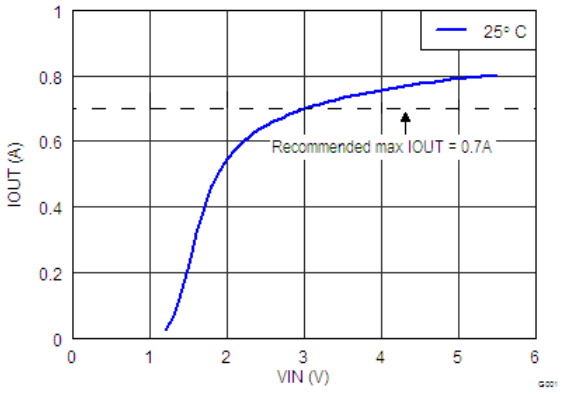


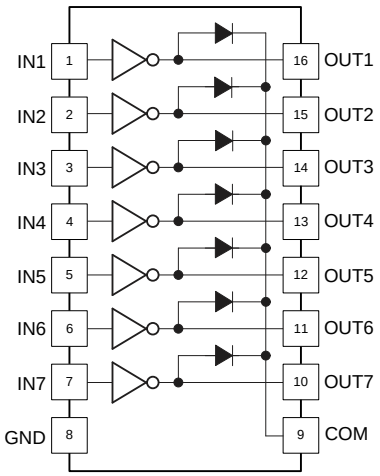
Figure 2. Load Current, 7-Channels in Parallel at V_{OL} = 0.6 V

7 Detailed Description

7.1 Overview

The ULN2003V12 device is a seven channel low-side NMOS driver capable of driving 100-mA Load with 3-V input drive voltage through each channel. This device can drive relays, LEDs, or resistive loads up to 16 V. The ULN2003V12 supports 3.3-V to 5-V CMOS logic input interface, thus making it compatible to a wide range of microcontrollers and other logic interfaces. The ULN2003V12 features an improved input interface that minimizes the input DC current drawn from the external drivers. The ULN2003V12 features an input RC snubber that greatly improves its performance in noisy operating conditions. The ULN2003V12 channel inputs feature an internal input pulldown resistor, thus allowing input logic to be tri-stated. The ULN2003V12 may also support other logic input levels (for example, TTL and 1.8 V).

7.2 Functional Diagram



7.3 Feature Description

As shown in Figure 3, each output of the ULN2003V12 features an internal free-wheeling diode connected in a common-cathode configuration at the COM pin. The ULN2003V12 provides flexibility of increasing current sink capability through combining several adjacent channels in parallel. Under typical conditions, the ULN2003V12 can support up to 1 A of load current when all 7-channels are connected in parallel. The ULN2003V12 can also be used in a variety of other applications requiring a sink driver.

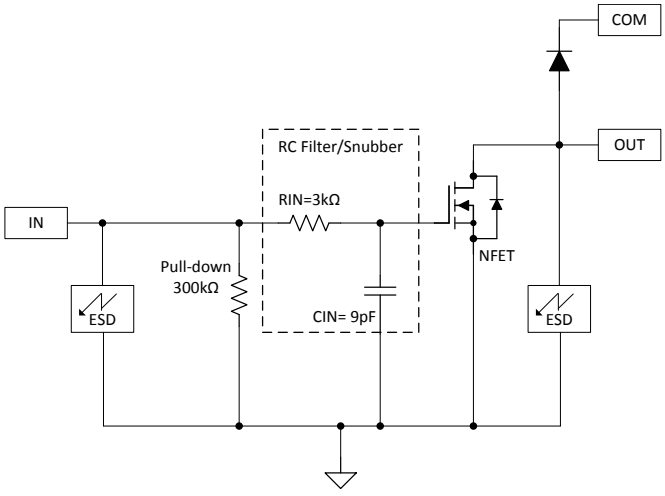


Figure 3. Channel Block Diagram

Feature Description (continued)

7.3.1 TTL and Other Logic Inputs

ULN2003V12 input interface is specified for standard 3-V and 5-V CMOS logic interface. However, ULN2003V12 input interface may support other logic input levels as well. See Figure 1 and Figure 2 to establish V_{OL} and the corresponding typical load current levels for various input voltage ranges. See *Applications and Implementation* for an implementation to drive 1.8-V relays using ULN2003V12.

7.3.2 Input RC Snubber

ULN2003V12 features an input RC snubber that helps prevent spurious switching in noisy environment. Connect an external 1-kΩ to 5-kΩ resistor in series with the input to further enhance ULN2003V12's noise tolerance.

7.3.3 High-impedance Input Drivers

ULN2003V12 features a 300-kΩ input pulldown resistor. The presence of this resistor allows the input drivers to be tri-stated. When a high-impedance driver is connected to a channel input the ULN2003V12 detects the channel input as a low level input and remains in the OFF position. The input RC snubber helps improve noise tolerance when input drivers are in the high-impedance state.

7.4 Device Functional Modes

Table 1 lists the functional modes for this device.

Table 1. ULN2003V12 Function Table(1)

INPUT (IN1 TO IN7)	OUTPUT (OUT1 TO OUT7)
L	Z
H	L
Z	Z

(1) L = Low-level (GND), H= High-level, Z= High-impedance

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Peripheral drivers such as the ULN2003V12 are primarily used in the following applications:

- Stepper Motor Driving
- Relay and Solenoid Driving
- LED Driving
- Logic Level Shifting

Peripheral Drivers are not limited to one specific application at a time, but can be used for all of these applications simultaneously. For example, one device could enable driving one stepper motor, driving one relay, driving an LED, and shifting a 3.3-V logic signal to a 12-V logic signal at the same time.

8.2 Typical Applications

8.2.1 Unipolar Stepper Motor Driver

The Figure 4 shows an implementation of ULN2003V12 for driving a unipolar stepper motor.

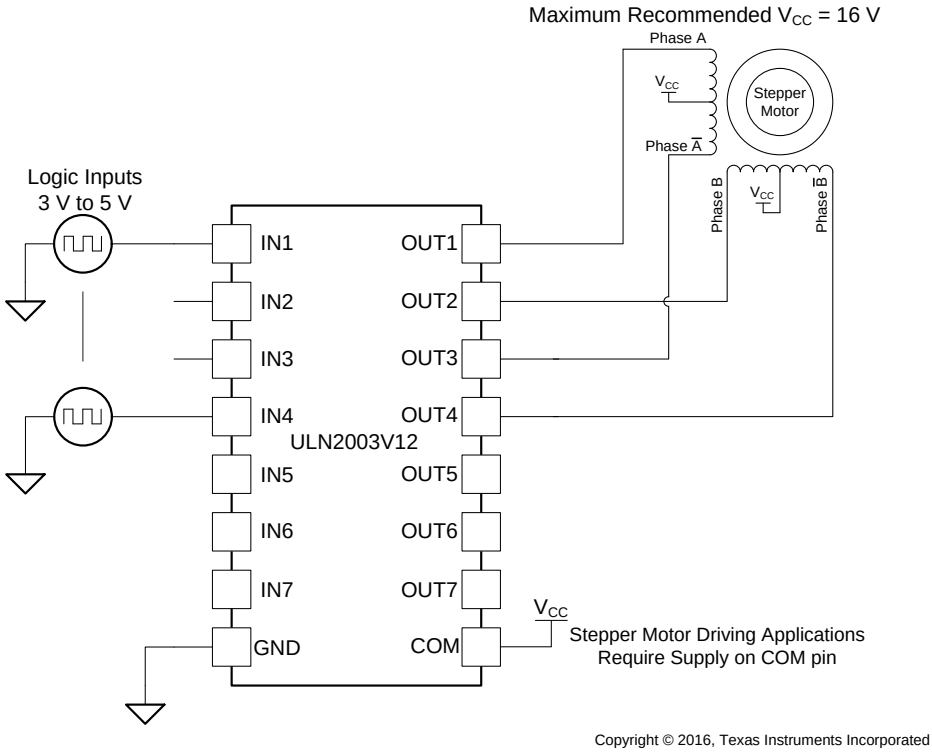


Figure 4. ULN2003V12 as a Stepper Motor Driver

Typical Applications (continued)

8.2.1.1 Design Requirements

The unconnected input channels can be used for other functions. When an input pin is left open, the internal 300-kΩ pulldown resistor pulls the respective input pin to GND potential. For higher noise immunity use an external short across an unconnected input and GND pins. See *Stepper Motor Driving with Peripheral Drivers* (SLVA767) for additional information regarding stepper motor driving.

8.2.1.2 Application Curves

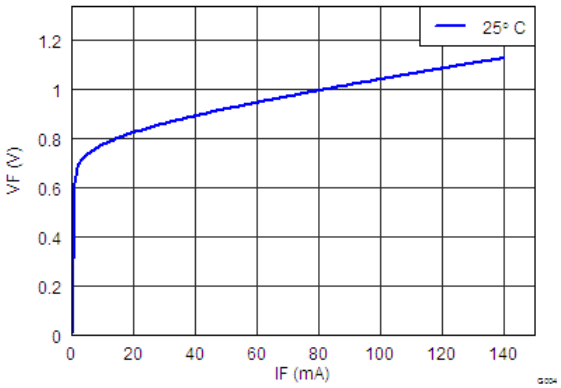


Figure 5. Freewheeling Diode VF vs IF

8.2.2 Inverting Logic Level Shifter

To use ULN2003V12 as an open-drain inverting logic level shifter, configure the device as shown in Figure 6. The device input and output logic levels can also be set independently. When using different channel input and output logic voltages, connect the ULN2003V12 COM pin to the maximum voltage.

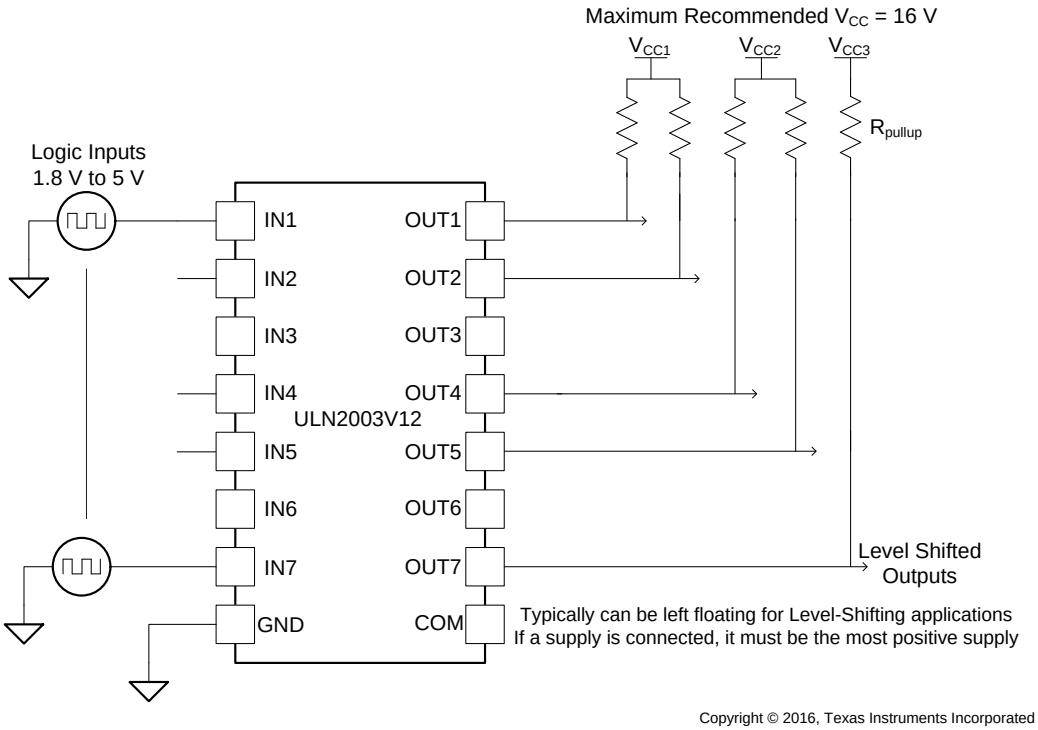


Figure 6. ULN2003V12 as Inverting Logic Level Shifter

Typical Applications (continued)

8.2.2.1 Design Requirements

ULN2003V12 can be used in digital applications requiring logic level shifting up to 16 V at the output side. Because the device pulls the output transistor low when input is high, this configuration is useful for applications requiring inverting logic with the level shifting operation.

8.2.2.2 Detailed Design Procedure

To operate in level shifting operation, timing and propagation delay must be kept in mind. Depending on the pullup resistors at the output ULN2003V12 exhibits different propagation delays. The choice of pullup resistor is dependent on the drive required at the output. The device can pull output to ground with the output transistor, but to transition from low to high output resistor plays a critical role. If high drive at output is required, use Equation 1 to calculate a lower resistance.

$$R_{Pullup} = OUT1\_VSUP / I_{Drive} \quad (1)$$

For example, a drive of 5 mA is required at the output for 1.8-V to 5-V translation application.

$$R_{Pullup} = OUT1\_VSUP / I_{Drive} = 5 / 0.005 = 1k \quad (2)$$

8.2.3 Maximum Supply Selector

The Figure 7 implements a maximum supply selector along with a 4-channel logic level shifter using a single ULN20003V12.

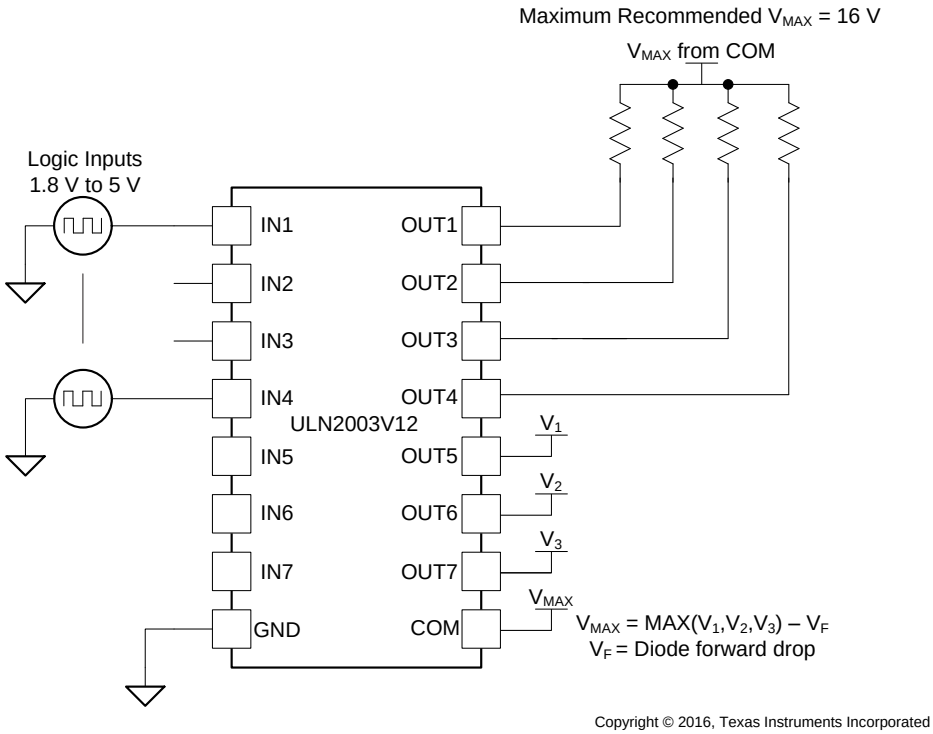


Figure 7. ULN2003V12 as a Maximum Supply Selector

8.2.3.1 Design Requirements

This setup configures ULN2003V12's channel clamp diodes OUT5 to OUT7 in a diode-OR configuration and thus the maximum supply among V_1, V_2, and V_3 becomes available at the COM pin. The maximum supply is then used as a pullup voltage for level shifters. Limit the net GND pin current to less than 100-mA DC to ensure reliability of the conducting diode. The unconnected inputs IN5 to IN7 are pulled to GND potential through 300-kΩ internal pulldown resistor.

Typical Applications (continued)

8.2.4 Constant Current LED Driver

When configured as per Figure 8, the ULN2003V12 outputs OUT1 to OUT6 act as independent constant current sources.

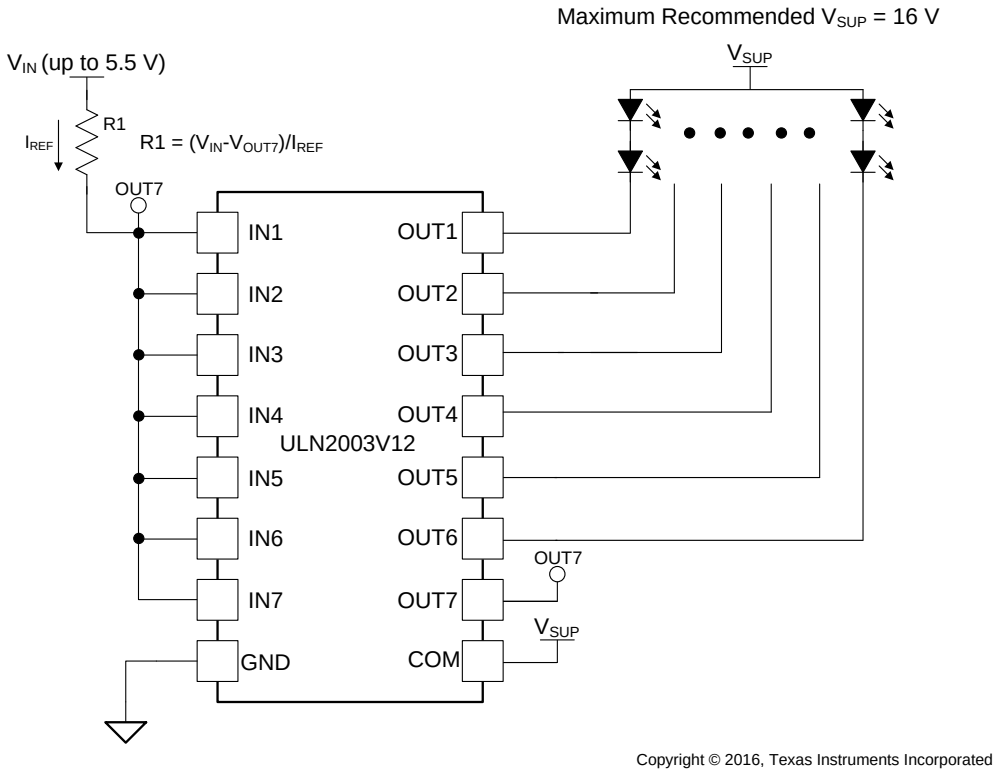


Figure 8. ULN2003V12 as a Constant Current Driver

8.2.4.1 Design Requirements

The current flowing through the resistor R1 is mirrored on all other channels. To increase the current sourcing connect several output channels in parallel. To ensure best current mirroring, set voltage drop across connected load such that VOUTx matches VOUT7.

Typical Applications (continued)

8.2.5 NOR Logic Driver

Figure 9 shows a NOR Logic driver implementation using the ULN2003V12 device.

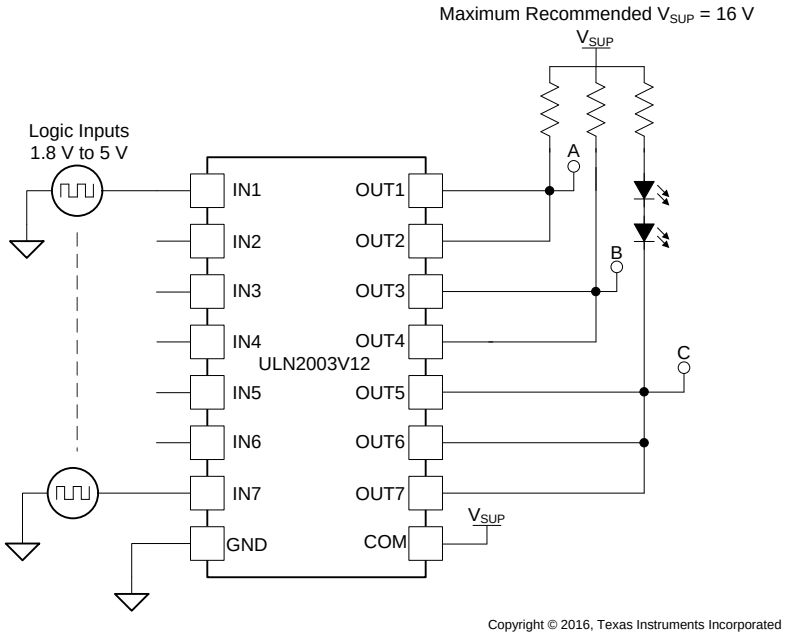


Figure 9. ULN2003V12 as a NOR driver

8.2.5.1 Design Requirements

The output channels sharing a common pullup resistor implement a logic NOR of the respective channel inputs. Node A is controlled by inputs IN1 and IN2 as described in Table 2 (Positive Logic Function: $A = \overline{IN1+IN2}$). Node B is controlled by inputs IN3 and IN4 as described in Table 3 (Positive Logic Function: $B = \overline{IN3+IN4}$). Node C is controlled by inputs IN5, IN6, and IN7 as described in Table 4 (Positive Logic Function $C = \overline{IN5+IN6+IN7}$).

Table 2. Output A Function Table

IN1	IN2	A
L	L	H
X	H	L
H	X	L

Table 3. Output B Function Table

IN3	IN4	B
L	L	H
X	H	L
H	X	L

Table 4. Output C Function Table

IN5	IN6	IN7	C	LED
L	L	L	H	OFF
X	X	H	L	ON
X	H	X	L	ON
H	X	X	L	ON

9 Power Supply Recommendations

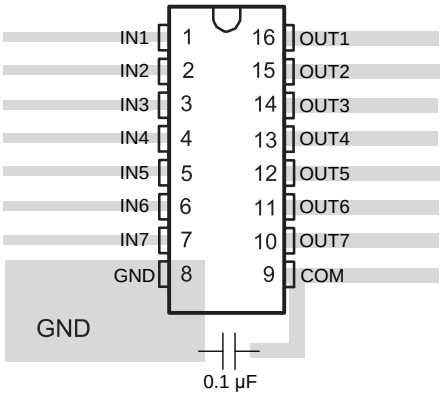
The COM pin is the power supply pin of this device to power the gate drive circuitry. Although not required, TI recommends putting a bypass capacitor of 0.1 µF across the COM pin and GND pin.

10 Layout

10.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive ULN2003V12. Take care to separate the input channels as much as possible, as to eliminate cross-talk. TI recommends thick traces for the output to drive high currents that may be required. Wire thickness can be determined by the trace material's current density and desired drive current. Because all of the channels currents return to a common ground, it is best to size that trace width to be very wide. Some applications require up to 1 A.

10.2 Layout Example



10.3 Thermal Considerations

10.3.1 On-chip Power Dissipation

Use Equation 3 to calculate ULN2003V12 on-chip power dissipation P_D.

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li} \quad (3)$$

where

- N is the number of channels active together
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}

10.3.2 Thermal Reliability

TI recommends limiting the ULN2003V12 IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use Equation 4 to calculate the maximum allowable on-chip power dissipation for a target IC junction temperature.

$$PD_{(MAX)} = \left(T_{J(MAX)} - T_A\right) \Big/ \theta_{JA} \quad (4)$$

where

- $T_{J(MAX)}$ is the target maximum junction temperature
- T_A is the operating ambient temperature
- θ_{JA} is the package junction to ambient thermal resistance

11 Device and Documentation Support

11.1 Documentation Support

For related documentation see the following:

Stepper Motor Driving with Peripheral Drivers (SLVA767)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ULN2003V12DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	U2003V12	Samples
ULN2003V12PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	U2003V12	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

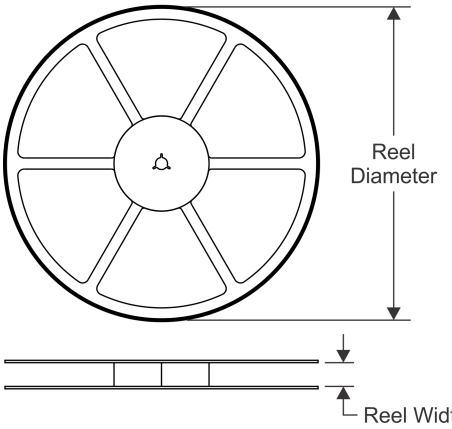
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

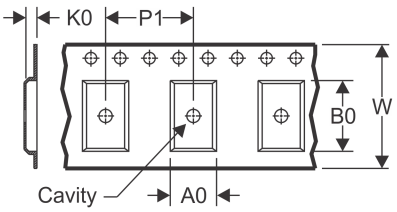
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

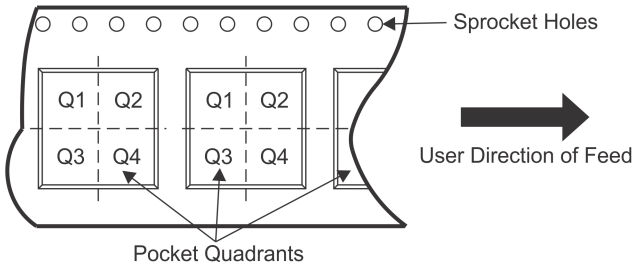


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

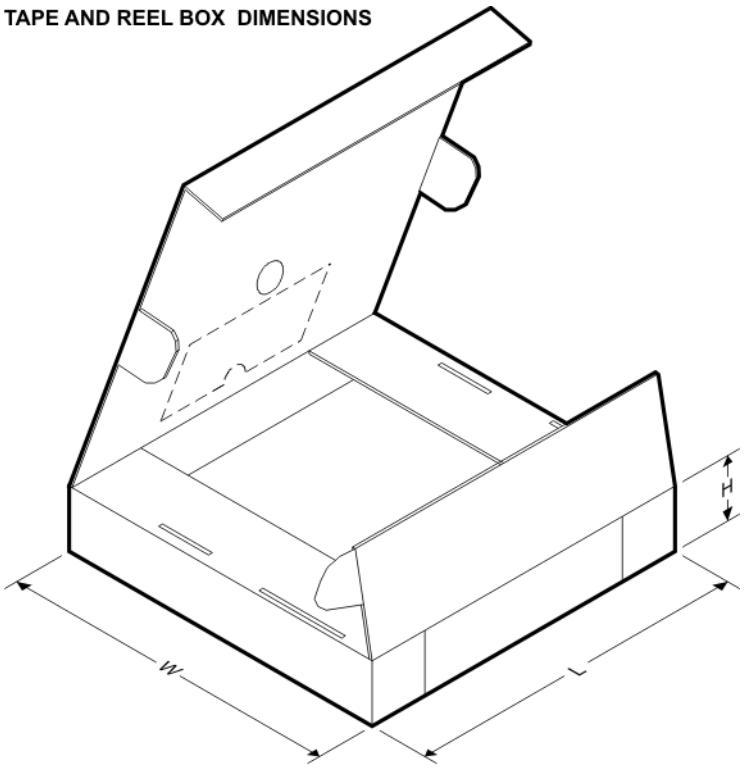
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2003V12DR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003V12PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

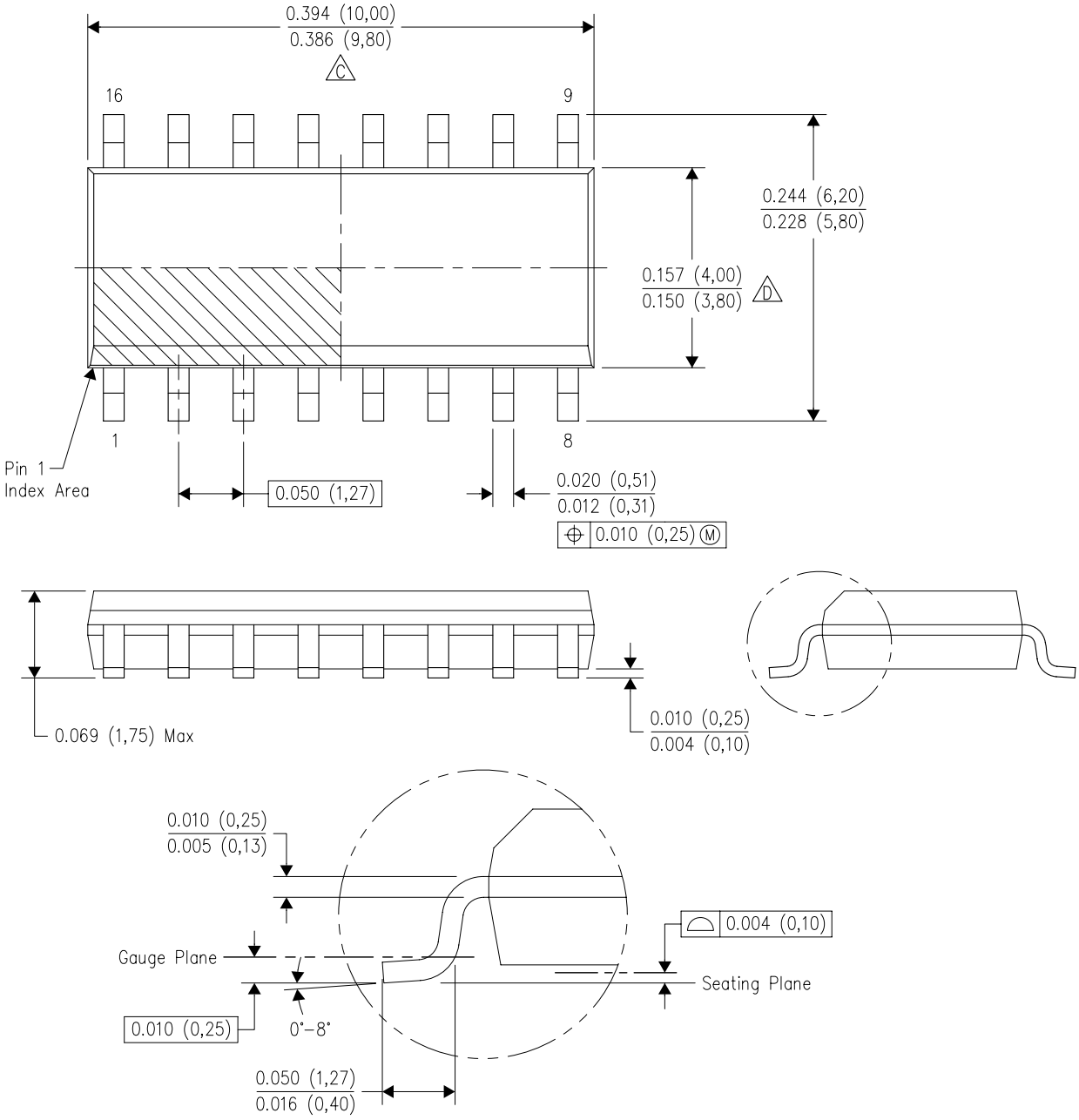
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

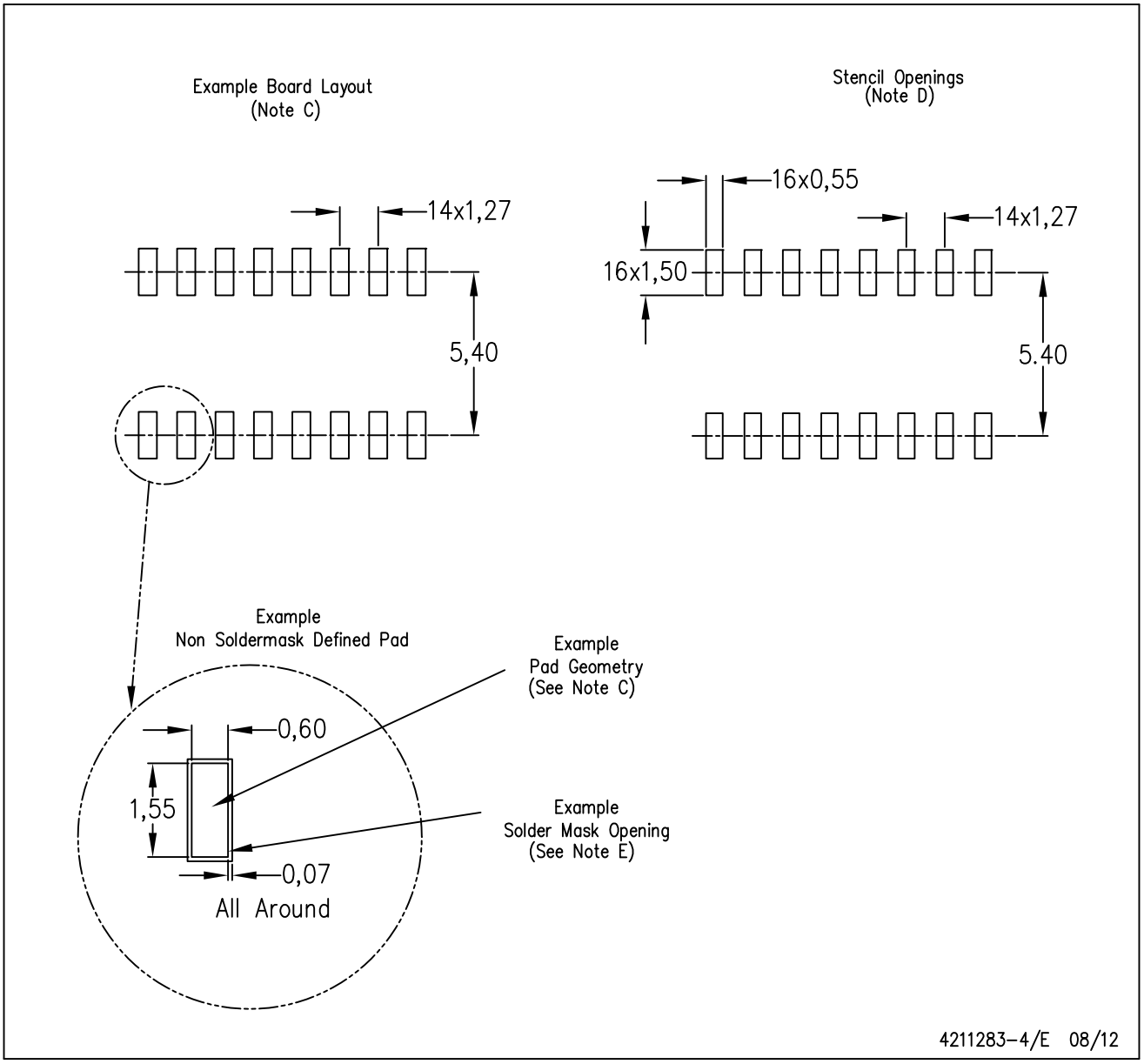
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2003V12DR	SOIC	D	16	2500	364.0	364.0	27.0
ULN2003V12PWR	TSSOP	PW	16	2000	364.0	364.0	27.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



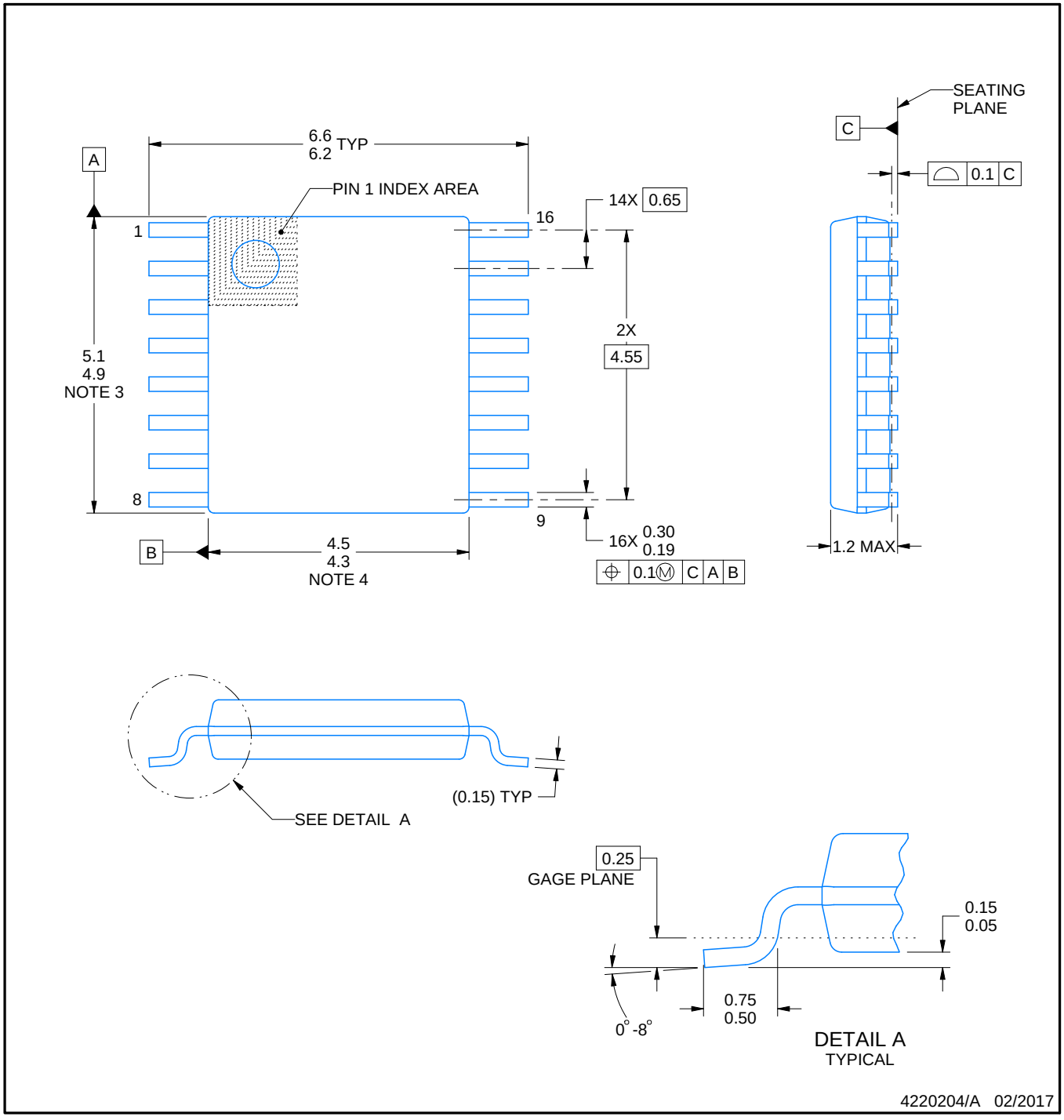
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

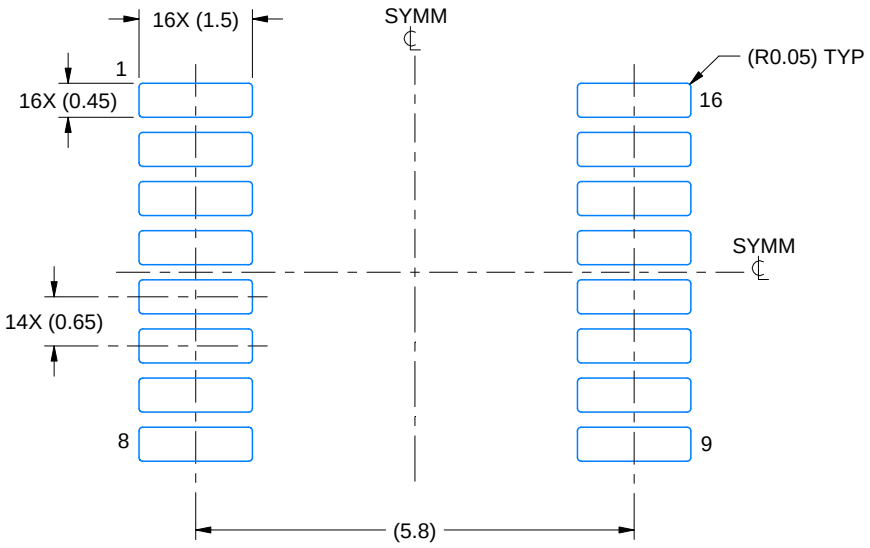
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

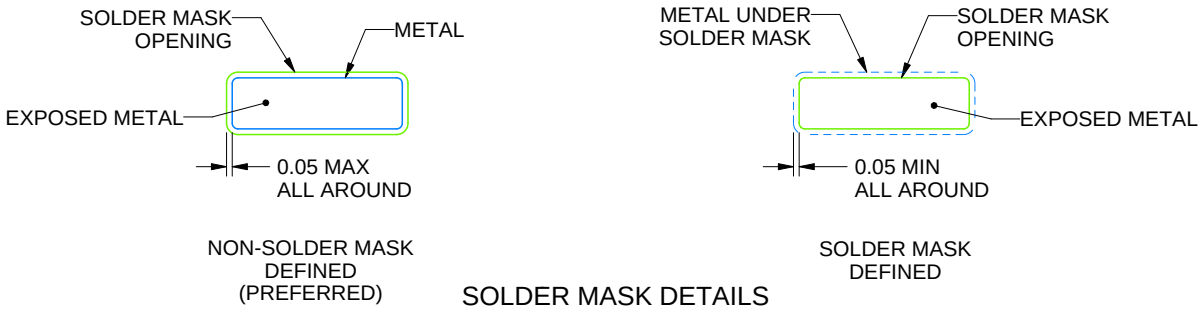


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

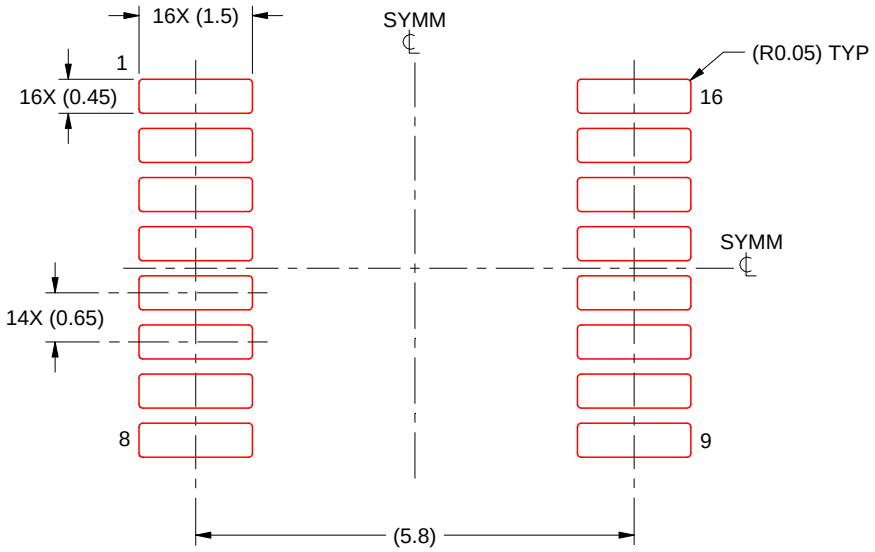


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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