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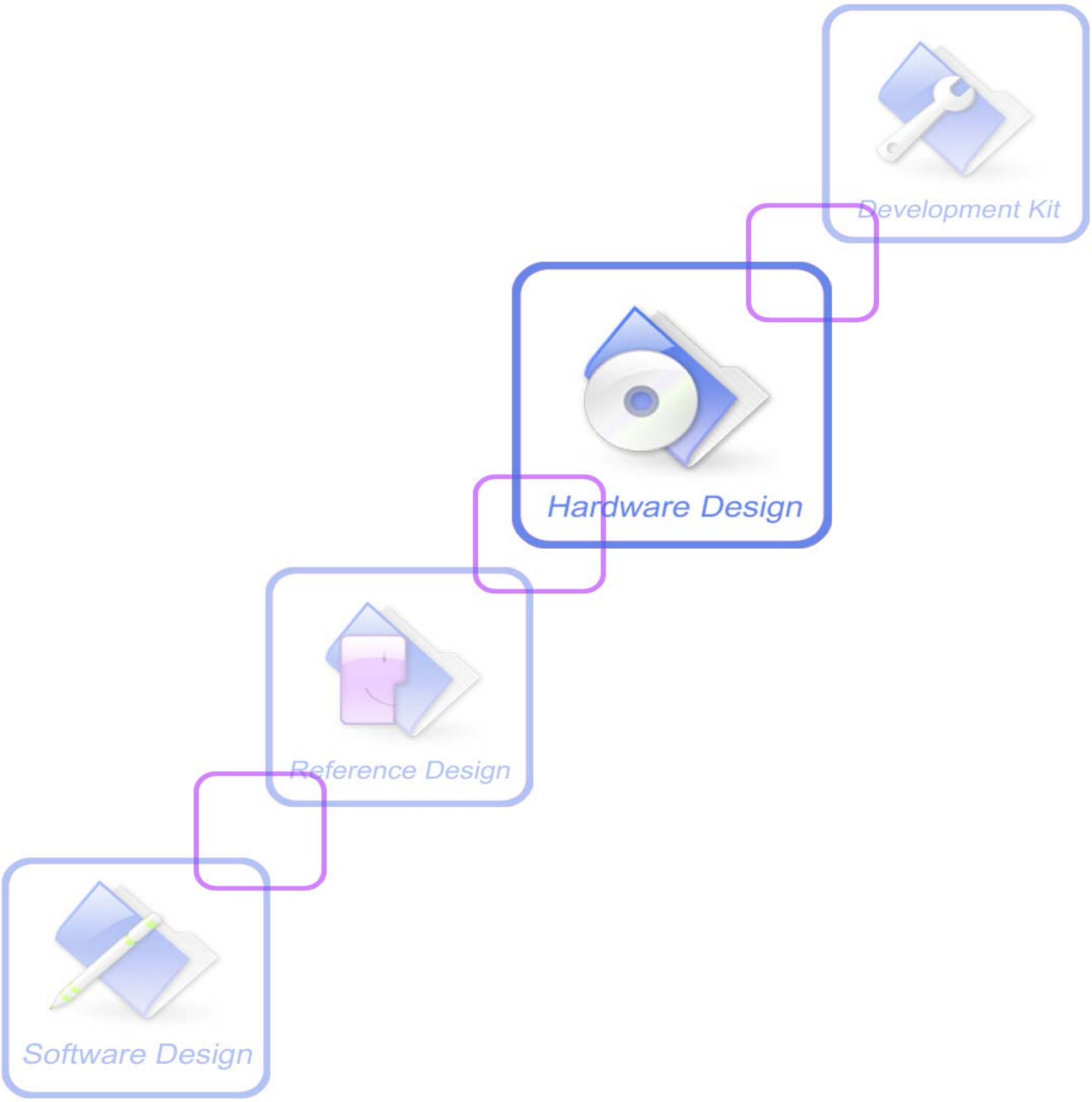
SIM18_Hardware Design_V1.05



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Version History

Date	Version	Description of change	Author
2010-10-07	V1.01	Origin	Huangqiuju
2011-05-31	V1.02	Delete the description of VRTC, add general features, add description of starting SIM18,verify figure3,delete some features that only supported by SIM18A rearrange the structure of document.	Huangqiuju
2011-11-30	V1.03	Modify package mechanical dimensions and PCB Decal	Sunshengwu
2012-06-06	V1.04	Add illustration of SIM18 module information	Sunshengwu
2012-07-25	V1.05	Add recommendation of SIM18 pin	JinXiaohan

1 Introduction

This document describes the hardware interface of the SIMCom module SIM18 which can be used as a stand alone or Aided GPS receiver. As a wide range of applications can be integrated in SIM18, all functional components of SIM18 are described in great detail.

2 SIM18 Overview

SIM18 is a ROM-based stand-alone or Aided GPS receiver. Designed with the new generation of SiRFstarIV™ navigation processor, SIM18 can track as low as -163dBm signal even without network assistance and can cost as low as 36uW @1.8V power consumption in sleep mode. Because of its ROM-based structure, SIM18 requires no host integration and is easy to use and can enable a shorter time to market.

Key Features

With a tiny configuration of 11*11*2.2mm, SIM18 can meet almost all the space requirements in your applications.

The module provides complete signal processing from antenna input to host port in either NMEA messages or in SiRF OSP binary protocol. The module requires 1.8V power supply. The host port is configurable to UART, SPI or I^2C during power up. Host data and I/O signal levels are 1.8V CMOS compatible, inputs are 3.6V tolerable. Both server-generated extended ephemeris (SGEE) and client-generated extended ephemeris (CGEE), version 3.0, are embedded and integrated in the SIM18. Customers who want to use SGEE needs to access servers periodically to download an extended ephemeris (EE) file and transfer it to SIM18. For CGEE customers, there is no need to access server because it will be generated locally. SIM18 can store extended ephemeris data to either serial EEPROM, flash, or host.

2.1 SIM18 Functional Diagram

The following figure shows a functional diagram of the SIM18 and illustrates the mainly functional parts:

- The GPS chip
- LNA
- SAW filter
- The antenna interface
- The communication interface
- The control signals

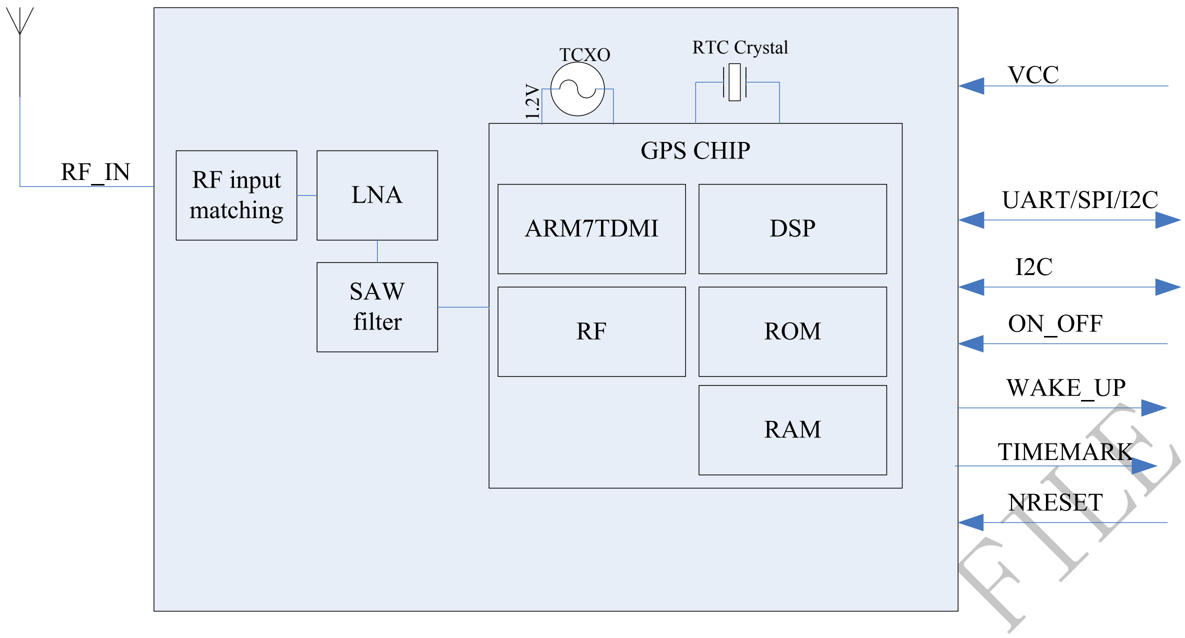

Figure 1: SIM18 functional diagram

2.2 GPS Performance

Table 1: GPS performance

Parameter	Description	Performance			
		Min	Typ	Max	Unit
Horizontal Position Accuracy[1]	Autonomous		<2.5		m
Velocity Accuracy[2]	Speed		<0.01		m/s
	Heading		<0.01		°
Time To First Fix[3]	Hot start		<1		s
	Warm start		<33		s
	Cold start		33	40	s
Sensitivity	Autonomous acquisition(cold start)		-147		dBm
	Re-acquisition		-162		dBm
	Tracking		-163		dBm
Receiver	Channels		48		
	Update rate		1		Hz
	Altitude			<18288	km
	Velocity			<1850	km/h
	Tracking L1, CA Code				
	Protocol support NMEA,OSP				

Power consumption(4)	Continuous tracking		40	65	mA
	Sleep current		20		uA

(1) 50% 24hr static, -130dBm

(2) 50% at 30m/s

(3) GPS signal level: -130dBm

(4) Single Power supply 1.8V

2.3 General features

Table 2: General features

Parameters	**Value**
Supply voltage VCC	+1.71V~1.89V
Supply voltage ripple VCC	54 mV(RMS) max @ f = 0~3MHz 15 mV(RMS) max @ f > 3 MHz
Power consumption(acquisition)	72mW type. @ VCC=1.8 V
Power consumption(sleep)	36uW type. @ VCC=1.8 V
Storage temperature	-40ºC~+85ºC
Operating temperature	-40ºC~+85ºC (note 1)
I/O signal levels	CMOS compatible: Low state 0~ +0.4 V max; High state 0.75~1.0xVCC; Inputs are 3.6 V tolerable.
I/O output sink/source capability	+/- 2 mA max
I/O input leakage	+/- 10 uA max
Host port options	SPI (default), UART or I2C
Serial port protocol (UART)	NMEA (configurable to SiRF binary OSP); 8 bits, no parity, 1 stop bit; 4800 baud (configurable)
TM output (1PPS)	200ms high pulse(+/-1us accuracy)

Note 1: Operation in the temperature range –40°C~ –30°C is allowed but Time-to-First-Fix performance and tracking sensitivity may be degraded.

3 Package Information

3.1 Pin out Diagram

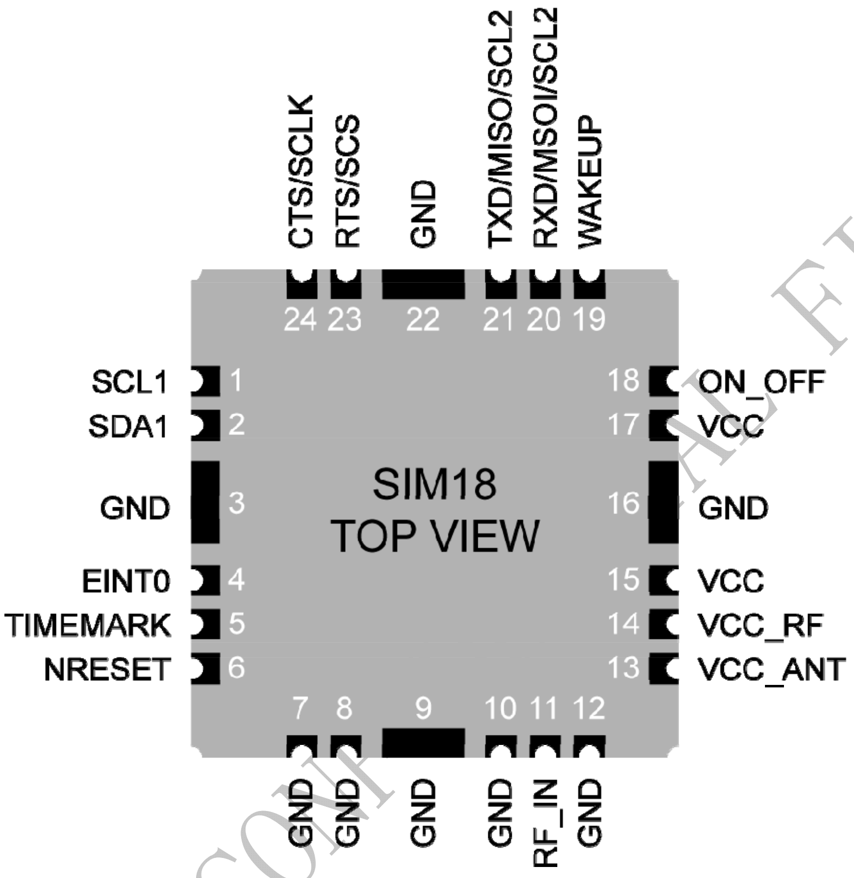

Figure 2: SIM18 pin out diagram (Top view)

3.2 Pin Description

Table 3: Pin description

Pin name	Pin number	I/O	Description	Comment
Power supply				
VCC	15,17	I	Main power input, which will be used to power the baseband and RF section internally.	Provide clean and stable power source to this pin. Add a 4.7uF capacitor to this pin for decouple.
VCC_RF	14	O	1.8V output power supply for active antenna	If it is used, connect to VCC_ANT directly. If unused, keep open.
VCC_ANT	13	I	Power input for active antenna	It depends on user's active antenna's power requirement. If it is unused, keep open.
GND	3,7,8,9,10,12, 16,22		Ground	
Power control				
ON_OFF	18	I	Power control input to control the module going into or wakeup from sleep mode	Must be controlled by host.
WAKEUP	19	O	Indicate the module's state, when it is running, it is high; when in sleep or off state, it is low	If unused, keep open.
nRESET	6	I	External reset input, active low	If unused, keep open.
Host port interface				
TXD/MISO/SCL2	21	O	Function overlay: slave SPI data output(MISO) UART data transmit(TXD) I² C bus clock (SCL2)	The default interface is SPI, user can configure the CTS/CLK and RTS/CS signal to select host port interface type. For details, please refer to chapter3.3.
RXD/MOSI/SDA2	20	I	Function overlay: slave SPI data input(MOSI) UART data receive(RXD) I² C bus data (SDA2)	
CTS/CLK	24	O	slave SPI clock input(CLK) UART clear to send(CTS) active low	
RTS/CS	23	I	slave SPI chip select (CS) active low UART ready to send (RTS) active low	
GPIOs				
SCL1	1	IO	dead reckoning I²C bus data (SCL)	
SDA1	2	IO	dead reckoning I²C	

			bus data (SDA)	
EINT0	4	IO	Provide an interrupt on either high or low logic level or edge-sensitive interrupt	
TIMEMARK	5	IO	Time Mark outputs timing pulse related to receiver time, GPS time or UTC time	
RF interface				
RF_IN	11	I/O	Radio antenna connection	Impendence must be controlled to 50Ω.

3.3 Package Dimensions

Following figure shows the Mechanical dimensions of SIM18 (top view, side view and bottom view).

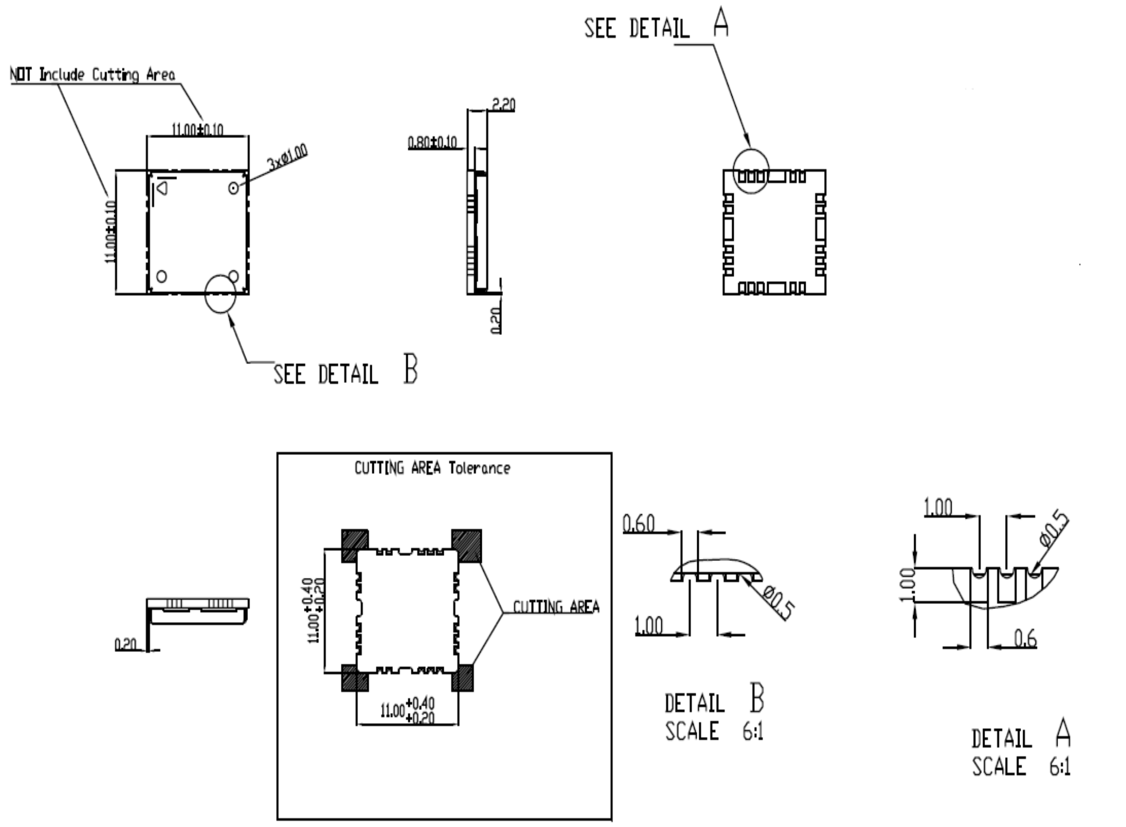

Figure 3: SIM18 mechanical dimensions (Unit: mm)

3.4 SIM18 Recommended PCB Decal

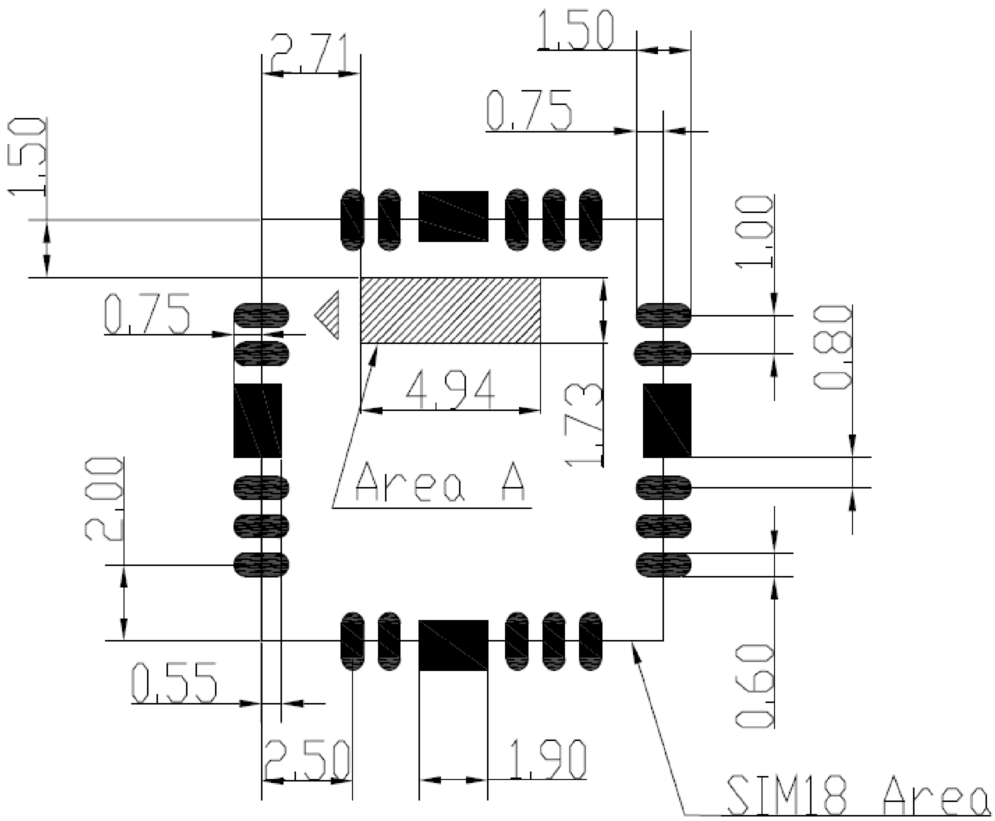

Figure 4: Recommended PCB decal (top view) (Unit: mm)

Note: In the figure, "Area A" is the copper ground on the bottom side of SIM18.Keep copper out of area A, do not place via in area A to avoid short circuit on the mother board.

3.5 SIM18 Recommended PCB Paste

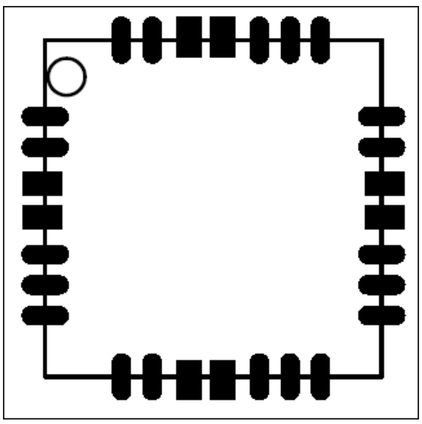

Figure 5: Recommended PCB paste(top view)(Unit: mm)

Note: Because the large pad area of four GNDs, their pastes are divided into 2 parts.

4 Application Interface

The following figure shows a functional diagram of the SIM18 and illustrates the mainly functional parts:

4.1 Power Management

4.1.1 Power Input

SIM18 requires one power supply input: VCC .For fastest possible TTFF, the power supply should be kept active all the time in order to keep the non-volatile RTC & RAM active.

4.1.2 Starting SIM18

For initial power up, the RTC must start oscillating to sequence the Finite State Machine. RTC startup time may vary.

- When power is first applied, SIM18 goes into a low-power mode while RTC starts and FSM sequences though to “ready-to-start” state.
- The host is not required to control nRESET pin since SIM18 internal reset circuitry handles detection of application of power.
- While in “ready-to-start” state, SIM18 awaits a pulse to the ON_OFF input pin to start.
- Since RTC startup time varies, detection of the time when SIM18 is ready to accept an ON_OFF pulse requires the host to either wait for a fixed interval, to monitor a pulse on SIM18 WAKEUP output that indicates FSM “ready-to-start”, or simply to assert a pulse on the ON_OFF input every second until SIM18 starts by indicating a high on WAKEUP or generation of host port messages.

4.1.3 Verification of SIM18 Start

- SIM18 WAKEUP pin will go high to indicate the internal processor is started.
- System activity indication depends upon the chosen serial interface:
  - ✧ UART with no flow control: When it is activated, SIM18 will output messages at the selected UART speed and message types.
  - ✧ UART with flow control: Host flow control must be released to allow SIM18 to send messages.
  - ✧ I^2C multi-master mode with no bus contention: SIM18 will spontaneously send messages at the speed and message types selected.
  - ✧ I^2C multi-master mode with bus contention: SIM18 will send messages after the I^2C bus contention resolution process allows SIM18 to send.
  - ✧ SPI: Since SIM18’s SPI is slave, there is no possible indication of system “ready” through SPI interface. The host must initiate SPI connection approximately one second after WAKEUP goes high.

4.1.4 Droop or Abrupt Removal of Supply Voltage while Operating

When power supplies are intended to be removed, it is suggested that prior power removal a serial message in binary (MID 205 *ref II*) or NMEA format ($PSRF117,16*0B<CR><LF>) is sent to the module to shut down firmware operations orderly. Otherwise e.g. external EEPROM may get corrupted if power down happens in the middle of EEPROM writing, which may increase in TTFF. If external EEPROM is also used for ROM patch code, the abrupt power removal may cause patch code corruption that may end to system failure.

Second option for orderly shutdown is to send ON_OFF interrupt prior removal of power supply. Shutdown operations may take anything between 10 to 900 ms depending upon operation in progress and messages pending and hence is dependent upon serial interface speed and host port type.

If it is likely that the power supply will be removed abruptly, suggestion is to add external voltage monitor to detect under voltage condition below 5% nominal supply voltage and to drive nRESET signal to reset condition (low state). This is important especially when external EEPROM or data storage at host is used. Power supply off-time is suggested to be over 10 seconds to next power up in order to clear all internal backup RAM content and to minimize risk for wrong backup data.

By-pass the VCC supply input by a low ESR ceramic de-coupling capacitor (e.g. 2.2 uF) placed nearby VCC pin to ensure low ripple voltage. Ensure that the supply input ripple voltage is low enough: 54 mV(RMS) max @ f = 0~3MHz and 15 mV(RMS) max @ f > 3 MHz.

4.1.5 Power Saving Modes

SIM18 supports SiRF operating modes for reduced average power consumption (*ref II*) like Adaptive TricklePower™, Advanced Power Management, and Push-to-Fix™ modes:

- **AdaptiveTrickle Power (ATP):** In this mode the receiver stays at Full on power state for 200~900ms and provides a valid fix. Between fixes with 1~10 sec interval the receiver stays in sleep mode. ATP mode is configurable with SiRF binary protocol message ID151 (*ref II*). The receiver stays once in while in Full on power mode automatically (typical every 1800 sec) to receive new ephemeris data from rising satellites or if the received signal levels drop below certain level.

- **Advanced Power Management (APM):** APM allows power savings while ensuring that the quality of the solution is maintained when signal levels drop. APM does not engage until all necessary information is received. Host can configure number of APM cycles (continuous or up to 255), time between fixes (10~180 sec), power duty cycle (5~100%) and max position error. Rest of the time the receiver stays in Sleep mode. This mode is configurable with SiRF binary protocol message ID53 (*ref II*).

- ***Push-to-Fix (PTF)*:** In this mode the receiver is configured to wake up periodically, typically every 1800 sec (configurable range 10~ 7200 sec), for position update and to collect new ephemeris data from rising satellites. Rest of the time the receiver stays in sleep mode. When position update is necessary, the host can wake up the receiver by ON_OFF control input interrupt (pulse low-high-low >90us after which the receiver performs either Snap or Hot start and a valid fix is available within 1~ 8 seconds typically. This mode is configurable with SiRF binary protocol message ID151 & 167 (*ref II*).

Note that position accuracy is somewhat degraded in power management modes when compared to full power operation.

4.1.6 Operating Mode

Table 4: Power supply and clock state according to operation mode

Mode	VCC	Main clock	RTC clock
Full on	on	on	on
Sleep	on	off	on

4.1.6.1 Full on Mode

The module will enter sleep mode after first power up with factory configuration settings. The navigation mode will start after waking up from sleep mode in cold start mode by sending ON_OFF signal interrupt pulse from host. Power consumption will vary depending on the amount of satellite acquisitions and number of satellites in track. This mode is also referenced as Full on, Full Power or Navigation mode.

Navigation is available and any configuration settings are valid as long as the VCC power supply is active. When the power supply is off, settings are reset to factory configuration and receiver performs a cold start on next power up.

The power supply is intended to be kept active all the time and navigation activity is suggested to be controlled to low quiescent sleep mode via ON_OFF control input.

4.1.6.2 Sleep Mode

Sleep mode means a low quiescent (20uA type.) power state where only the internal I/O Keep Alive, non-volatile RTC, patch RAM and backup RAM block is powered on. Other internal blocks like digital baseband and RF are internally powered off. The power supply input VCC shall be kept active all the time, even during sleep mode. Waking up from and entering into sleep mode is controlled by host interrupt at ON_OFF control input (rising edge toggle low-high-low>90us).

During sleep mode the I/O Keep Alive is still active, thus I/O signals keep respective states except TX and RX signals, which are configured to high input impedance state.

During sleep mode, the WAKEUP signal will be kept low. So the host can verify the SIM18's state by reading this pin's voltage level if the power supply is always active.

4.1.7 ON_OFF

An interrupt on the ON_OFF input line can control the SIM18 module going into or waking up from power saving mode.

- If the system is in sleep state, an ON_OFF pulse will move to full-on mode.
- If the system is in TricklePower Mode, on ON_OFF pulse will move it to full-on mode.
- If the system is in Push-To-Fix mode, on ON_OFF pulse will initiate one Push-To-Fix cycle.
- If the system is already in full-on mode, an ON_OFF pulse will move it to sleep mode.

The ON_OFF interrupt is generated by rising edge of a low-high-low pulse, which should be longer than 90us and less than 1s (suggestion is about. 100ms pulse length). Do not generate ON_OFF interrupts to be less than 1 second intervals. Especially take care that any multiple switch bounce pulses are filtered out.

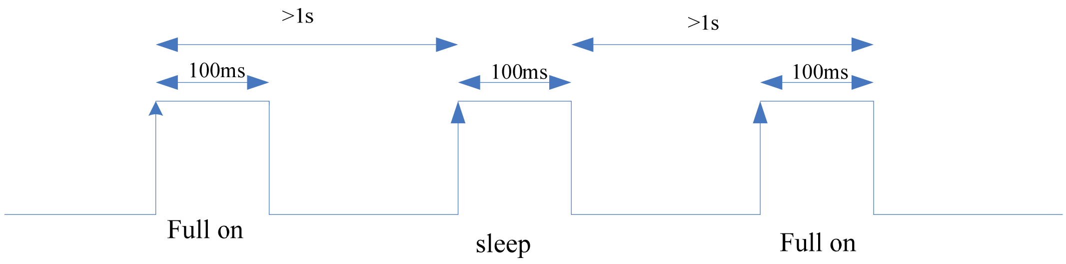

Figure 6: ON_OFF timing

4.1.8 WAKEUP

Wakeup is an output pin which can indicate the SIM18 module's state. When in full-on mode, SIM18 will pull up the WAKEUP pin, while in sleep mode, the WAKEUP pin will be pulled low. So the host can verify the module's state by reading this pin's voltage level.

4.1.9 nRESET

The nRESET pin is an optional, external, emergency reset. It is only for use in the event of a malfunction. When power supply may be abruptly removed, suggestion is to use externally generated reset by means of external voltage monitor or connect this pin to a GPIO of host to control the module.
When nRESET signal is used, it will force volatile RAM data loss (e.g. ROM patch code). Non-Volatile Backup RAM content is not cleared and thus fast TTFF is possible after reset. The input has internal pull up resistor and leave it not connected (floating) if not used.

4.1.10 VCC_ANT, VCC_RF

VCC_RF is a 1.8V output for external active antenna, if the external active antenna works at 1.8V voltage supply domain, the user can tie the VCC_RF and VCC_ANT directly. If the antenna's power is not 1.8V, the pin VCC_ANT is a voltage input pin, it should be provided a proper voltage depending on the active antenna. For passive antennas, both the pin VCC_RF and the pin VCC_ANT should be open.
As shown in the following figure7, it is recommended to add a 10Ω resistor in VCC_ANT pin.

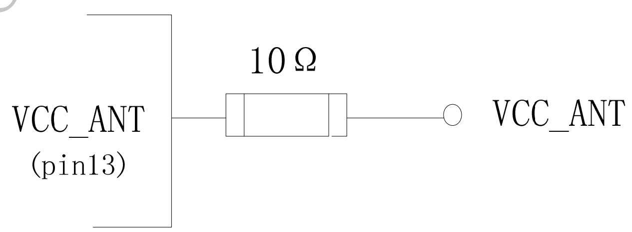

Figure 7: Recommend a resistor in VCC_ANT pin

4.2 Host Interface

User can select the host port configuration between UART, SPI (slave) and I^2C (master/slave) during power up boot.

Table 5 shows these three alternative ports which are multiplexed on a shared set of pins.

Table 5: Host port multiplexed function pins

Pin name	Pin number	Host interface		
		UART	Slave SPI	I^{2}C
TXD/MISO/SCL2	21	data transmit	slave SPI data output (MISO)	I^{2}C bus clock (SCL)
RXD/MOSI/SDA2	20	data receive	slave SPI data output (MOSI)	I^{2}C bus data (SDA)
CTS/CLK	24	clear to send, active low	slave SPI clock input (CLK)	
RTS/CS	23	ready to send, active low	slave SPI chip select (CS#), active low	

At system reset, the host port pins are disabled so no port conflict occurs. User can configure the multiplexed ports by pulling up or pulling down the CTS/CLK and RTS/CS. Table 6 shows the pin strapping information for selecting the host port interface type.

Table 6: Host port type selection

Port type	CTS/CLK	RTS/CS
SPI(default)	0	1
UART	1 (Add a pull-up 10kΩ resistor.)	1
I^{2}C	0	0 (Add a pull-down)

The port selection is not intended to be changed dynamically but only set once at power up.

4.2.1 UART

This UART is used for GPS data report and receiver control. At boot up, the software uses different default baud rates depending on the protocol selected, in OSP mode it is 115200 baud and in NMEA mode it is 4800 baud. The protocol (OSP or NMEA) and/or the communication parameters (Baud rate, data bits, stop bits, and parity) can be configured by NMEA $PSRF100 message, while operation at speeds below 38400 carries risk of dropped messages when using SGEE (Server Generated Extended Ephemeris).

4.2.2 Slave SPI

The host interface SPI is a slave mode SPI:

- Support both SPI and Microwire formats
- An interrupt is provided when the transmit FIFO and output serial register (SR) are both empty
- The transmitter and receiver each have independent 1024B FIFO buffers
  The transmitter and receiver have individual software-defined 2-byte idle patterns of 0xa7 0xb4
- SPI detects synchronization errors and is reset by software
- Supports a maximum clock of 6.8MHz

The slave has no way of forcing data to the master to indicate it is ready for transmission; the master must poll the client periodically. Since the specified idle byte pattern for both receive and transmit is A7 B4, the master can transmit this idle pattern to the slave repeatedly. If the master receives idle patterns back from the slave, it indicates that the slave currently has nothing to transmit but is ready to communicate. Default protocol is NMEA (protocol can be configured by NMEA $PSRF100 message).

On the receiver side, the host is expected to transmit idle pattern A7 B4 when it is querying the module's transmit buffer, unless it has traffic to send to the module. In this way, the volume of discarded bytes is kept nearly as low as in the UART implementation because the hardware does not place most idle pattern bytes in its RX FIFO.

The FIFO thresholds are placed to detect large messages requiring interrupt-driven servicing. On the transmit side, the intent is to fill the FIFO only when it is disabled and empty. In this condition, the SPI driver software loads as many queued messages as it can to completely fit in the FIFO. Then the FIFO is enabled. The host is required to poll messages until idle pattern bytes are detected. At this point the FIFO is empty and disabled, allowing the SPI driver to again respond to an empty FIFO interrupt and load the FIFO with any messages in queue.

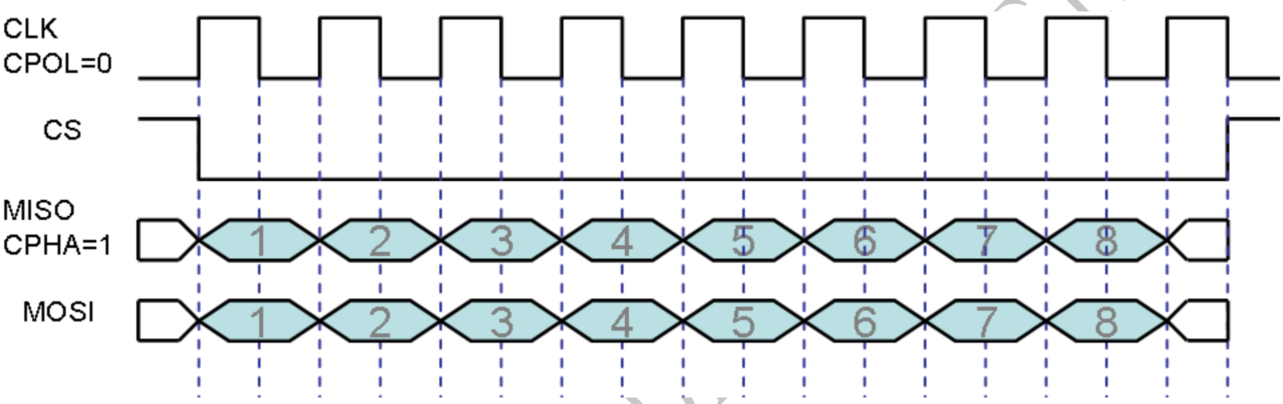

Figure 8: SPI timing (Mode1)

4.2.3 I^{2}C Interface

The I^{2}C host port interface supports:

- Default operating mode is multi-master (configurable to slave, OSP Message ID 178, Sub ID 2)
- Individual transmit and receive FIFO lengths of 64B
- The default I^{2}C address values are(configurable by OSP Message ID 178, Sub ID 2):Rx: 0x60,Tx: 0x62
- Multi-master I^{2}C mode is supported by default.
    - ✧ Transmit side operates as master by seizing the I^{2}C bus when idle is detected
    - ✧ Receive side operates as a slave when another master seizes bus and transmits to this address

The operation of the I^{2}C in multi-master mode with a master transmit and slave receive mimics a UART operation, where both module and host can transmit independently and freely.

Notes: When host port is configured to I^{2}C bus, external pull-up resistors at both signals are required.

4.3 Master mode dead reckoning (DR) I^{2}C Bus

The SCL1 and SDA1 are the DR I^{2}C bus pins, which can be optionally connected to a 1 Mbit EEPROM for Client Generated Extended Ephemeris (CGEE) data storage (see Chapter 4.3.1 and 4.3.2) DR I^{2}C interface supports:

- Typical data lengths (command + in/data out) of several bytes

- Common EEPROM data formats (STMicroelectronics, M24M01, 1 Mbit device)
- Standard I²C bus maximum data rate 400kbps
- Minimum data rate 100kbps

NOTE: the SCL1 and SDA1 pins are both pseudo open-drain and require a 2.2k pull-up resistor on the external bus.

4.3.1 Self-Assistance - Client Generated EE Usage

The SIM18 module supports Client Generated Extended Ephemeris (CGEE), which allows fast TTFF 10 sec typically for 3 days. The CGEE data is generated internally from satellite ephemeris as a background task and thus host should allow the SIM18 to navigate and to collect ephemeris from as many satellites as possible before entering Sleep mode. The CGEE feature requires that power supply is kept active all the time and that an external 1Mbit EEPROM connected to DR I²C bus for CGEE data storage. A command is also required from host to enable EE storage to EEPROM ($PSRF120,F,R*30<CR><LF> or OSP binary message ID 232, Sub ID 253 (*ref II*)). The CGEE data can also be stored optionally to host (contact SIMCom support for availability and details).

4.3.2 Patching ROM Firmware

The firmware that is associated with SIM18 is executed for internal ROM memory. It is a normal practice that firmware patches may be provided from time to time in order to address ROM firmware issues as a method of implementing bug fixes. Patch can be stored on external EEPROM at DR I²C bus or at host.

Patch firmware (max. size 24 kB) and downloading tools are available. The user can contact SIMCom for suggested procedure.

4.4 Timemark Output

The Timemark pin outputs pulse-per-second (1PPS) pulse signal for precise timing purposes. Pulse high level is 200ms about 1us accuracy synchronized at rising edge to full UTC second.

4.5 GPS Antenna

4.5.1 Antenna Interface

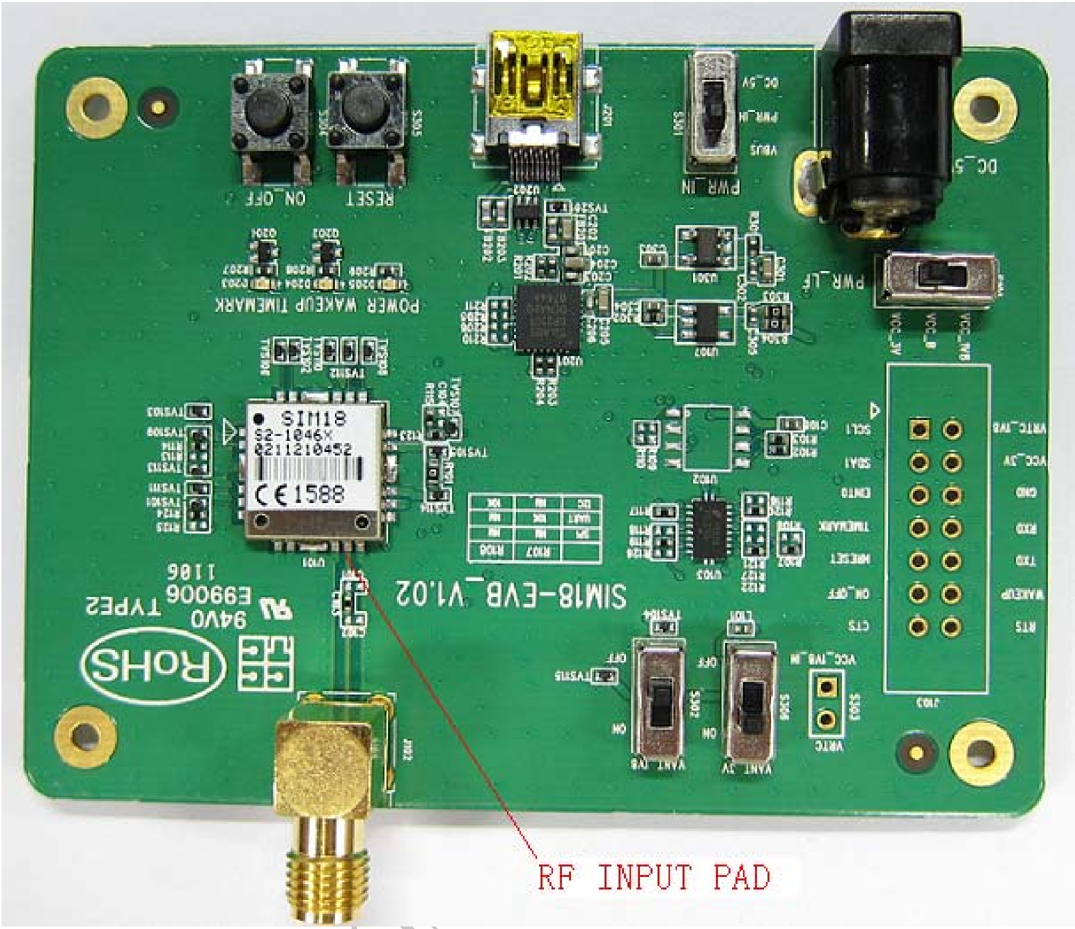

Figure 9: Antenna interface

The RF interface has an impedance of 50Ω. The trace from RF PAD to antenna should also be 50Ω.

To suit the physical design of individual applications the RF interface pad can lead to three alternatives:

- Recommended approach: solderable RF coaxial cable assembly antenna connector, such as HRS' U.FL-R-SMT(10) connector or I-PEX's 20279-001E-01 RF connector.
- SMA connector, such as the example shown in the photo above.
- PCB Antenna.

4.5.2 GPS Antenna Choice Consideration

To obtain excellent GPS reception performance, a good antenna will always be required. The antenna is the most critical item for successful GPS reception in a weak signal environment. Proper choice and placement of the antenna will ensure that satellites at all elevations can be seen, and therefore, accurate fix measurements are obtained.

Most customers contract with antenna design houses to properly measure the radiation pattern of the final mounted configuration in a plastic housing with associated components near the antenna.

4.5.2.1 Passive Antennas

Passive antennas contain only the radiating element, e.g. the ceramic patch, the helix structure, and chip antennas. Sometimes they also contain a passive matching network to match the electrical connection to 50 Ohms impedance.

The most common antenna type for GPS applications is the patch antenna. Patch antennas are flat, generally have a ceramic and metal body and are mounted on a metal base plate. But linear antennas like chip antennas are becoming more popular, and the gain is reasonable, since a smaller ground plane can be used.

User can choose passive antennas following these factors:

- Choose antenna with a reasonably uniform hemispherical gain pattern of >-4dBi.
- Use of an antenna with lower gain than this will give less than desirable results. Please note that a RHCP antenna with a gain of 3dBi, equates to a linear polarized antenna of 0dBi.
- Proper ground plane sizing is a critical consideration for small GPS antennas.
- Proper placement of the GPS antenna should always be the FIRST consideration in integrating the SIM18 GPS Module.

4.5.2.2 Active Antennas

Active antennas have an integrated Low-Noise Amplifier (LNA). Active antennas need a power supply that will c ontribute to GPS system power consumption. Usually, the supply voltage is fed to the antenna through the coaxia l RF cable. Inside the antenna, the DC component on the inner conductor will be separated from the RF signal and routed to the supply pin of the LNA.

It is suggested the active antenna should be chosen as following:

Antenna Chosen	
Frequency range	1575±3MHz
Polarization	RHCP
Gain	>20dB
Noise Figure	NF<1.5
VSWR	<1.5

If the customer's design is for automotive applications, then an active antenna can be used and located on top of the car in order to guarantee the best signal quality.

GPS antenna choice should base on the designing product and other conditions. For detailed Antenna designing consideration, please refer to related antenna vendor's design recommendation. The antenna vendor will offer further technical support and tune their antenna characteristic to achieve successful GPS reception performance depending on the customer's design.

5 Electrical, Reliability and Radio Characteristics

5.1 Absolute Maximum Ratings

The absolute maximum ratings stated in Table 7 are stress ratings under non-operating conditions. Stresses beyond any of these limits will cause permanent damage to SIM18.

Table 7: Absolute maximum ratings

Parameter	Min	Max	Unit
VCC	-	2.2	V
VCC_ANT	-5.5V	+5.5	V
RF pin voltage	-	2.2	V
I/O pin voltage	-	3.6	V
Storage temperature	-	+85	℃

5.2 Recommended Operating Conditions

Table 8: SIM18 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating temperature range		-40	+25	+85	℃
Main supply voltage	VCC	1.71	1.8	1.89	V
Active antenna supply voltage output	VCC_RF	1.71	1.8	1.89	V

Table 9: SIM18 standard IO features

Parameter	Symbol	Min	Typ	Max	Unit
Low level output voltage Test conditions IOL = 2mA and 4.0mA	V_{ol}			0.40	V
High level output voltage Test conditions IOL = 2mA and 4.0mA	V_{oh}	1.35			V
Low level input voltage	V_{il}	-0.4		0.45	V
High level input voltage	V_{ih}	1.26		3.6	V
Input leakage at Vi = 1.8V or 0V	I_i	-10			uA
Tristate output leakage at Vo = 1.8V or 0V	I_{oz}	-10		10	uA
Input capacitance	C_{in}		5		pF
Load capacitance	C_{load}			8	pF

5.3 Electro-Static Discharge

The GPS engine is not protected against Electrostatic Discharge (ESD) in general. Therefore, it is subject to ESD handing precautions that typically apply to ESD sensitive components. Proper ESD handing and packaging procedures must be applied throughout the processing, handing and operation of any application using a SIM18 module.

5.4 Certification

SIM18 meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).and has acquired CE certification.

6 Manufacturing

6.1 Top and Bottom View of SIM18

Figure 10: Top and bottom view of SIM18

Table 10: Illustration of module information

Item	Description
A	Module name
B	Module part number
C	Module serial number
D	CE authenticated code

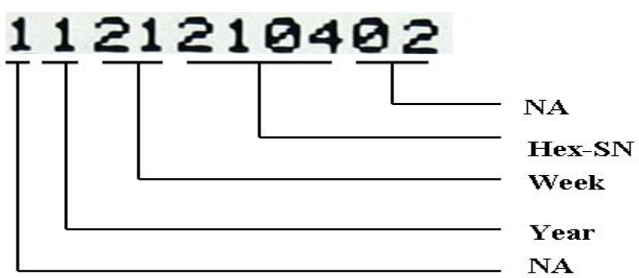

Figure 11: Illustration of module serial number information

6.2 Assembly and Soldering

The SIM18 module is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB. Suggested solder paste stencil height is 150um minimum to ensure sufficient solder volume. If required paste mask pad openings can be increased to ensure proper soldering and solder wetting over pads.
The following figure is the Ramp-Soak-Spike Reflow Profile of SIM18:

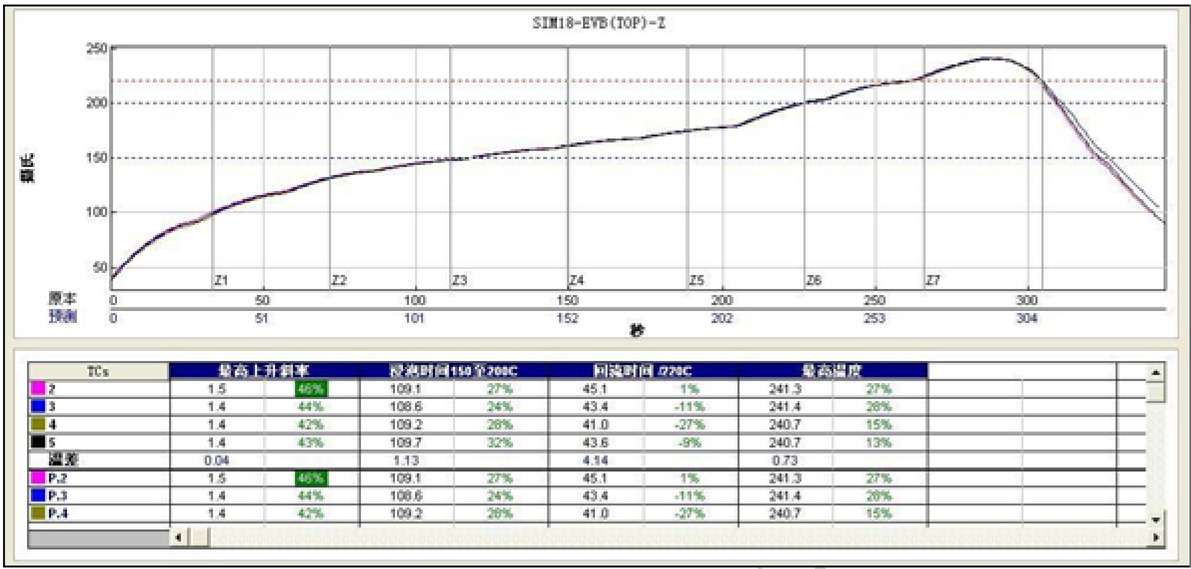

Figure 12: The Ramp-Soak-Spike reflow profile of SIM18

SIM18 is Moisture Sensitive Devices (MSD), appropriate MSD handling instruction and precautions are summarized in Chapter 6.3.

SIM18 modules are also Electrostatic Sensitive Devices (ESD), handling SIM18 modules without proper ESD protection may destroy or damage them permanently.

Avoid ultrasonic exposure due to internal crystal and SAW components.

6.3 Moisture sensitivity

SIM18 module is moisture sensitive at MSL level 3, dry packed according to IPC/JEDEC specification J-STD-020C. The calculated shelf life for dry packed SMD packages is a minimum of 12 months from the bag seal date, when stored in a non condensing atmospheric environment of <40°C/90% RH.

Table 11 lists floor life for different MSL levels in the IPC/JDEC specification:

Table 11:Moisture Classification Level and Floor Life

Level	Floor Life(out of bag)at factory ambient≦30℃/60%RH or as stated
1	Unlimited at ≦30℃/85% RH
2	1 year
2a	4 weeks
3	168 hours

4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, module must be reflowed within the time limit specified on the label.

Factory floor life is 1 week for MSL 3, SIM18 must be processed and soldered within the time. If this time is exceeded, or the humidity indicator card in the sealed package indicates that they have been exposed to moisture, the devices need to be pre-baked before the reflow solder process.

Both encapsulate and substrate materials absorb moisture. IPC/JEDEC specification J-STD-020 must be observed to prevent cracking and delamination associated with the "popcorn" effect during reflow soldering. The popcorn effect can be described as miniature explosions of evaporating moisture. Baking before processing is required in the following cases:

- Humidity indicator card: At least one circular indicator is no longer blue
- Floor life or environmental requirements after opening the seal have been exceeded, e.g. exposure to excessive seasonal humidity.

Refer to Section 4 of IPC/JEDEC J-STD-033 for recommended baking procedures.

Notes: Oxidation Risk: Baking SMD packages may cause oxidation and/or inter metallic growth of the terminations, which if excessive can result in solder ability problems during board assembly. The temperature and time for baking SMD packages are therefore limited by solder ability considerations. The cumulative bake time at a temperature greater than 90°C and up to 125°C shall not exceed 96 hours.

6.4 ESD handling precautions

SIM18 modules are Electrostatic Sensitive Devices (ESD). Observe precautions for handling!
Failure to observe these precautions can result in severe damage to the GPS receiver!

GPS receivers are Electrostatic Sensitive Devices (ESD) and require special precautions when handling. Particular care must be exercised when handling patch antennas, due to the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the receiver:

Unless there is a galvanic coupling between the local GND (i.e. the work Table) and the PCB GND, then the first point of contact when handling the PCB shall always be between the local GND and PCB GND.
Before mounting an antenna patch, connect ground of the device

When handling the RF pin, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna ~10pF, coax cable ~50-80pF/m, soldering iron, …)
To prevent electrostatic discharge through the RF input, do not touch the mounted patch antenna.
When soldering RF connectors and patch antennas to the receiver's RF pin, make sure to use an ESD safe soldering iron (tip).

6.5 Shipment

SIM18 is designed and packaged to be processed in an automatic assembly line, and it is now packaged in SIM18 tray.

7 Reference Design

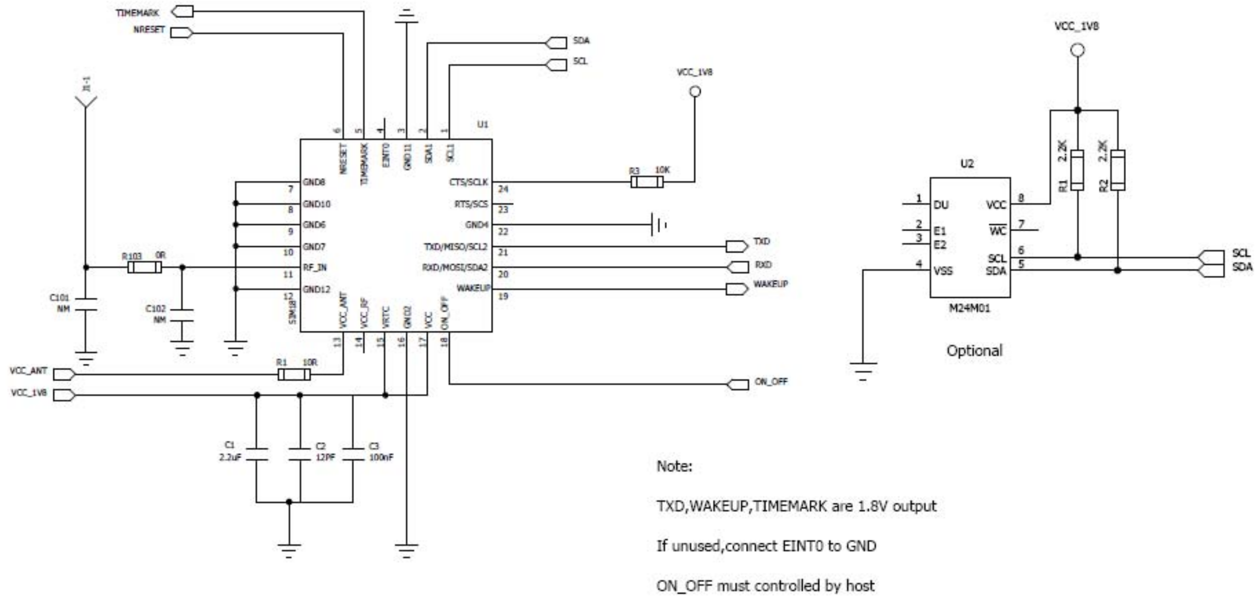

Figure 13: Example application schematic with UART

Notes:

1) ***The pin VCC_RF provides a 1.8V output level for external active antenna.***
   For active antenna, if antenna's power domain is 1.8V, the pin VCC_RF could connect to the pin VCC_ANT directly. If the antenna's power is not 1.8v, keep the pin VCC_RF open and supply the pin VCC_ANT proper voltage depending on the active antenna.
   For passive antenna, the pin VCC_RF and the pin VCC_ANT should be kept open.
2) ***All I/O signal levels are CMOS 1.8V compatible and inputs are 3.6V tolerable. For when SIM18 working in 3V domain, level shift components are needed for output pins.***
3) ***It is recommended to add a 10 Ω resistor(R1 in Figure13) in VCC_ANT pin.***
4) ***The maximum input ripple of VCC is as follows:***

Table 12: Maximum allowable ripple

Rail	Frequency range	Allowable ripple
VCC	0~3MHZ	54mV
	>3MHZ	15mV

Appendix

A. Related Documents

Table 13: Related documents

SN	Document name	Remark
[1]	CS-130679-DS-3	GSD4e datasheet
[2]	CS-129291-DC-2	One Socket Protocol Interface Control Document
[3]	CS-129291-DC-8	GSD4e OSP Manual
[4]	CS-129435-MA	NMEA Reference Manual

B. Terms and Abbreviations

Table 14:Terms and abbreviations

Abbreviation	Description
CGEE	Client Generated Extended Ephemeris
CMOS	Complementary Metal Oxide Semiconductor
EEPROM	Electrically Erasable Programmable Read Only Memory
ESD	Electrostatic Sensitive Devices
FSM	Finite State Machine
GPS	Global Positioning System
I/O	Input/Output
IC	Integrated Circuit
Inorm	Normal Current
Imax	Maximum Load Current
kbps	Kilo bits per second
KA	Keep alive
MSL	moisture sensitive level
NEMA	National Marine Electronics Association
SGEE	server-generated extended ephemeris

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