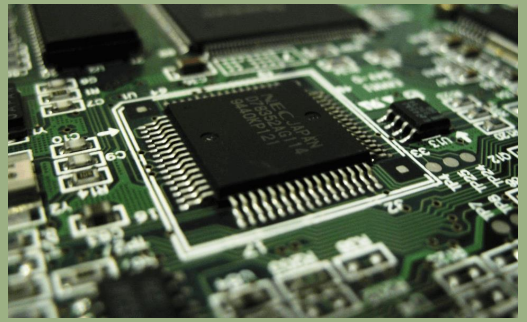


8085 Microprocessor

Dr. Manju Khurana
Assistant Professor, CSED
TIET, Patiala
manju.khurana@thapar.edu

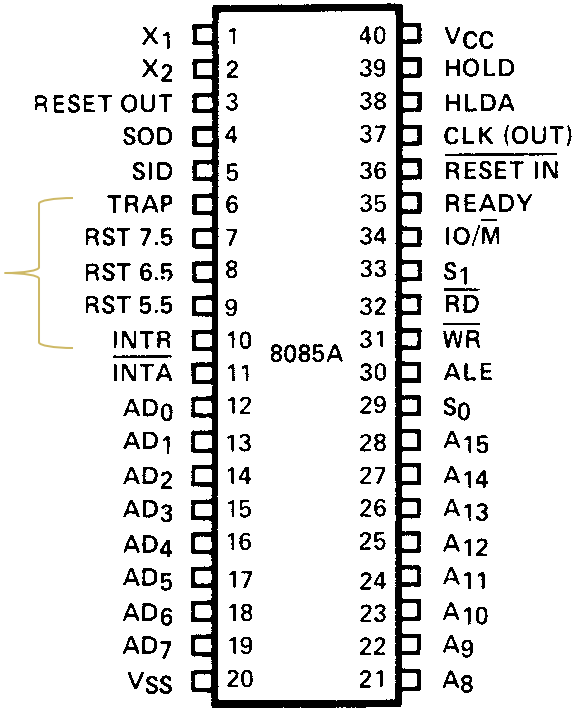
Interrupts

- Interrupt is a mechanism by which an I/O or an instruction can suspend the normal execution of processor and get itself serviced. Generally, a particular task is assigned to that interrupt signal. In the microprocessor based system the interrupts are used for data transfer between the peripheral devices and the microprocessor.
- After receiving an interrupt signal from the peripheral, the microprocessor executes current instruction completely.
- Store the contents of program counter i.e. return address on the stack and then executes interrupts service (ISR) to provide service to the interrupting device.
- After servicing the device, the microprocessor transfer program control back to the program where interrupt occurs by reloading the content of program counter which has been stored on the stack when an interrupt occurs.

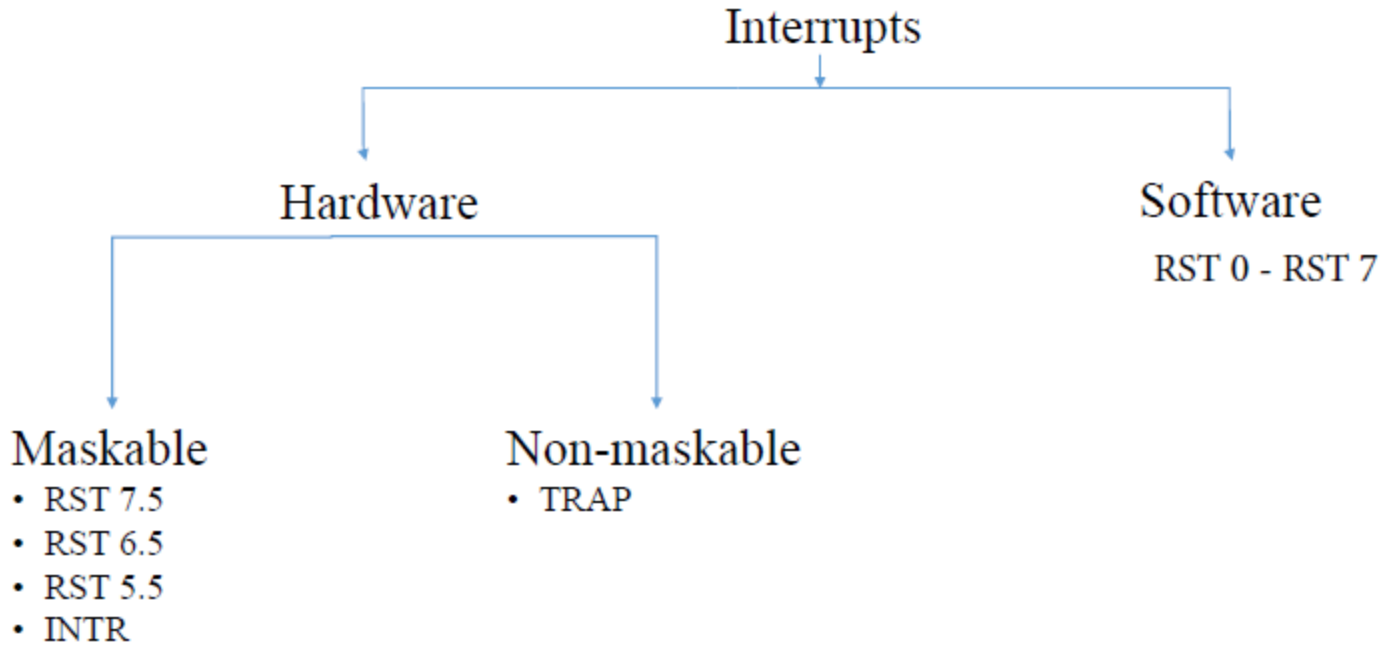
Interrupt pins on IC

There are 5 interrupt inputs:

- TRAP (non-maskable)
- RST7.5
- RST6.5
- RST5.5
- INTR



Classification of Interrupts



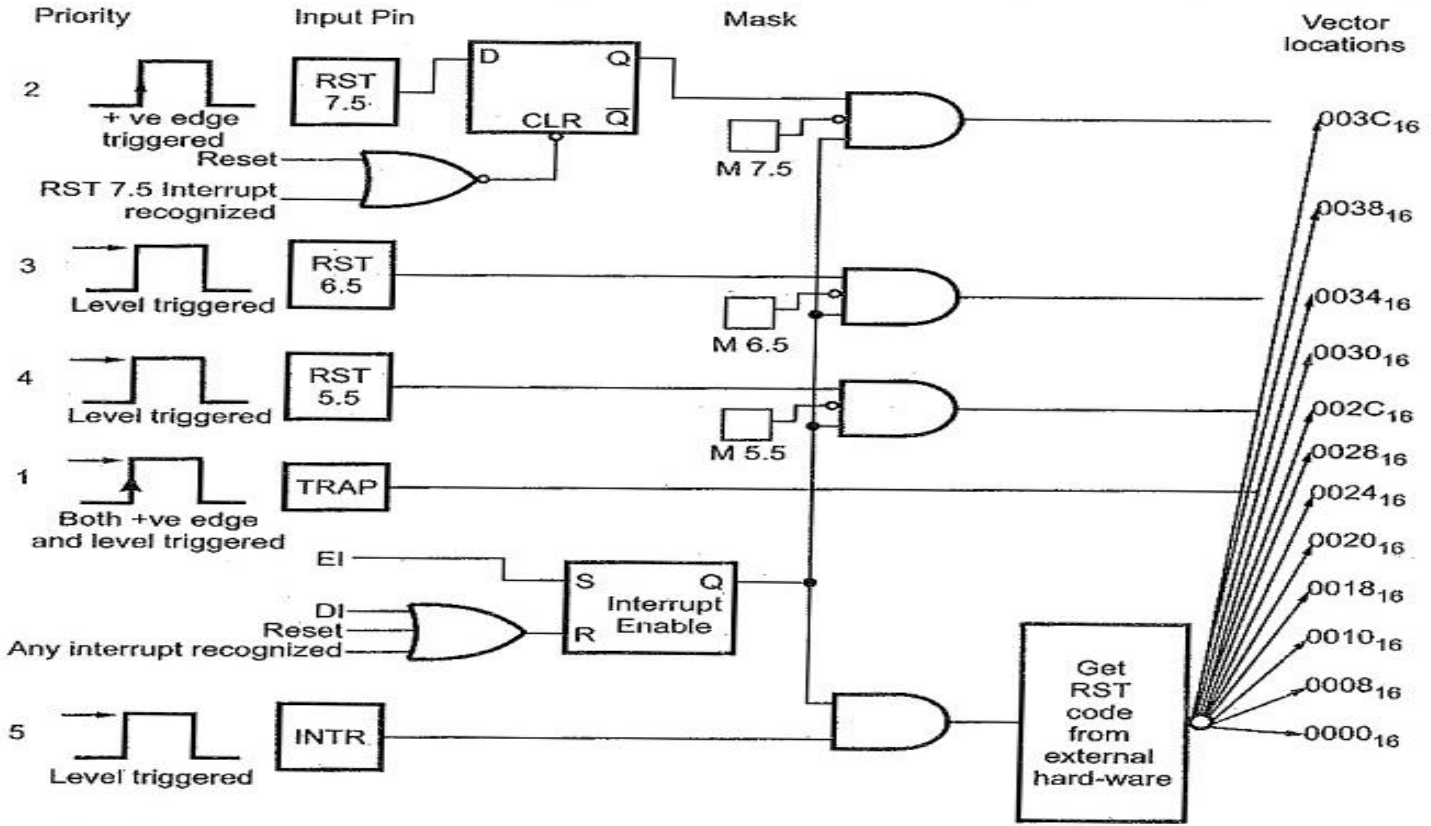
Hardware Interrupts

Interrupt type	Trigger	Priority	Maskable	Vector address
TRAP	Edge and Level	1st	No	0024H
RST 7.5	Edge	2nd	Yes	003CH
RST 6.5	Level	3rd	Yes	0034H
RST 5.5	Level	4th	Yes	002CH
INTR	Level	5th	Yes	-

Software Interrupts

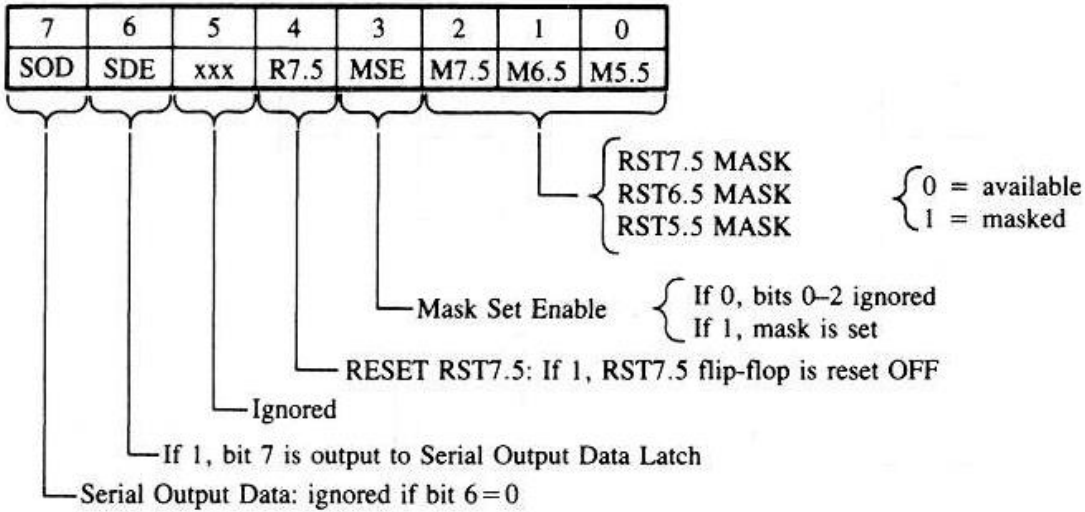
Instruction	Corresponding HEX code	Vector addresses
RST 0	C7	0000H
RST 1	CF	0008H
RST 2	D7	0010H
RST 3	DF	0018H
RST 4	E7	0020H
RST 5	EF	0028H
RST 6	F7	0030H
RST 7	FF	0038H

Schematic Diagram of 8085 Interrupts



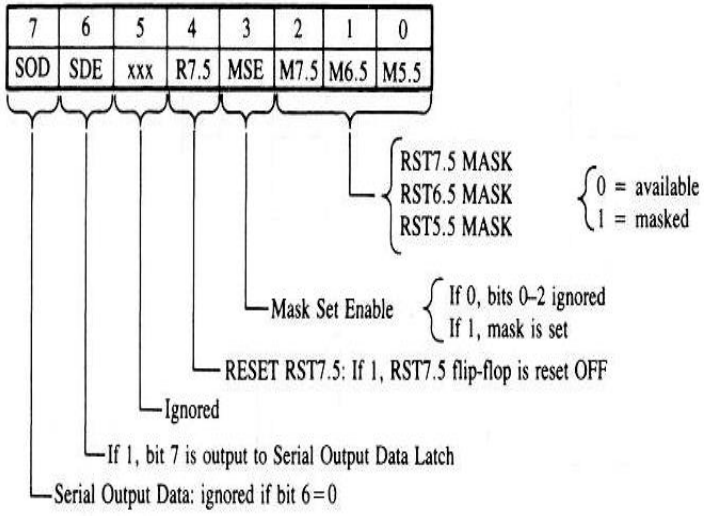
SIM (Set Interrupt Mask) Instruction

- This is a multipurpose instruction and used to implement The 8085 interrupts 7.5, 6.5, 5.5, and serial data output. The instruction interrupts the accumulator contents as following:



1. Example: Enable all the interrupts of Intel 8085. First, determine the contents of the accumulator

- Enable 5.5 bit 0 = 0
- Enable 6.5 bit 1 = 0
- Enable 7.5 bit 2 = 0
- Allow setting the masks bit 3 = 1
- Don't reset the flip flop bit 4 = 0
- Bit 5 is not used bit 5 = 0
- Don't use serial data bit 6 = 0
- Serial data is ignored bit 7 = 0



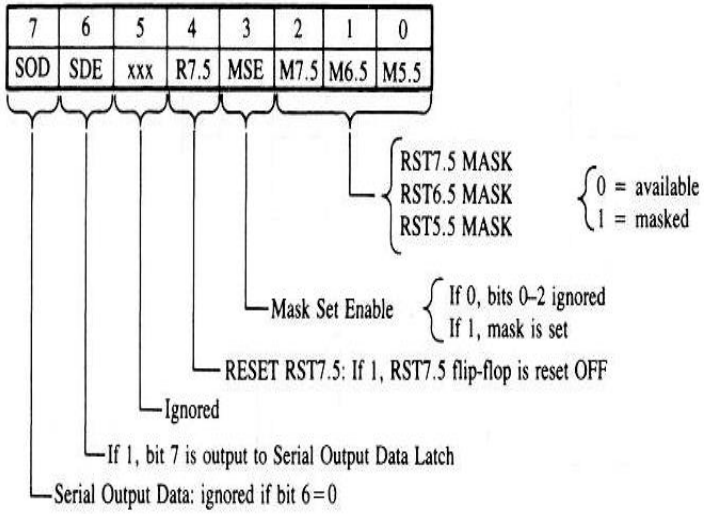

```
EI                  ; Enable interrupts including INTR
MVI A, 08   ; Prepare the mask to enable RST 5.5, 6.5 and 7.5.
SIM                 ; Apply the settings RST masks
```

0	0	0	0	1	0	0	0

Contents of accumulator are: 08 H

2. Example: Set the interrupt masks so that RST6.5 is enabled and disable RST7.5 and RST5.5. First, determine the contents of the accumulator

- Disable 5.5 bit 0 = 1
- Enable 6.5 bit 1 = 0
- Disable 7.5 bit 2 = 1
- Allow setting the masks bit 3 = 1
- reset the flip flop bit 4 = 1
- Bit 5 is not used bit 5 = 0
- Don't use serial data bit 6 = 0
- Serial data is ignored bit 7 = 0



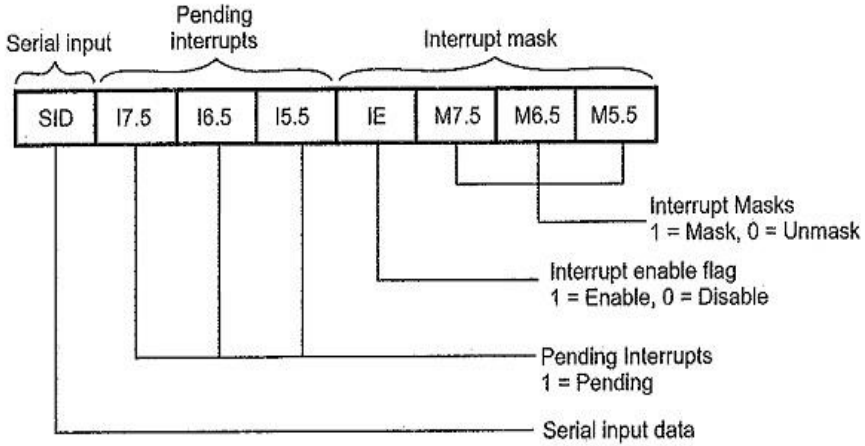

```
EI                  ; Enable interrupts including INTR
MVI A, 1D           ; Prepare the mask to enable RST 6.5, disable 6.5 and 5.5.
SIM                 ; Apply the settings RST masks
```

0	0	0	1	1	1	0	1

Contents of accumulator are: 1D H

RIM (Read Interrupt Mask) Instruction

- The Read Interrupt Mask, RIM, instruction loads the status of the interrupt mask, the pending interrupts and the contents of the serial input data line, SID, into the accumulator. Thus, it is possible to monitor status of interrupt mask, pending interrupts and serial input. There are number of Types of Interrupts in 8085. When one interrupt is being serviced, other interrupt requests may occur. If the interrupt requests are of higher priority, 8085 branches program control to the requested interrupt service routines. But when the interrupt requests are of lower priority, 8085 stores the information about these interrupt requests. Such interrupts are called pending interrupts. The status of pending interrupts can be monitored using RIM instruction.




Thank you!