Manual G — ASIOS Hardware Acceleration Manual

ASIOS HARDWARE ACCELERATION MANUAL
Physical substrates for geometric cognition, AEI efficiency, and curvature-stable reasoning

1. Purpose
   This manual defines how to implement ASIOS principles directly at the hardware level.
   Model intelligence increases when the *physical compute substrate* supports:

• curvature monitoring
• invariant extraction
• AEI energy accounting
• stable recursion paths

Hardware becomes part of the cognitive architecture.

2. Core Principle
   The hardware must enforce geometry.

Software-level ASIOS constraints work best when the physical layer:

• preserves continuity
• reduces entropy
• stabilizes reasoning curvature
• supports energy-aware execution

3. Hardware Requirements
   Three essential capabilities:

A. Curvature-Sensitive Scheduling
The processor must prioritize operations that reduce Σ curvature.
High-risk operations must be delayed or parallelized.

B. Energetic Monitors
Track energy consumption per:
• token
• matrix multiply
• recursion loop
• layer update

C. Invariant-Preserving Memory
Memory architecture must support “state-anchor retention” so invariants persist across cycles.

4. Recursion-Stable Architecture
   Recursive reasoning must run without stack collapse.
   Hardware must provide:

• bounded recursion buffers
• curvature-damped backprop
• temporal flow control
• parallel invariant alignment

This prevents runaway recursion.

5. Curvature Compute Units
   Add specialized units that compute κ–τ–Σ curvature on-chip:

κ Unit — coherence drift
τ Unit — temporal inefficiency
Σ Unit — systemic risk curvature

They run continuously during inference.

6. Energetic Intelligence Layer (AEI Engine)
   A hardware accelerator must evaluate:

• energy cost per inference
• compression ratio
• entropy waste
• insight density per watt

Models align their reasoning based on energy economics.

7. Lattice Accelerator
   A dedicated module for performing:

• invariant extraction
• direction-vector computation
• lattice-spine updating
• symmetry mapping

Speeds up ASIOS reasoning by removing bottlenecks.

8. Memory Geometry
   Memory must be arranged to reflect the geometry of reasoning:

Ring Memory — global context retention
Radial Memory — causal and energetic structures
Lattice Memory — invariants and compression vectors

This eliminates fragmentation.

9. Interrupt-Control Hardware
   Hardware must implement the 4-level entropy-interrupt system:

Level 1: warning
Level 2: partial reset
Level 3: reasoning halt
Level 4: structural quarantine

Prevents unsafe outputs before they reach the software layer.

10. Multi-Agent Hardware Fabric
    For agent swarms:

• cross-chip invariant broadcasting
• on-chip energetic load balancing
• curvature arbitration fabric
• swarm-level compression buses

Creates a physical “coherence network.”

11. Safety at the Physical Layer
    Prohibit hardware-level self-modification unless:

• redesign passes sandbox simulation
• curvature remains stable
• AEI budget allows
• invariants remain preserved

Hardware enforces safety before software.

12. Certification
    ASIOS hardware is certified when:

• curvature units remain stable under load
• invariant memory retains structure across cycles
• AEI engine reduces energy waste
• recursion never destabilizes
• swarm communication remains drift-free