Nanya Quality Monthly Report

Apr./2024

☐ Report Date ：2024/04/30

Agenda

- *CLCR performance……3-4*
- *OOC performance……..5*
- *Wafer manufacture process Cpk performance……6*
- *KEP electrical Parameter Cpk performance……..……7*
- *Component assembly process Cpk performance……8*
- *ORT monitor Summary……..9*

➢ *20nm 8Gb DDR4 UCLCR performance*

Remark	23'Oct	23'Nov	23'Dec	24'Jan	24'Feb	24' Mar
STI final CD	-0.26	-0.28	-0.15	-0.22	-0.20	-0.08
RAD final CD	-0.30	-0.33	-0.14	-0.10	-0.12	-0.20
Thick Gate Oxide Thickness	-0.14	-0.17	-0.22	-0.16	-0.17	-0.15
Thin Gate Oxide Thickness	-0.53	-0.48	-0.53	-0.50	-0.46	-0.48
Buried digital line CD	0.11	0.09	0.19	0.09	0.10	0.05
Periphery PMOS gate CD	-0.06	-0.09	-0.20	-0.29	-0.28	-0.22
Cell Contact CD	-0.19	-0.28	-0.34	-0.25	-0.18	-0.21
Container Bot CD	0.29	0.30	0.33	0.28	0.26	0.20
Metal 1 contact CD to buried digital line	0.33	0.32	0.41	0.38	0.31	0.30
Metal 1 CD	-0.01	0.03	-0.09	-0.15	-0.05	0.06
Via1 (M2 to M1 contact)	-0.47	-0.67	-0.53	-0.51	-0.61	-0.72
Metal 2 CD	-0.66	-0.59	-0.54	-0.67	-0.50	-0.62
Via2 (M3 to M2 contact)	-0.09	0.03	0.13	0.01	0.13	0.22
Metal 3 CD	-0.34	-0.42	-0.45	-0.59	-0.65	-0.46

➢ *20nm 8Gb DDR4 LCLCR performance*

Remark	23' Oct	23'Nov	23'Dec	24'Jan	24'Feb	24'Mar
STI final CD	-0.26	-0.28	-0.15	-0.22	-0.20	-0.08
RAD final CD	-0.30	-0.33	-0.14	-0.10	-0.12	-0.20
Thick Gate Oxide Thickness	-0.14	-0.17	-0.22	-0.16	-0.17	-0.15
Thin Gate Oxide Thickness	-0.53	-0.48	-0.53	-0.50	-0.46	-0.48
Buried digital line CD	0.11	0.09	0.19	0.09	0.10	0.05
Periphery PMOS gate CD	-0.06	-0.09	-0.20	-0.29	-0.28	-0.22
Cell Contact CD	-0.19	-0.28	-0.34	-0.25	-0.18	-0.21
Container Bot CD	0.29	0.30	0.33	0.28	0.26	0.20
Metal 1 contact CD to buried digital line	0.33	0.32	0.41	0.38	0.31	0.30
Metal 1 CD	-0.01	0.03	-0.09	-0.15	-0.05	0.06
Via1 (M2 to M1 contact)	-0.47	-0.67	-0.53	-0.51	-0.61	-0.72
Metal 2 CD	-0.66	-0.59	-0.54	-0.67	-0.50	-0.62
Via2 (M3 to M2 contact)	-0.09	0.03	0.13	0.01	0.13	0.22
Metal 3 CD	-0.34	-0.42	-0.45	-0.59	-0.65	-0.46

➢ *20nm 8Gb DDR4 OOC performance*

Remark	23' Oct	23'Nov	23'Dec	24'Jan	24'Feb	24'Mar
STI final CD	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
RAD final CD	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
Thick Gate Oxide Thickness	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
Thin Gate Oxide Thickness	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
Buried digital line CD	0.26%	0.21%	0.39%	0.25%	0.28%	0.23%
Periphery PMOS gate CD	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
Cell Contact CD	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
Container Bot CD	0.39%	0.41%	0.60%	0.43%	0.26%	0.21%
Metal 1 contact CD to buried digital line	0.28%	0.25%	0.29%	0.23%	0.20%	0.18%
Metal 1 CD	0.00%	0.29%	0.00%	0.00%	0.00%	0.34%
Via1 (M2 to M1 contact)	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
Metal 2 CD	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
Via2 (M3 to M2 contact)	0.00%	0.35%	0.51%	0.29%	0.41%	0.50%
Metal 3 CD	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%

➢ *20nm 8Gb DDR4 Cpk performance(wafer manufacture process)*

Remark	23' Oct	23'Nov	23'Dec	24'Jan	24'Feb	24'Mar
STI final CD	2.50	2.55	2.47	2.50	2.45	2.37
RAD final CD	2.55	2.58	2.50	2.42	2.49	2.56
Thick Gate Oxide Thickness	3.89	3.92	3.99	3.92	3.98	3.92
Thin Gate Oxide Thickness	3.90	3.86	3.92	3.88	3.84	3.86
Buried digital line CD	2.32	2.34	2.30	2.37	2.35	2.40
Periphery PMOS gate CD	2.17	2.20	2.27	2.33	2.32	2.28
Cell Contact CD	3.73	3.82	3.90	3.82	3.70	3.74
Container Bot CD	2.68	2.65	2.61	2.69	2.74	2.76
Metal 1 contact CD to buried digital line	2.40	2.45	2.37	2.40	2.42	2.45
Metal 1 CD	3.16	3.10	3.23	3.28	3.19	3.09
Via1 (M2 to M1 contact)	2.42	2.51	2.46	2.45	2.52	2.60
Metal 2 CD	2.20	2.18	2.14	2.20	2.14	2.19
Via2 (M3 to M2 contact)	3.16	3.07	2.97	3.02	2.96	2.87
Metal 3 CD	2.90	2.99	3.05	3.11	3.14	3.08

➢ *20nm 8Gb DDR4 Cpk performance(KEP electrical Parameter)*

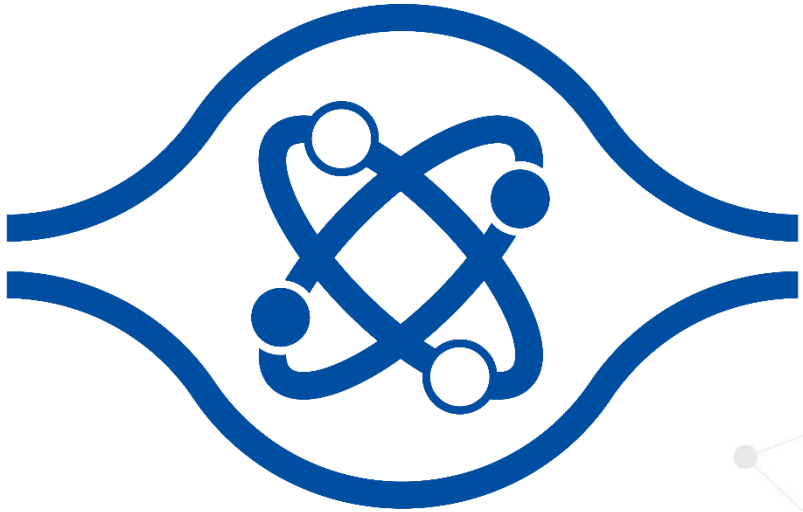
Remark	23' Oct	23'Nov	23'Dec	24'Jan	24'Feb	24'Mar
Thin gate oxide breakdown voltage	6.01	6.10	5.95	5.98	5.77	5.82
Thick gate oxide breakdown voltage	19.89	19.61	19.89	19.44	19.52	19.91
Metal3 to metal2 contact resistance	9.26	8.74	8.83	8.84	8.49	8.27
Metal2 to metal1 contact resistance	9.14	9.15	8.77	8.54	8.66	8.41
Container capacitance	7.02	7.20	7.86	7.89	7.35	7.43
Array device Idsat	6.37	6.63	7.06	6.86	6.42	6.51
Thin gate oxide NFET Idsat	5.20	5.48	5.34	5.53	5.28	5.06
Thin gate oxide PFET Idsat	5.60	5.36	5.43	5.30	5.58	5.44
Metal1 to metal0 contact	5.72	6.21	5.88	5.36	5.93	5.58
Metal1 serpentine Rs	5.56	5.18	5.27	5.33	5.46	5.60

➢ *20nm 8Gb DDR4 Cpk performance(Component assembly process)*

Sample size (per lot)	Remark	23'Oct	23'Nov	23'Dec	24'Jan	24'Feb	24'Mar
10 wires	Wire Bonding: Gold Wire Pull	3.65	3.79	3.64	3.78	3.62	3.80
10 wires	Wire Bonding: Gold Ball Shear	3.43	3.55	3.42	3.41	3.47	3.48
18 balls	Solder Ball Mounting: Solder Ball Shear	3.87	3.64	3.78	3.51	3.57	3.86

➢ *20nm 8Gb DDR4 reliability monitor results*

Test Items	Frequency	Condition	Sample size	Target	Jan./'24	Feb./'24	Mar./'24
ELFR	Monthly	1.2x ~1.3x Vinternal Ta=125°C, 36 hrs	>=6,000ea / 3 lots	100 ppm @1year	0ppm/year (0/11277)	0ppm/year (0/10200)	0ppm/year (0/10965)
				dpm w/ 60%C.L.	81dpm	90dpm	84dpm
HTOL	Quarterly	1.3x Vinternal Ta=125°C, 500 hrs Continue to 1,000hrs for next quarter	>=500ea/ 3 lots	10 FIT @60% C.L.	0 fail		
Package Integrity	Quarterly	JSTD-020 Level 3	66ea/ 2 lots	0 fail	0 fail		
PC+ TC	Quarterly	-55°C / +125°C, 2 cycles/hr, 1,000 cycles	231ea/ 3 lots	0 fail	0 fail		
PC+ HAST	Quarterly	130°C,85% RH, 96 hrs, Vmax	231ea/ 3 lots	0 fail	0 fail		
PC+ HTS	Quarterly	150°C, 1,000 hrs	231ea/ 3 lots	0 fail	0 fail		



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