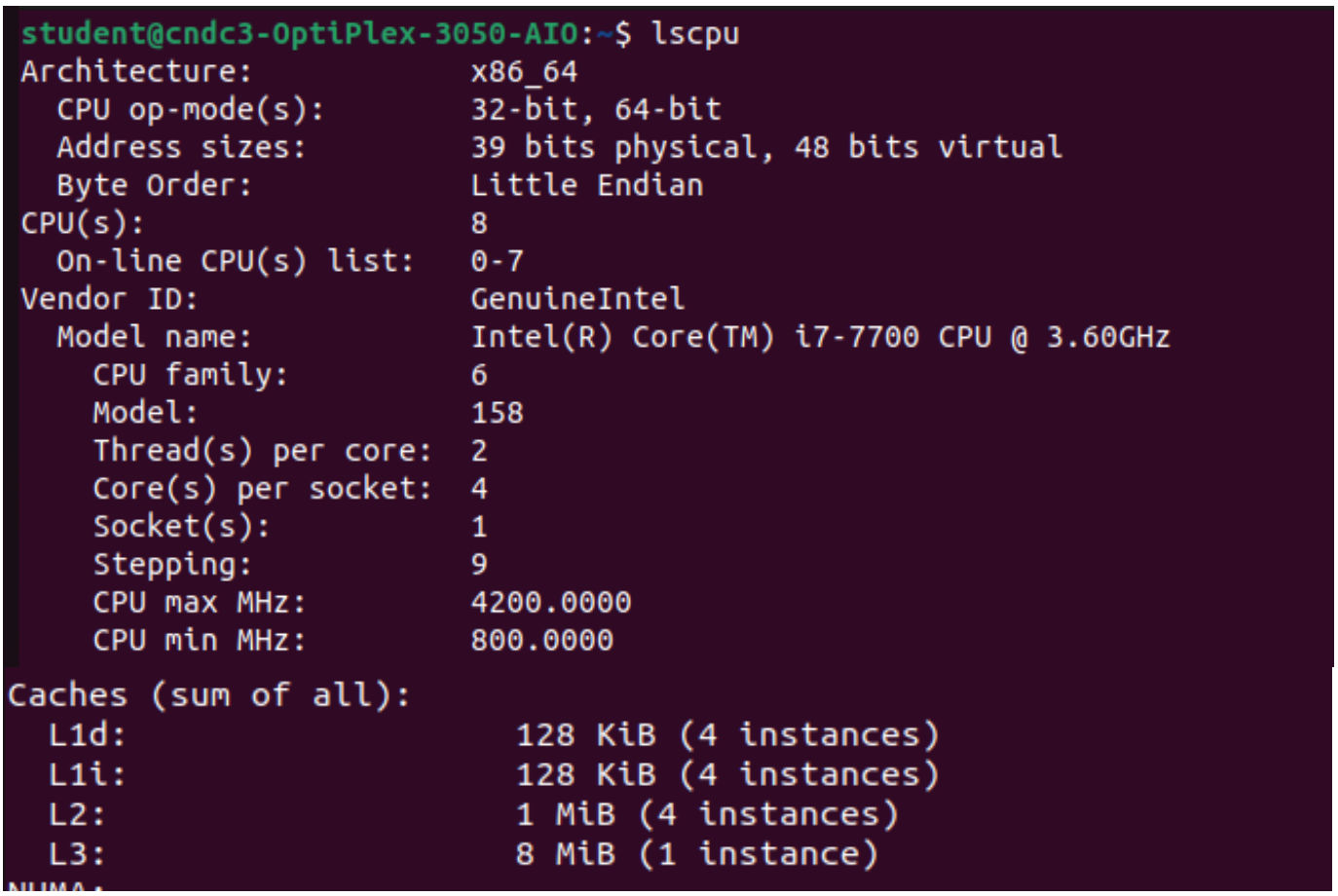

1) Instruction set architecture (ISA) : Instruction set architecture (ISA) is a bridge between the software and hardware of a computer.
Instruction set architecture dictates that the computer must assist:

- Arithmetic/logic instructions
- Data transfer instructions
- Branch and jump instructions

Little Endian byte ordering is defined as follows:

In a binary number consisting of multiple bytes the least significant byte shall be encoded first; with the remaining bytes encoded in increasing order of significance.
In a character string consisting of multiple 8-bit single byte codes, the characters will be encoded in the order of occurrence in the **string** (left to right).

Virtual Memory Schemes

Every architecture has its own virtual memory system. However, most of these architectures contain common elements. Essentially, there is a translated portion of a virtual address and the untranslated portion. The untranslated portion is simply copied from the virtual address into the physical address. However, only those portions that are translated can have different protection bits set or cleared. Therefore, the larger the page size, the less control we have over its protection.

SOCKET : is one endpoint of a **two way** communication link between two programs running on the network.

Cores are physical processing units.A CPU refers to the whole computer chip, while the number of cores present on a single CPU can vary

Threads are virtual sequences of instructions given to a CPU. The more threads a CPU can execute at once, the more tasks it can complete.

2) CLOCK SPEED :

CPU speed is determined by how many calculations the processor can perform per cycle.

Clock speed is expressed in gigahertz — billions of cycles per second. Higher clock speeds generate more heat , higher clock speed means a faster CPU.

Clock speed of this computer is 3.60GHz .

3) BYTE ORDER : LITTLE ENDIAN

In a binary number consisting of multiple bytes the least significant byte shall be encoded first; with the remaining bytes encoded in increasing order of significance.

In a character string consisting of multiple 8-bit single byte codes, the characters will be encoded in the order of occurrence in the string (left to right).

L1d cache stores data, while the

L1i cache stores instructions for the cores to execute.

L1 cache, or primary cache, is extremely fast but relatively small, and is usually embedded in the processor chip as CPU cache.

L2 cache, or secondary cache, is often more capacious than L1. L2 cache may be embedded on the CPU, or it can be on a separate chip

Level 3 (L3) cache is specialized memory developed to improve the performance of L1 and L2.