DRAFT SEMINAR REPORT

RECONFIGURABLE PROCESSOR ARCHITECUTRE

Submitted by,

Deepak J Puthukkaden

Roll No: 20

EC7B

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ABSTRACT

Reconfigurable processors combine the speed of application specific integrated circuits (ASIC) and the universality of classical digital processors by means of adaptability to the currently executed code. There is a great number of varieties in today's reconfigurable processor architectures. Processor architectures can be specified in many ways. Architecture specifications are usually used during the architecture design phase and in software tools such as compilers and simulators. The aim of this seminar is to propose various comparison criteria for reconfigurable processor architectures and to give an overview of the specification methods for them.

Reconfigurable processors (RP) combine the speed of application specific integrated circuits (ASIC) and the universality of classical digital processors. ASIC circuits are the fastest way of processing digital data because they are pre-tailored for known functions. Classical processors spend a lot of time in fetching and decoding relatively small set of basic instructions. The main difference between classical processors and reconfigurable processors is that RPs try to adjust their internal structure to the currently executed code. Classical processors have fixed, unchangeable structure while all RPs have some changeable, adjustable components. These changeable components are called reconfigurable fabric (RF).