

DRAFT SEMINAR REPORT

RECONFIGURABLE PROCESSOR ARCHITECTURE

Submitted by,

Deepak J Puthukkaden

Roll No: 20

EC7B

ACKNOWLEDGEMENT

I wish to thank **Dr. V.P.Devassia**, Principal, Govt. Model Engineering College, for giving me the opportunity to conduct a detailed study and analysis of my seminar. I wish to thank **Mr. Jayachandran. E.S**, Associate Professor, Head of the Department of Electronics Engineering, for his support and faith in me for the completion of this seminar. I express my profound gratitude to **Ms. Shiji T.P**, Associate Professor, the coordinator of Electronics & Communications for allowing me to proceed with this seminar. I take this opportunity to express my profound gratitude and deep regards to my guide **Mr. Rashid M.E**, Associate professor, Department of Electronics Engineering, for his exemplary guidance, monitoring and constant encouragement throughout the course of this seminar. I would also like to thank all the teachers of the Department of Electronics for their whole hearted support.

Index

| Chapter No. | Chapter Name | Page No. |
|--------------------|--|-----------------|
| 1. | Introduction | 1 |
| 2. | History | 2 |
| 2.1 | ROM as PLD | 2 |
| 2.2 | Early Programmable Logic | 3 |
| 2.3 | Field Programmable Gate Array | 4 |
| 2.4 | Present day developments | 5 |
| 3. | Architecture | 7 |
| 3.1 | Implementation Spectrum | 7 |
| 3.1.1 | PLD | 8 |
| 3.1.2 | CPLD | 9 |
| 3.1.3 | FPGA | 10 |
| 3.2 | System Level Architecture | 11 |
| 3.2.1 | External Stand-Alone Processing Unit | 11 |
| 3.2.2 | Attached Processing Unit | 12 |
| 3.2.3 | Co-Processor | 12 |
| 3.2.4 | Reconfigurable Functional Unit | 13 |
| 3.2.5 | Processor Embedded In Reconfigurable Fabric | 14 |
| 3.3 | Granularity | 15 |
| 3.3.1 | Fine-grained Architecture | 15 |
| 3.3.2 | Coarse-grained Architecture | 16 |
| 3.4 | Programmable Logic Elements | 18 |
| 3.4.1 | Look Up Table (LUT) | 18 |
| 3.4.2 | Configurable Logic Blocks (CLB) | 19 |
| 3.5 | Reconfiguration Models | 20 |
| 3.5.1 | Static Reconfiguration | 21 |
| 3.5.2 | Partial Reconfiguration | 22 |
| 3.5.3 | Dynamic Reconfiguration | 22 |
| 4. | Advantaged and Limitations | 23 |
| 4.1 | Advantages of Reconfigurable Processors | 23 |
| 4.2 | Limitation of Reconfigurable Processors | 23 |
| 5. | Applications | 24 |
| 6. | Conclusion | 25 |

ABSTRACT

Reconfigurable processors combine the speed of application specific integrated circuits (ASIC) and the universality of classical digital processors by means of adaptability to the currently executed code. There is a great number of varieties in today's reconfigurable processor architectures. Processor architectures can be specified in many ways. Architecture specifications are usually used during the architecture design phase and in software tools such as compilers and simulators. The aim of this seminar is to propose various comparison criteria for reconfigurable processor architectures and to give an overview of the specification methods for them.

Reconfigurable processors (RP) combine the speed of application specific integrated circuits (ASIC) and the universality of classical digital processors. ASIC circuits are the fastest way of processing digital data because they are pre-tailored for known functions. Classical processors spend a lot of time in fetching and decoding relatively small set of basic instructions. The main difference between classical processors and reconfigurable processors is that RPs try to adjust their internal structure to the currently executed code. Classical processors have fixed, unchangeable structure while all RPs have some changeable, adjustable components. These changeable components are called reconfigurable fabric (RF).