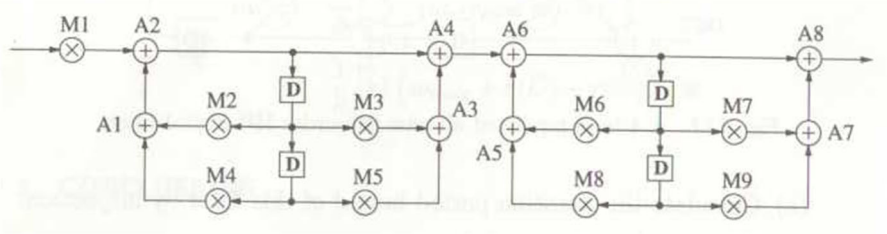
2023 Spring VLSI DSP Homework Assignment #6

Due date: 2023/6/13

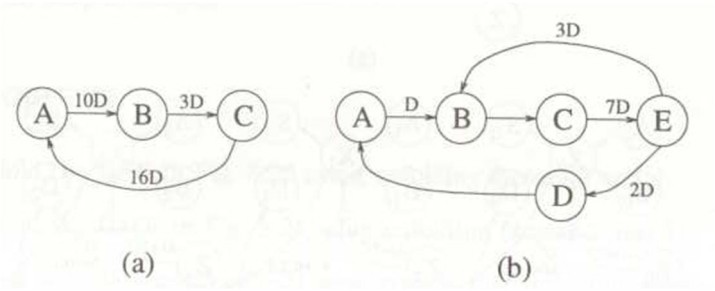
Q1. The DFG shown below describes a 4th order IIR digital filter implemented as cascade of two 2nd order sections. Assume each multiply require 2 u.t. and add requires 1 u.t.

a) What is the critical path of the DFG? What is the iteration bound of the DFG?

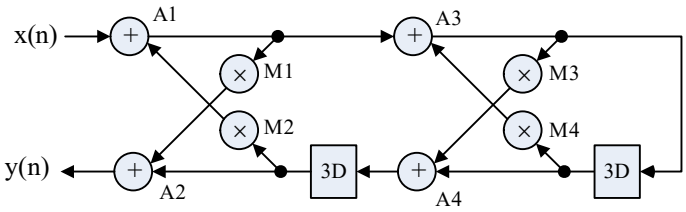
b) Retime and pipeline the DFG to minimize the clock period. What is the minimum achievable clock period obtained with pipelining and retiming?



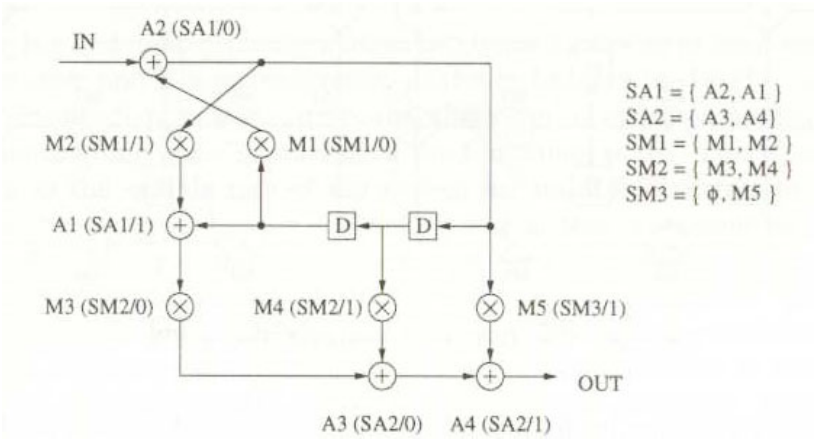
Q2. Unfold the DFG shown below using unfolding factors 2 and 5



Q3. For the DFG shown below, assume the computing times of multiplier and adder are 3 u.t and 1 u.t., respectively. Unfold the design by a factor of 2 and apply retiming to achieve a critical path delay of 6 u.t..



Q4. For the design shown below.



a) For a folded design with 5 folding sets (SA1, SA2, SM1, SM2, SM3) and a folding factor equal to 2, verify if this is a valid folding

b) If it is not, find a new valid folding design by modifying the folding orders in each set. **Note:** Each folding set has only two possible folding orders. In total, there are 32 possible combinations of folding orders. You may write a program to enumerate all 32 possible combinations and check if any of them are valid.

c) In case, you cannot identify any valid combinations of folding orders in (b), perform retiming first followed by folding

d) Derive your folded design without register minimization based on the folding obtained in (b) or (c). You need to draw the folded circuit design.

e) Repeat (d) using the forward backward register allocation scheme to minimize the register usage. **Note:** you need to show the derivation details, e.g. life time chart, register allocation table, and so on.