

Ch5 note

p5-1~p5-12 note

1. 同個hyperplane為相同執行順序
 2. 同個projection為同樣一顆processor
 3. normal vector (\vec{s}) 垂直於hyperplane, length由DG維度決定
 4. components of the scheduling vector \vec{s} must be co-prime(互質)
 5. schedule of node i = inner product of \vec{s} & i
 6. nodes on the same hyperplane should not be assigned to the same processor to preserve computing parallelism
- Observe partial ordering(precedence relation)
 $\vec{s}^t \cdot \vec{e} \geq 0$ for all \vec{e} (單位向量)
 - Preserve parallelism
 $\vec{s}^t \cdot \vec{d} \neq 0$ for projection vector \vec{d}
7. Type of schedules
 - default schedule $\Rightarrow \vec{s} = \vec{d}$
 - Resursion schdule $\Rightarrow \vec{s}$ is parallel to one of axis in the index space of the DG, usually the recursion direction
 - Systolic schedule \Rightarrow at least one delay on each edge of SFG
 8. example 在講義5-9~5-11
 - pipeline period $\alpha = \vec{s}^t \cdot \vec{d}$ (number of clock cycles between two successive computations)

P5-13~

1. \vec{P} is the processor basis or processor allocation matrix, and their dim is $(N-1) \times N$ (N is DG dimension)
 - spatial mapping
 - $\vec{P} \cdot \vec{e} = 0$, where \vec{d} is projection vector
 - process index $\vec{n} = \vec{P} \cdot \vec{i}$
2. Timing mapping
 - time index $t = \vec{s}^t \cdot \vec{i}$, \vec{s}^t is the scheduling vector
3. Transfer matrix is $T = \begin{bmatrix} \vec{s}^t \\ \vec{P} \end{bmatrix}$
4. Mapping procedures
 - Node mapping

$$\begin{bmatrix} \vec{t}(\vec{i}) \\ \vec{n} \end{bmatrix} = \begin{bmatrix} \vec{s}^t \\ \vec{P} \end{bmatrix} \cdot \begin{bmatrix} \vec{i} \end{bmatrix}$$

\vec{i} is DG node, $t(\vec{i})$ is schedule, \vec{n} is Processor index

- Arc mapping

$$\begin{bmatrix} \vec{D}(\vec{e}) \\ \vec{e} \end{bmatrix} = \begin{bmatrix} \vec{s}^t \\ P \end{bmatrix} \cdot \begin{bmatrix} \vec{a} \end{bmatrix}$$

\vec{a} is DG arc, $D(\vec{e})$ is edge delay, \vec{e} is SFG edge

- IO mapping

$$\begin{bmatrix} \vec{t}(\vec{c}) \\ \vec{n} \end{bmatrix} = \begin{bmatrix} \vec{s}^t \\ P \end{bmatrix} \cdot \begin{bmatrix} \vec{c} \end{bmatrix}$$

\vec{c} is I/O node, $t(\vec{c})$ is schedule, \vec{n} is Processor index

Mapping example: insertion sorting (1)

■ DG of sorting algorithm

■ Insertion sorting

- Sorted result will be stored in each node
- Each time a new value x entered, it will be inserted into a proper position
- Choose $\underline{d} = \underline{s} = [1 \ 0]^t$, and $P = [0 \ 1]$

Node mapping $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} i \\ j \end{bmatrix} = \begin{bmatrix} i \\ j \end{bmatrix}$

Arc mapping $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 0 \\ 1 \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$

No delay $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 0 \\ 1 \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$

one delay $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$

I/O mapping $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i \\ 1 \end{bmatrix} = \begin{bmatrix} i \\ 1 \end{bmatrix}$

output: $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} N \\ j \end{bmatrix} = \begin{bmatrix} N \\ j \end{bmatrix}$

Handwritten notes:

- 第i時間 (Time i)
- 第j process (Process j)
- 往下個 process 傳 (SFG edge) (Pass to next process)
- keep value (keep value)
- keep 在原 reg (keep in original register)

VLSI DSP 2019 Y.T. Hwang 5-16

Ref

[1] 如何在 Markdown 輸入數學公式及符號

[2] Markdown 文本居中、字体颜色以及数学公式