Introduce to

Field Programmable Logic Device

Ref: 1. Michael Shyu, VLSI system lab, NCTU
2. Lattice datasheets
3. Xilinx datasheets

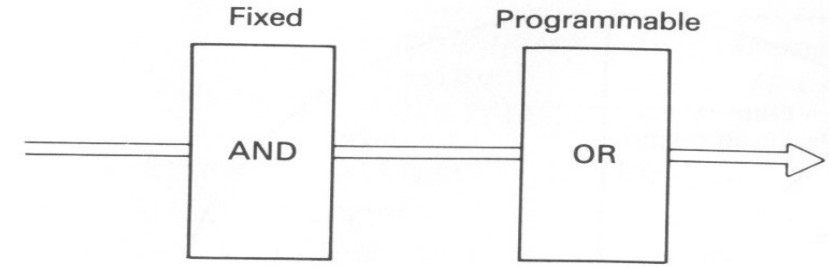
Digital System Implementation

- Full Custom

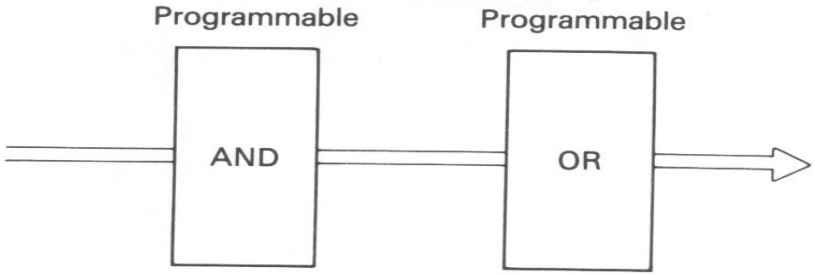
- Semi-custom
  - Gate array
  - Standard cells

- Programmable Logic Device
  - Programmable read only memory (PROM)
  - Field programmable logic array (FPLA)
  - Programmable array logic (PAL)

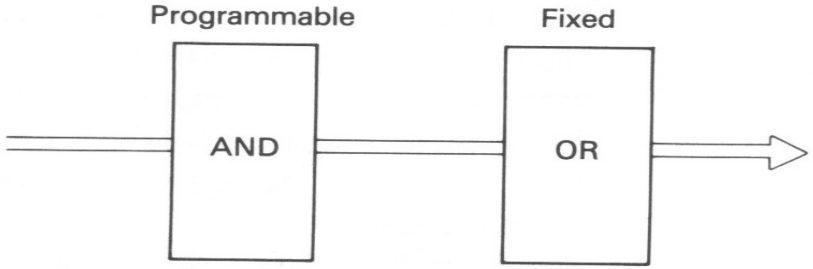
Structure of Programmable Logic Device



(a) PROM



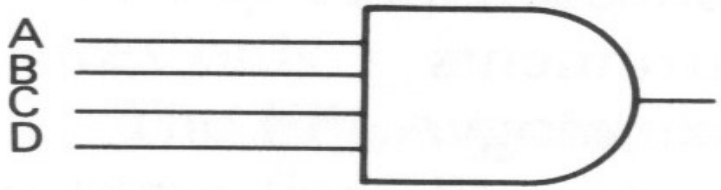
(b) FPLA

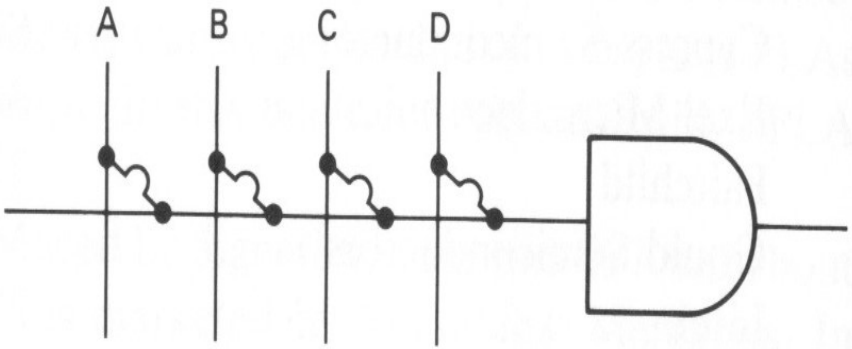


(c) PAL

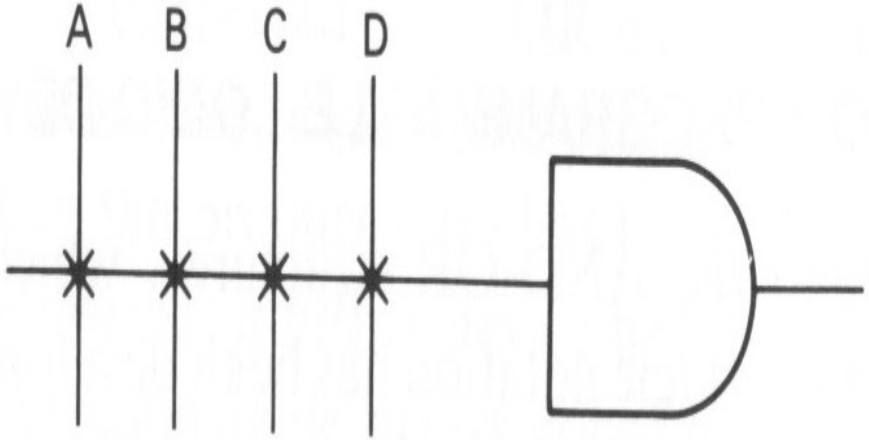
Programmable Logic Notation

A four-input AND gate



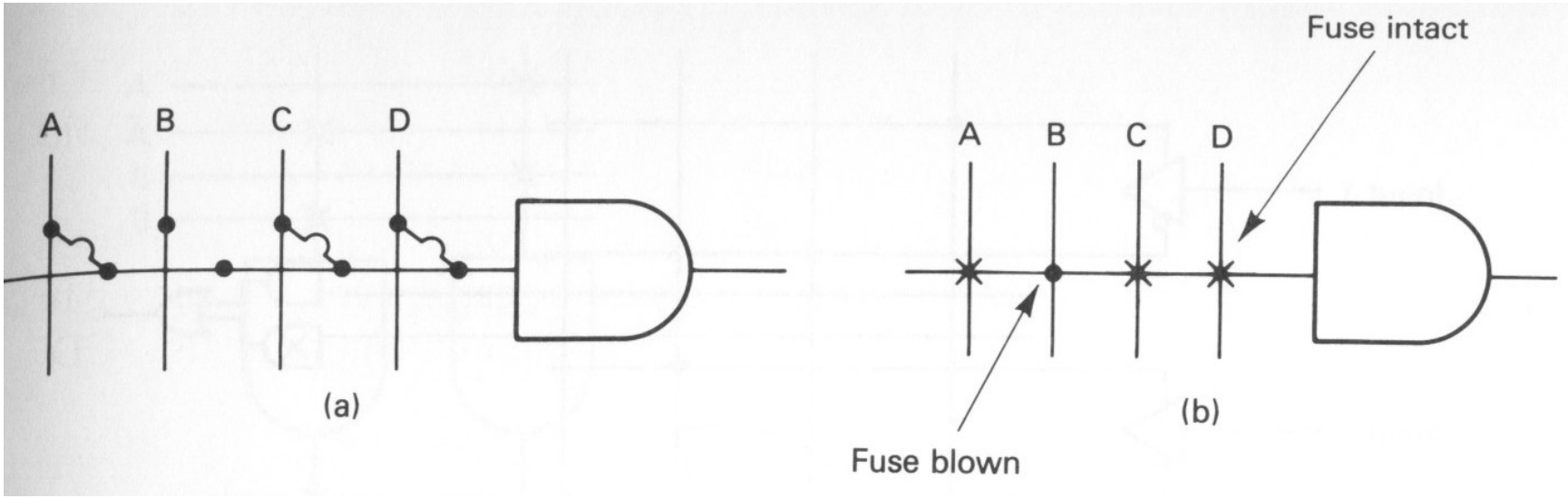


Fusible input connections to the AND gate



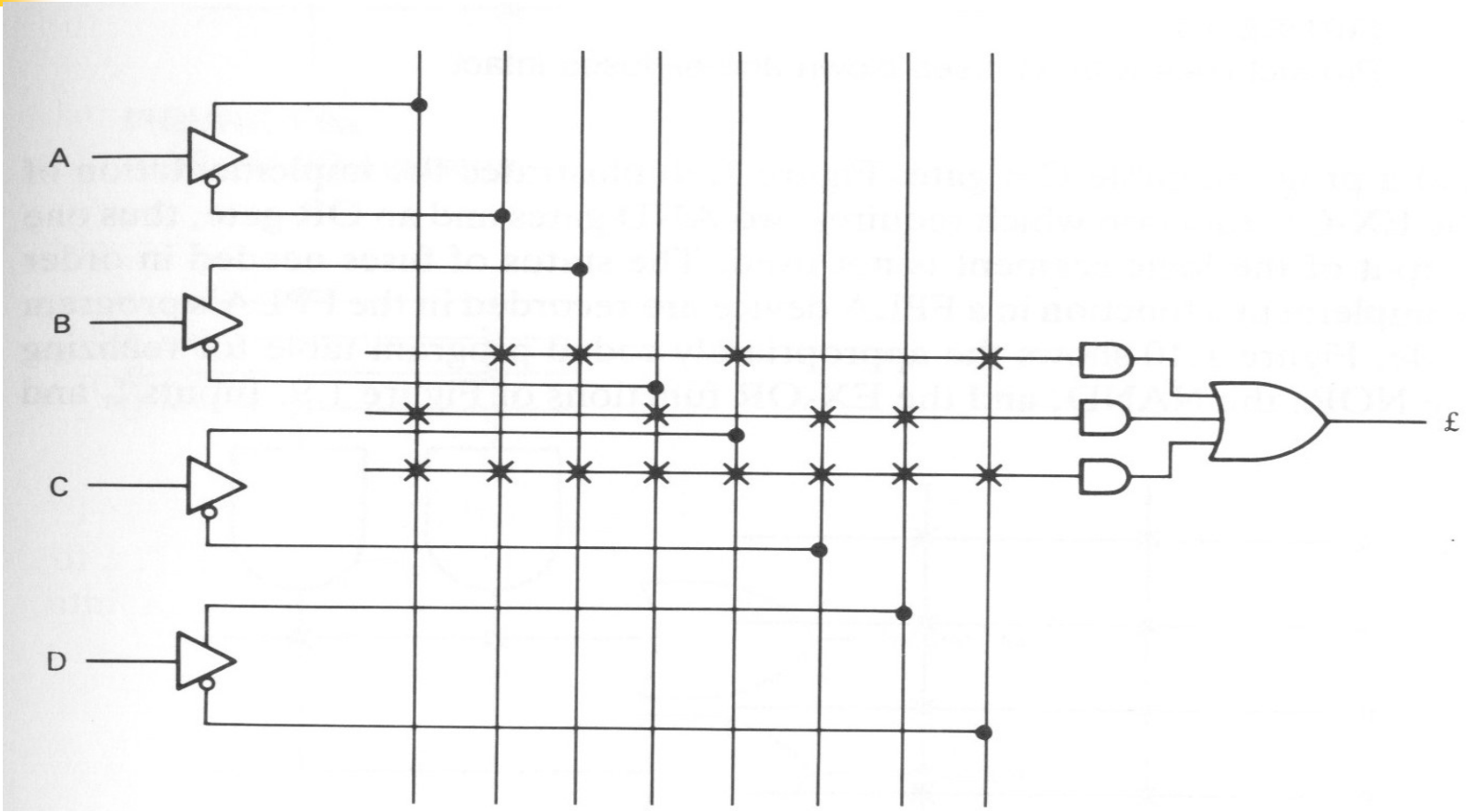
Notation.

Programmable Logic Notation



Product line implements ACD

Programmable Logic Notation



Portion of the programmable logic array programmed to implement $f(A,B,C,D) = \overline{A}BC\overline{D} + A\overline{B}\overline{C}D$

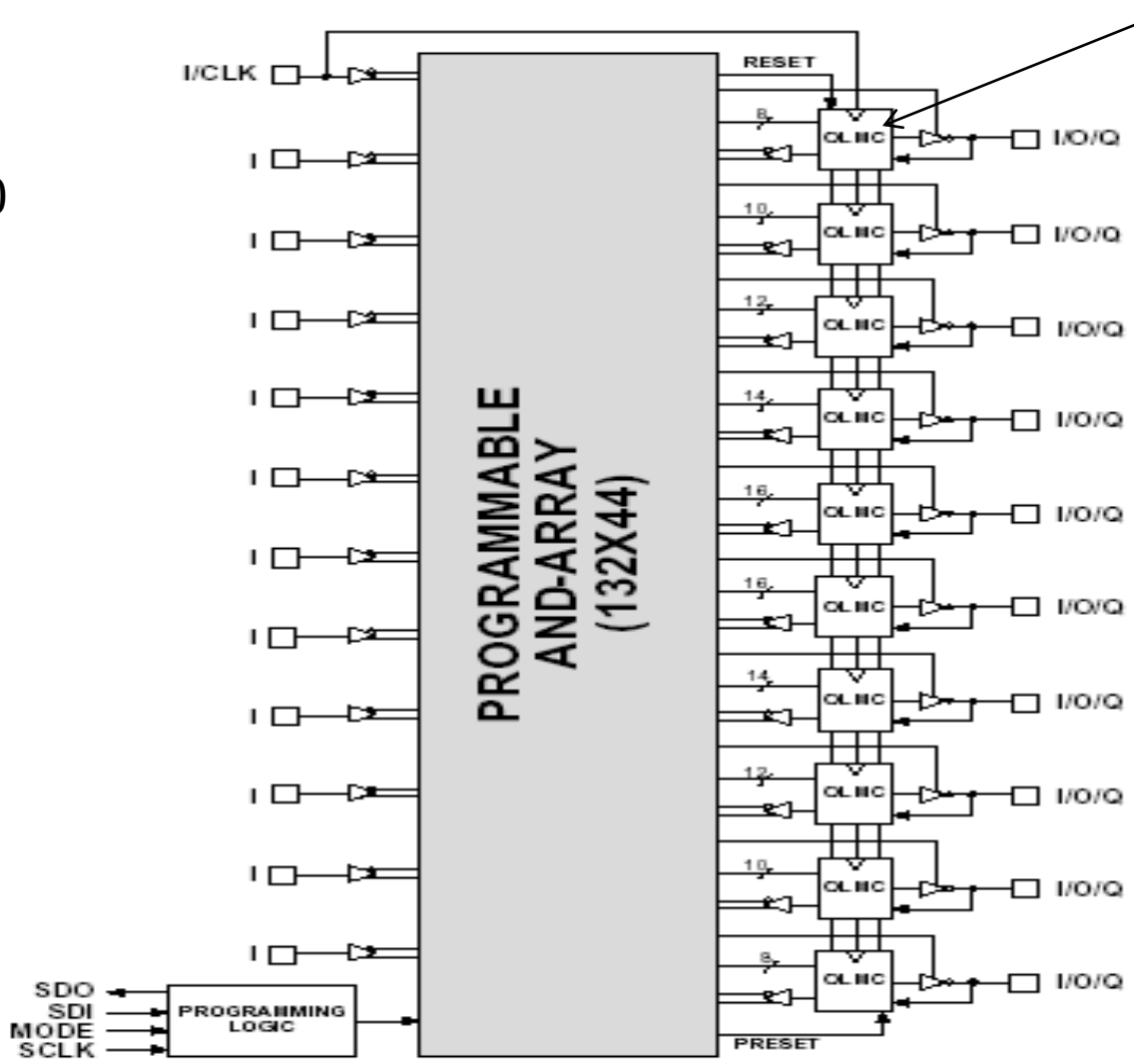
Field Programmable Logic Device

- Function is specified by the user after the device is manufactured.

- FPLD families
  - SPLD (*Simple Programmable Logic Device*)
  - CPLD (*Complex Programmable Logic Device*)
    - : Xilinx XC9500
  - FPGA (*Field Programmable Gate Arrays*)
    - : Xilinx XC3000, VirtexE, VirtexII

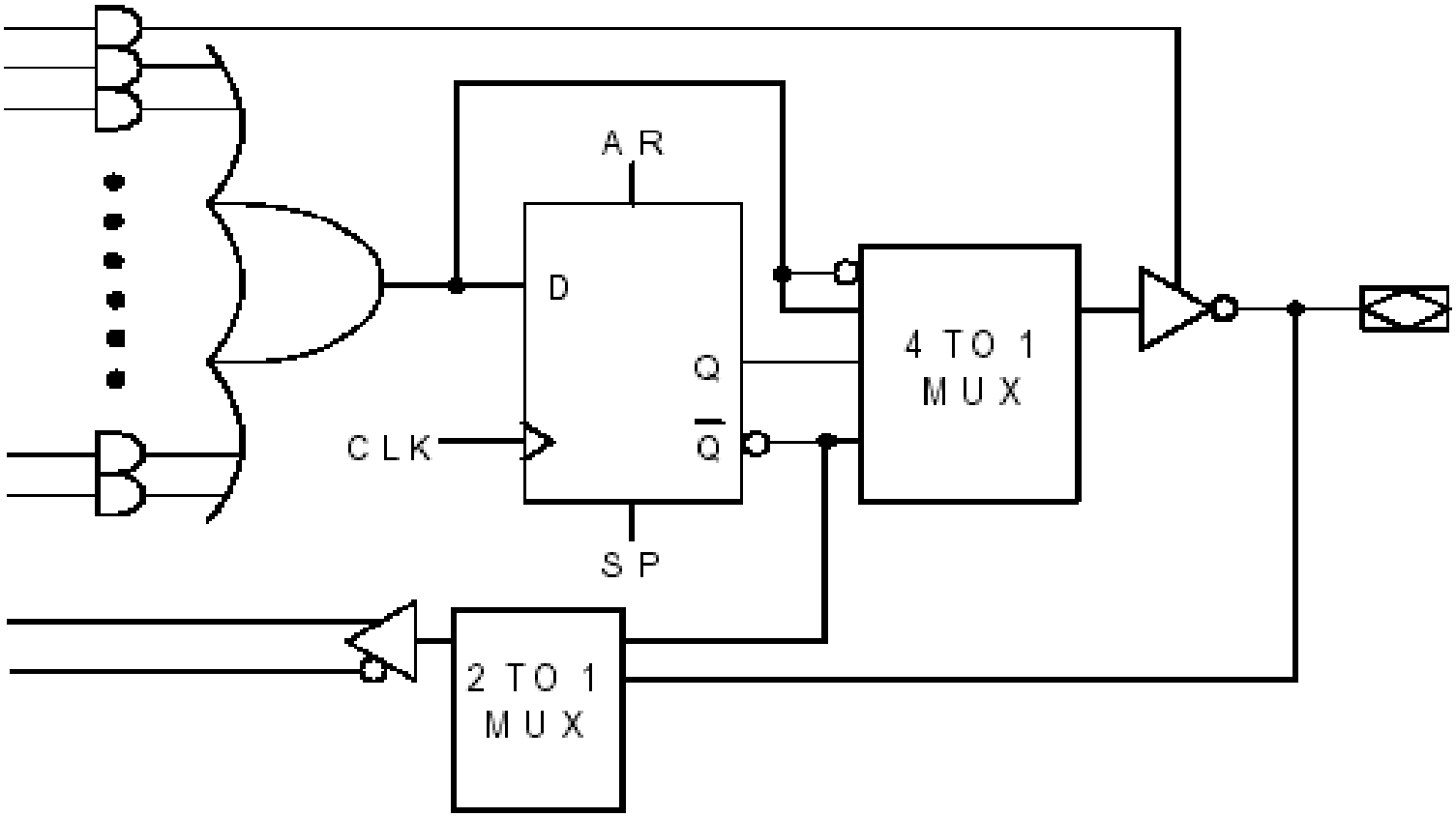
SPLD

Lattice
ispGAL22v10



OLMC
See next slide

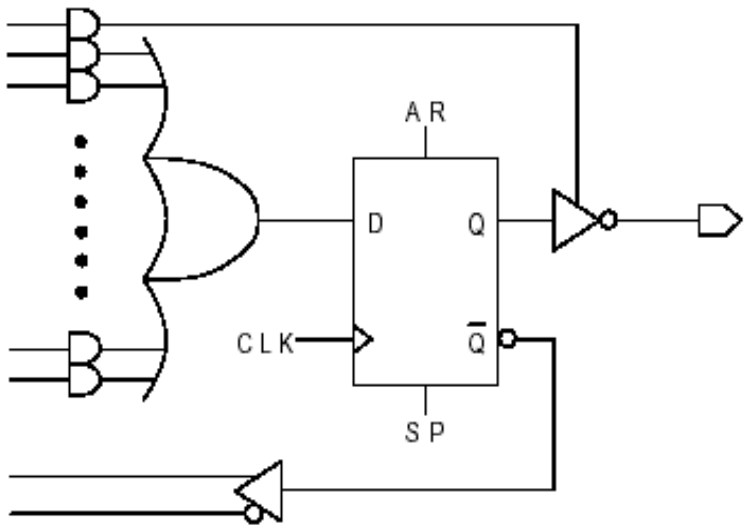
SPLD



ispGAL22V10 OUTPUT LOGIC MACROCELL (OLMC)

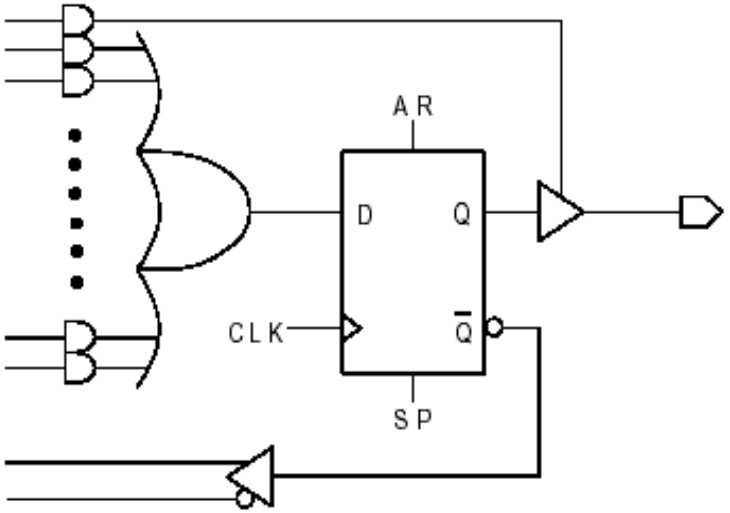
SPLD

Registered Mode



ACTIVE LOW

$S_0 = 0$
$S_1 = 0$

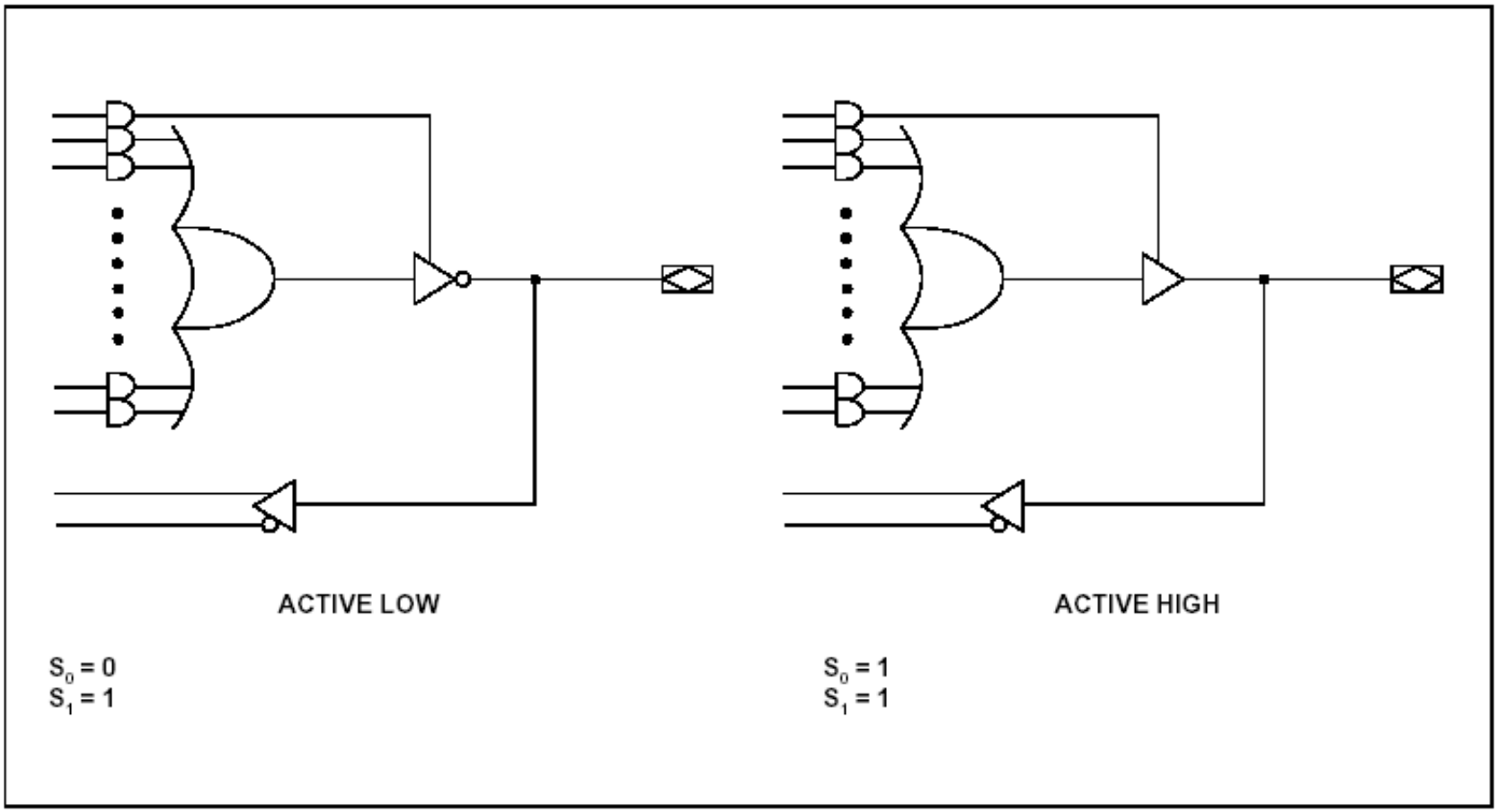


ACTIVE HIGH

$S_0 = 1$
$S_1 = 0$

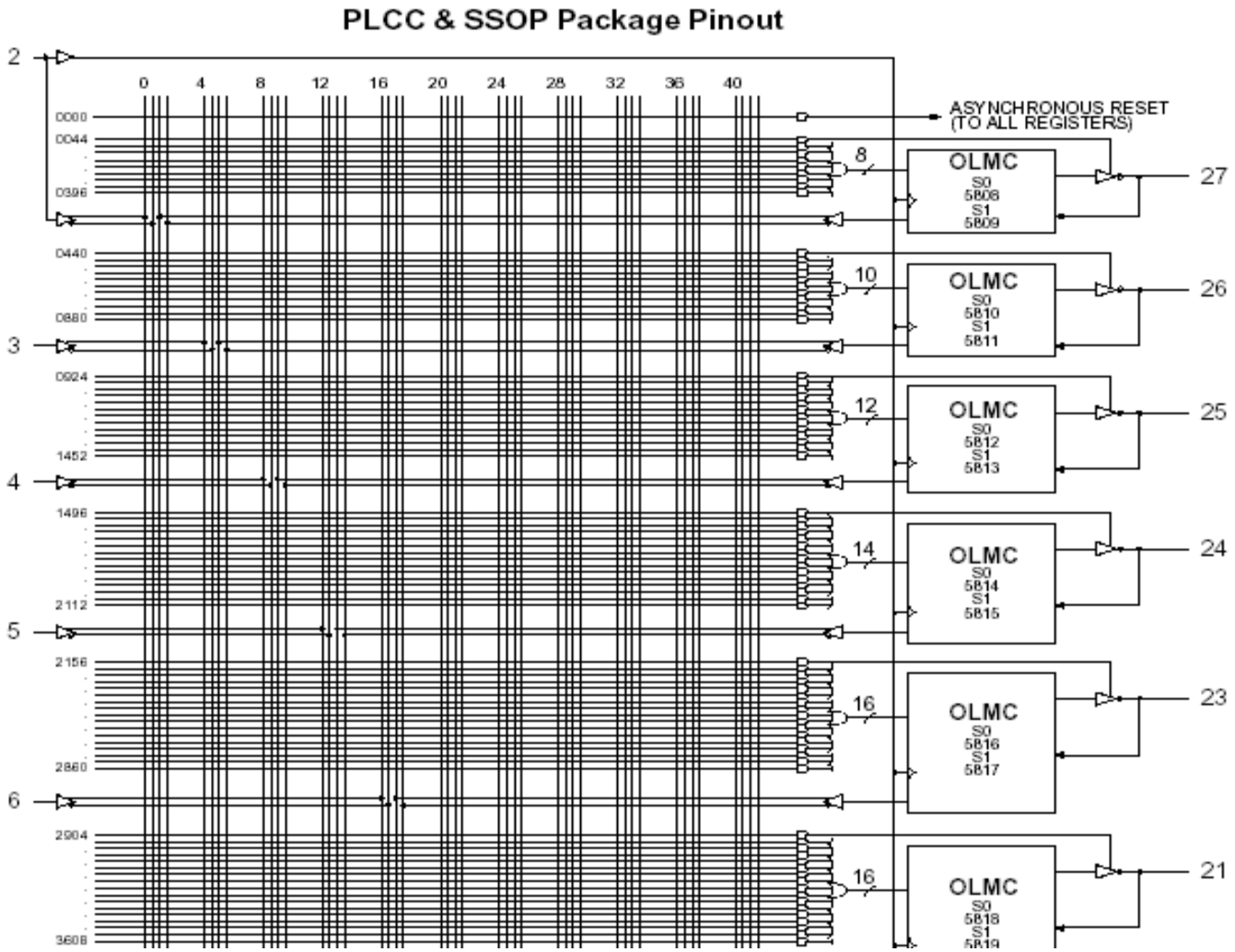
SPLD

Combinatorial Mode



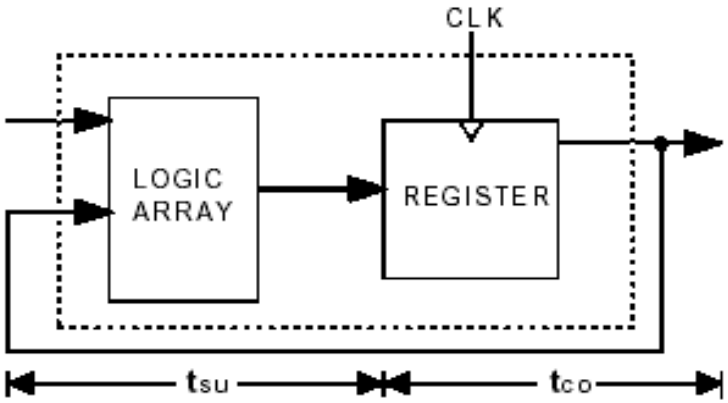
SPLD

ispGAL22V10 Logic Diagram/JEDEC Fuse Map



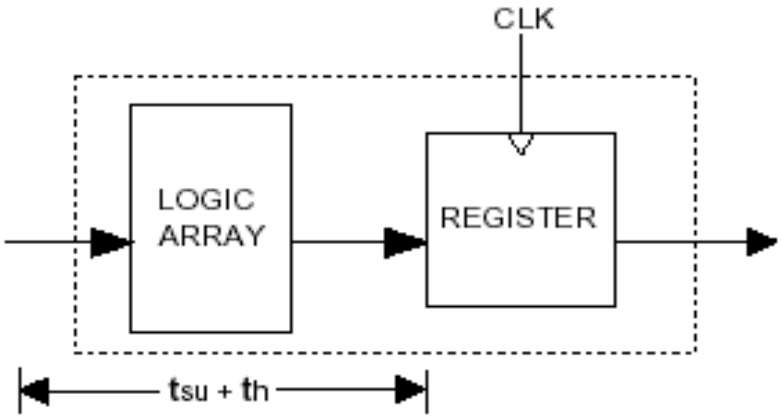
SPLD

PARAMETER	TEST COND.[1]	DESCRIPTION
t_{pd}	A	Input or I/O to Combinatorial Output
t_{co}	A	Clock to Output Delay
t_{cf}[2]	—	Clock to Feedback Delay
t_{su_1}	—	Setup Time, Input or Feedback before Clock↑
t_{su_2}	—	Setup Time, SP before Clock↑
t_h	—	Hold Time, Input or Feedback after Clock↑



fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

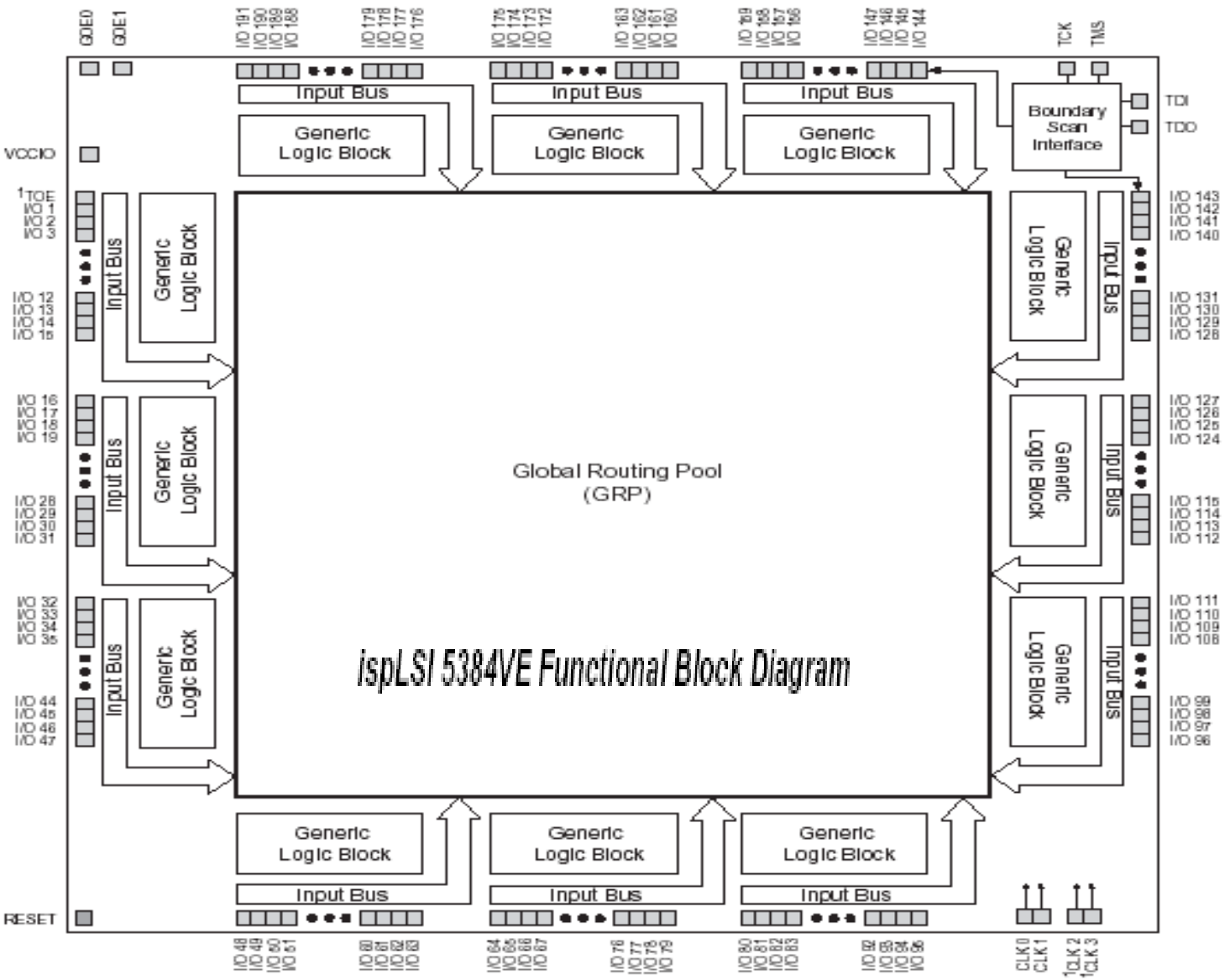
CPLD

Table 1. ispLSI 5000VE Family Attributes

	5128VE	5256VE	5384VE	5512VE
Density (PLD Gates)	6,000	12,000	18,000	24,000
Speed: f_{max} (MHz)	180	165	165	155
Speed: t_{pd} (ns)	5.0	6.0	6.0	6.5
Macrocells	128	256	384	512
Registers	128	256	384	512
I/O	96	72/96/144	192	192/256
Pin/Package	128 TQFP	100 TQFP 128 TQFP 256 fpBGA 272 BGA	256 fpBGA 272 BGA	256 fpBGA 272 BGA 388 fpBGA 388 BGA

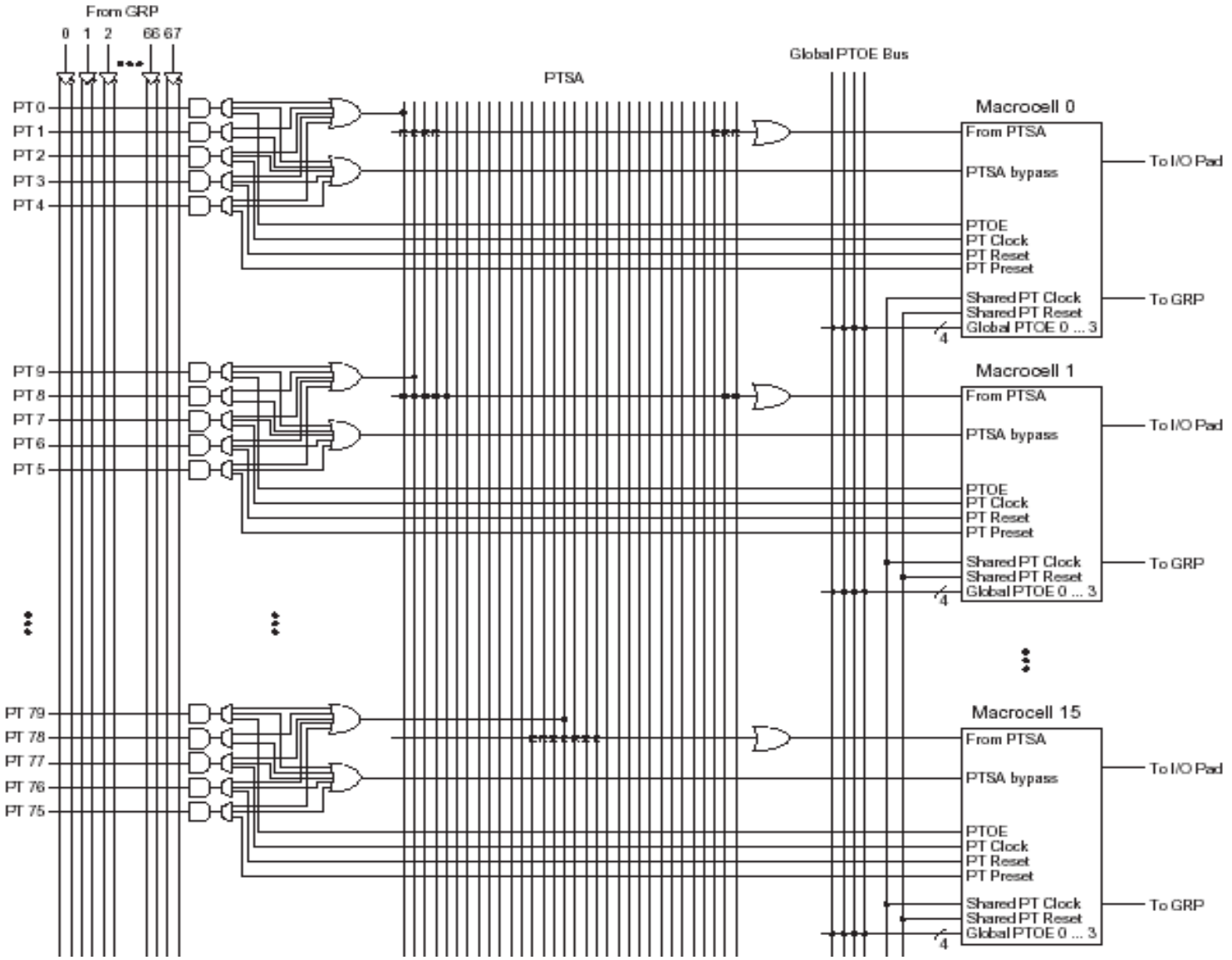
5KVE attributes

CPLD

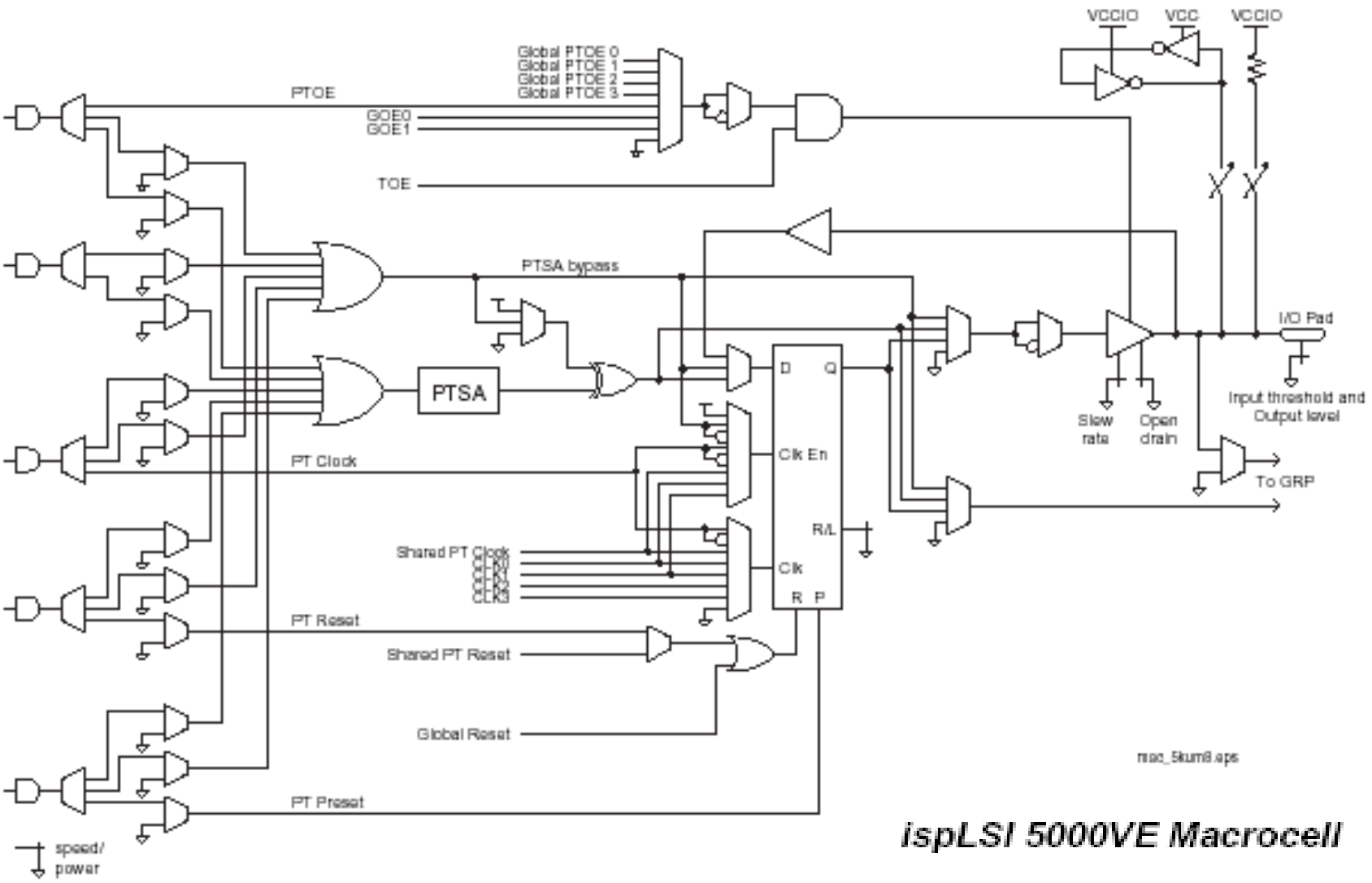

GOE0
GOE1
I/O 191
I/O 190
I/O 189
I/O 188
I/O 179
I/O 178
I/O 177
I/O 176
I/O 175
I/O 174
I/O 173
I/O 172
I/O 163
I/O 162
I/O 161
I/O 160
I/O 159
I/O 158
I/O 157
I/O 156
I/O 147
I/O 146
I/O 145
I/O 144
TCK
TMS
TDI
TDO
Boundary Scan Interface
Input Bus
Generic Logic Block
VCCIO
1TOE
I/O 1
I/O 2
I/O 3
I/O 12
I/O 13
I/O 14
I/O 15
I/O 16
I/O 17
I/O 18
I/O 19
I/O 28
I/O 29
I/O 30
I/O 31
I/O 32
I/O 33
I/O 34
I/O 35
I/O 44
I/O 45
I/O 46
I/O 47
I/O 143
I/O 142
I/O 141
I/O 140
I/O 131
I/O 130
I/O 129
I/O 128
I/O 127
I/O 126
I/O 125
I/O 124
I/O 115
I/O 114
I/O 113
I/O 112
I/O 111
I/O 110
I/O 109
I/O 108
I/O 99
I/O 98
I/O 97
I/O 96
Global Routing Pool
(GRP)
ispLSI 5384VE Functional Block Diagram
RESET
I/O 48
I/O 49
I/O 50
I/O 51
I/O 60
I/O 61
I/O 62
I/O 63
I/O 64
I/O 65
I/O 66
I/O 67
I/O 76
I/O 77
I/O 78
I/O 79
I/O 80
I/O 81
I/O 82
I/O 83
I/O 92
I/O 93
I/O 94
I/O 95
CLK 0
CLK 1
CLK 2
CLK 3

CPLD

ispLSI 5000VE GLB

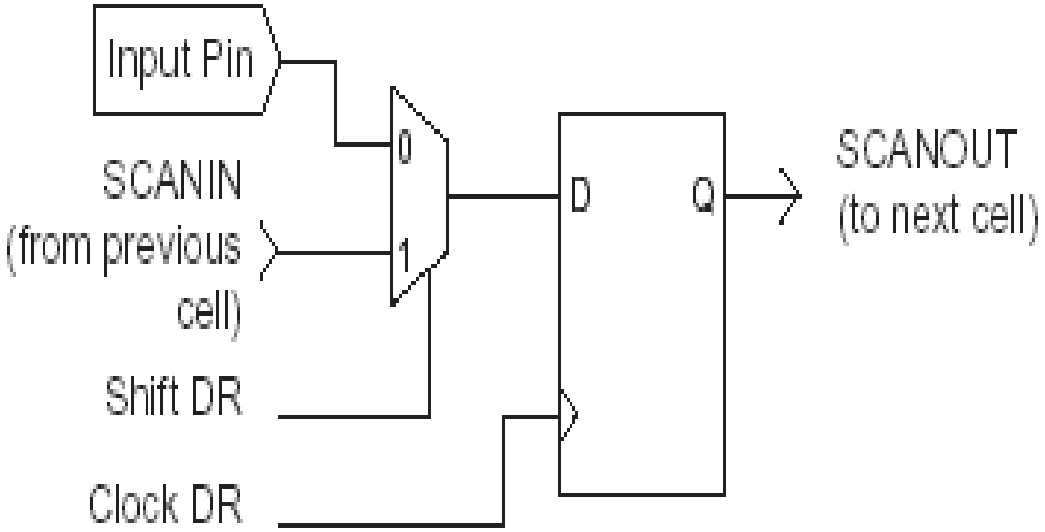


CPLD


VCCIO
VCC
VCCIO
Global PTOE 0
Global PTOE 1
Global PTOE 2
Global PTOE 3
PTOE
GOE0
GOE1
TOE
PTSA bypass
PTSA
PT Clock
Shared PT Clock
PT Reset
Shared PT Reset
Global Reset
PT Preset
speed/
power
D
Q
Clk En
R/L
Clk
R P
I/O Pad
Slew
rate
Open
drain
Input threshold and
Output level
To GRP
mac_5kum8.eps
ispLSI 5000VE Macrocell

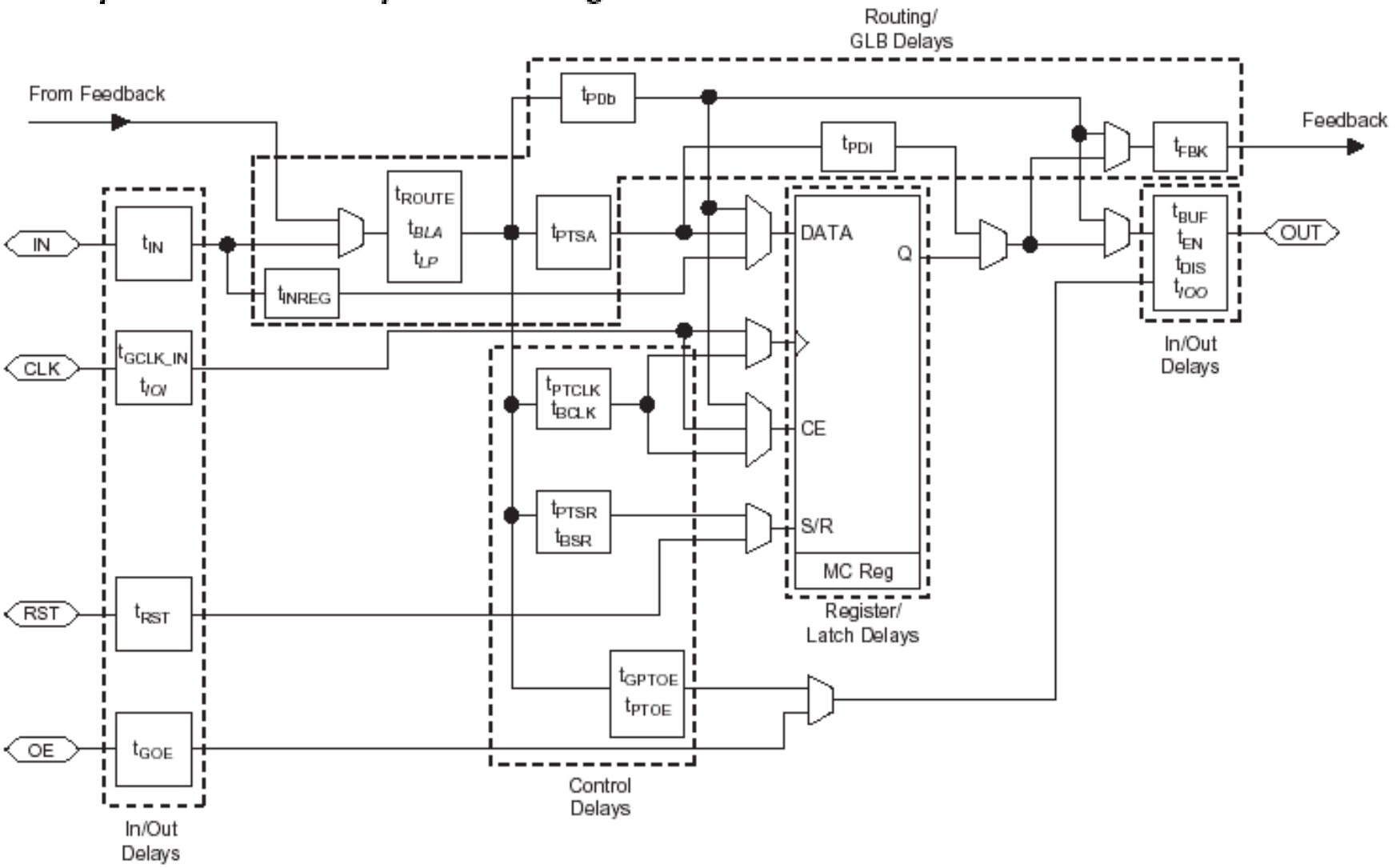
CPLD

Boundary Scan Register for Dedicated Input Pins



CPLD

ispLSI 5000VE Simplified Timing Model



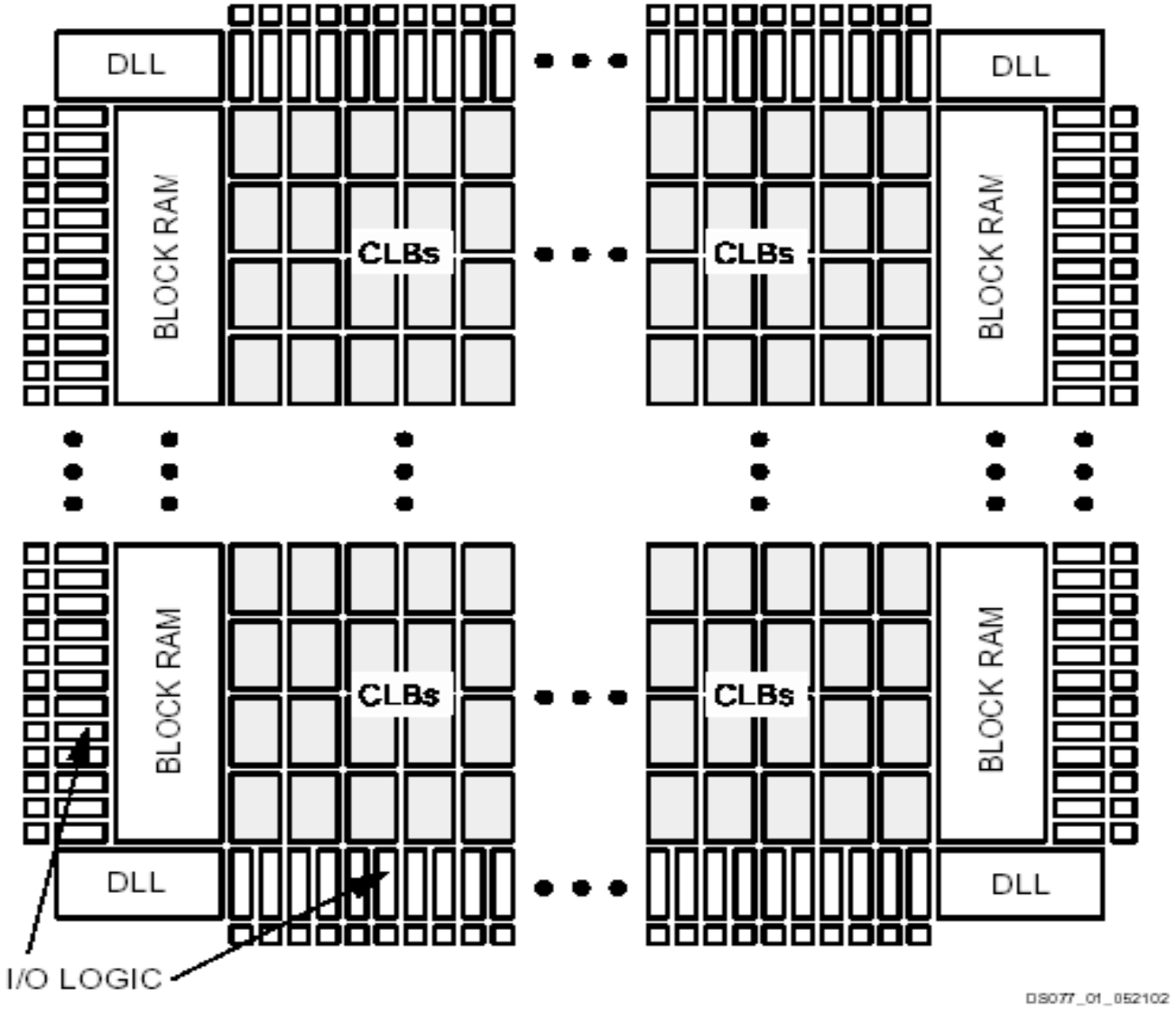
FPGA

Table 1: **Spartan-IIE FPGA Family Members**

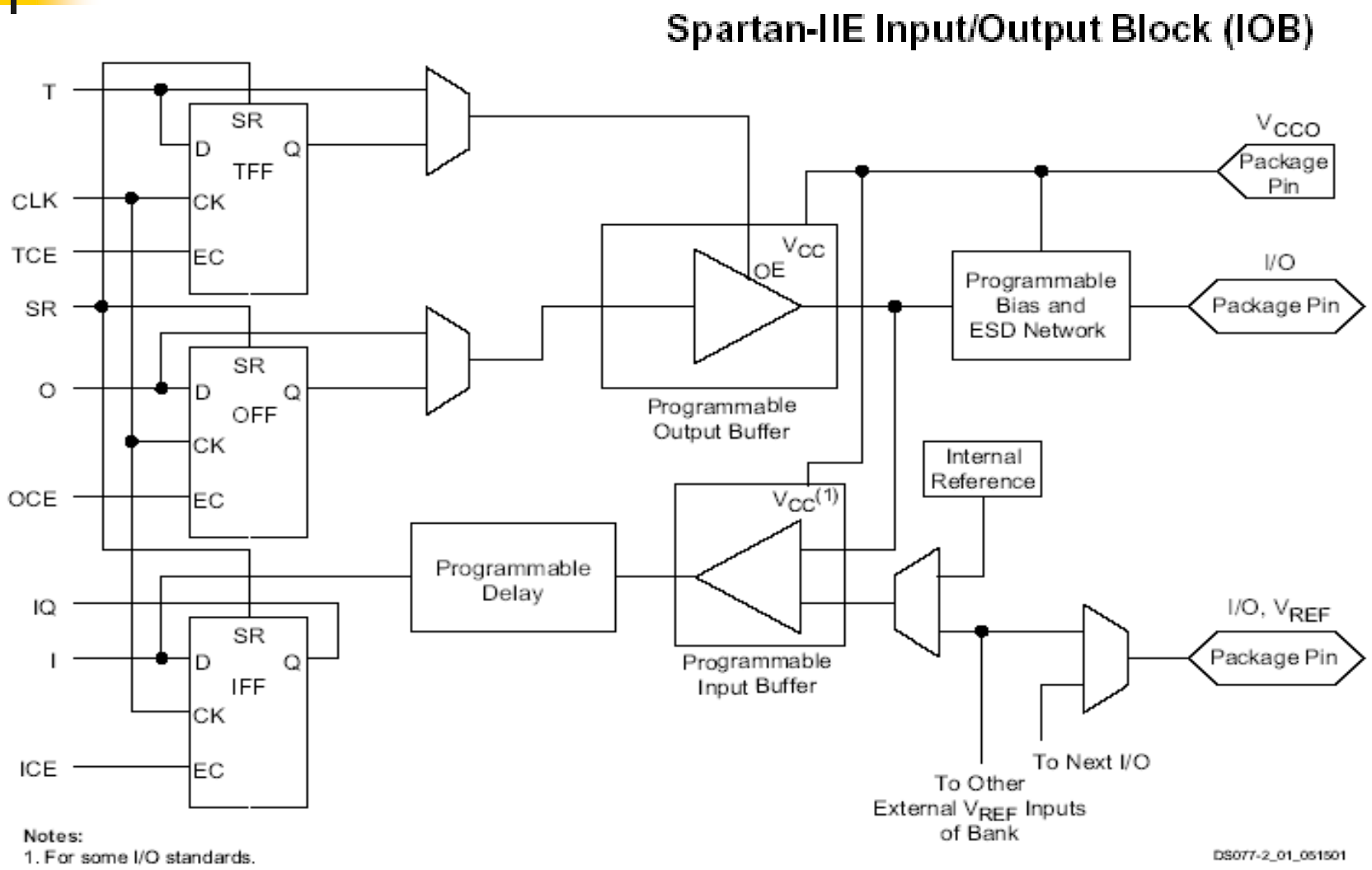
Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O(1)	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	83	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	202	86	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	265	114	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	289	120	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K
XC2S400E	10,800	145,000 - 400,000	40 x 60	2,400	410	172	153,600	160K
XC2S600E	15,552	210,000 - 600,000	48 x 72	3,456	514	205	221,184	288K

FPGA

FPGA Block Diagram

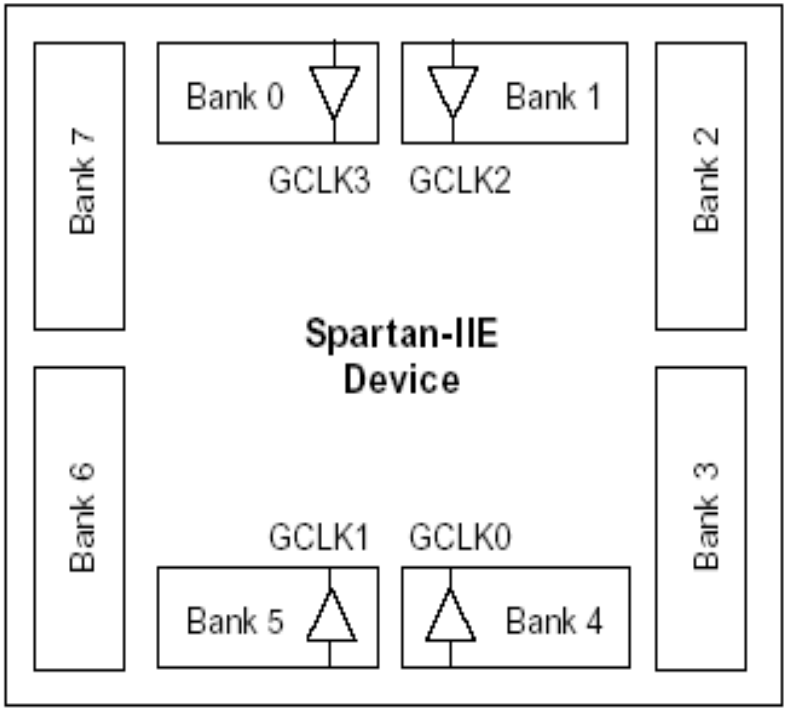


FPGA


Spartan-IIE Input/Output Block (IOB)
T
CLK
TCE
SR
O
OCE
IQ
I
ICE
SR
D
Q
TFF
CK
EC
SR
D
Q
OFF
CK
EC
SR
D
Q
IFF
CK
EC
Programmable Delay
OE
VCC
Programmable Output Buffer
VCC(1)
Programmable Input Buffer
Internal Reference
VCCO
Package Pin
Programmable Bias and ESD Network
I/O
Package Pin
I/O, VREF
Package Pin
To Next I/O
To Other External VREF Inputs of Bank
Notes:
1. For some I/O standards.
DS077-2_01_051501

FPGA

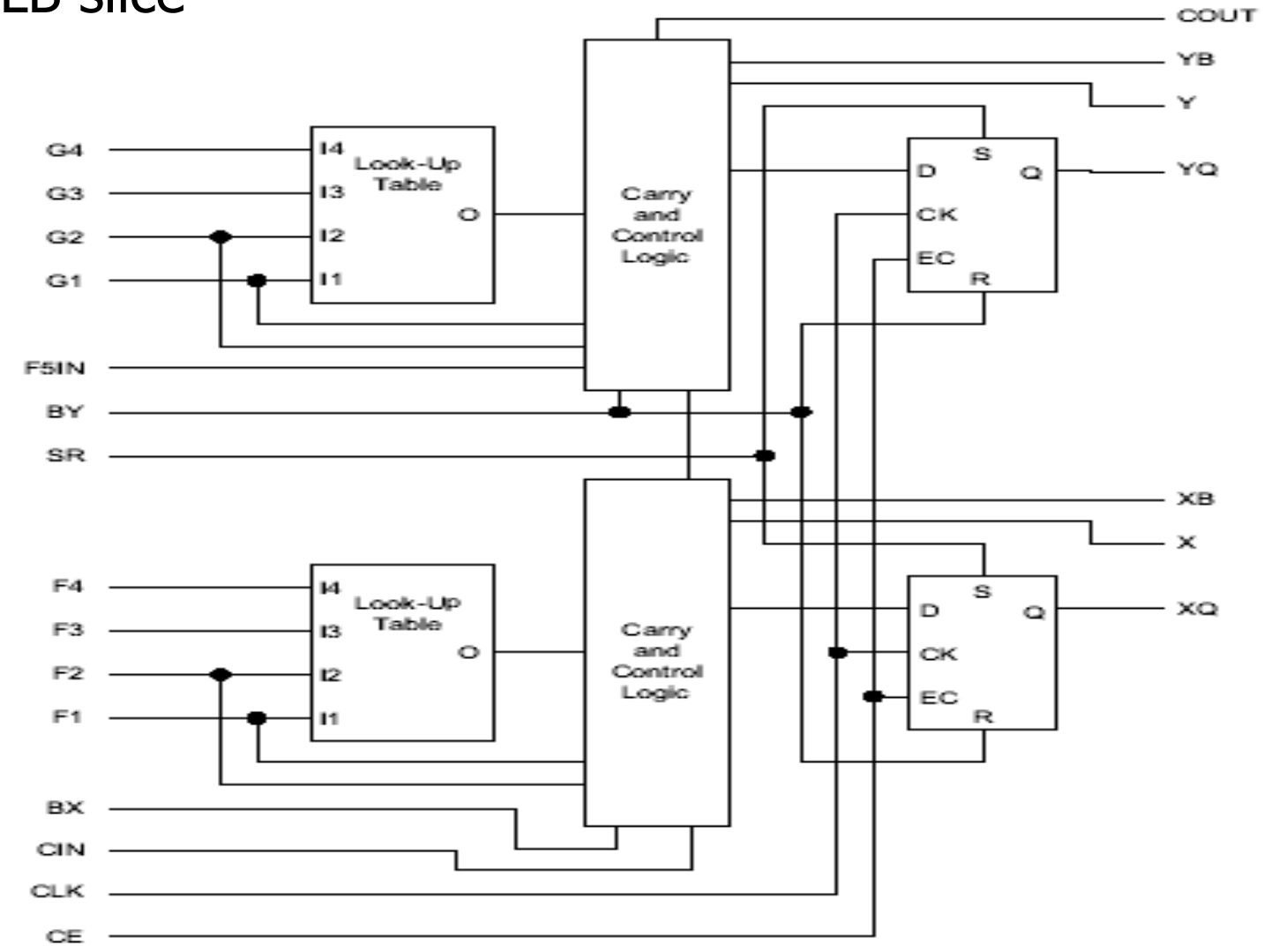
Spartan-IIE I/O Banks



V_{CCO}	Compatible Standards
3.3V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, LVPECL, GTL, GTL+
2.5V	SSTL2 I, SSTL2 II, LVCMOS2, LVDS, Bus LVDS, GTL, GTL+
1.8V	LVCMOS18, GTL, GTL+
1.5V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

FPGA

CLB slice



FPGA