Introduction to Xilinx

FPGA Design Workshop

Objectives

After completing this section, you will be able to. . .

- **Describe who Xilinx is**
- **Describe where Programmable Logic fits into the Engineering Curriculums**
- **List the Xilinx Products necessary to set up a lab**

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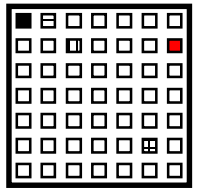
Who is Xilinx?

- World's leading innovator of complete programmable logic solutions



Programmable Logic Devices

ISE Alliance and Foundation Series Design Software

- Inventor of the Field Programmable Gate Array
- Fabless* Semiconductor and Software Company
  - **UMC (Taiwan)** **{*Xilinx acquired an equity stake in UMC in 1996}**
  - **Seiko Epson (Japan)**
  - **TSMC (Taiwan)**

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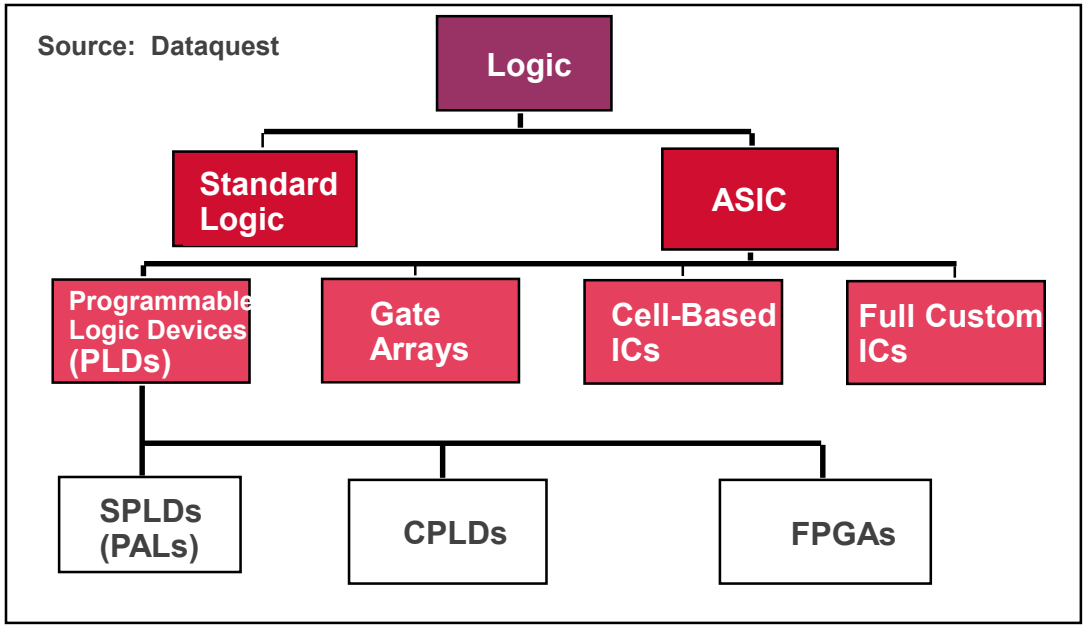
XILINX

Electronic Components



Acronyms

SPLD = Simple Prog. Logic Device
PAL = Prog. Array of Logic
CPLD = Complex PLD
FPGA = Field Prog. Gate Array

Common Resources

Configurable Logic Blocks (CLB)
- Memory Look-Up Table
- AND-OR planes
- Simple gates

Input / Output Blocks (IOB)
- Bidirectional, latches, inverters, pullup/pulldowns

Interconnect or Routing
- Local, internal feedback, and global

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Programmable Logic Solution

- No high development cost barriers
- Recovered time for authoring and innovating
  - **SW improvements reduce design iterations**
- No lengthy prototyping cycle
- Ability to remotely upgrade any networked system
- Ultimate flexibility to manage rapid change

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Where Programmable Logic Fits into the Electronics Industry

Key components of an electronics system:

- Processor
- Memory
- *Logic*

Xilinx is the Leading Innovator of Complete Programmable Logic Solutions

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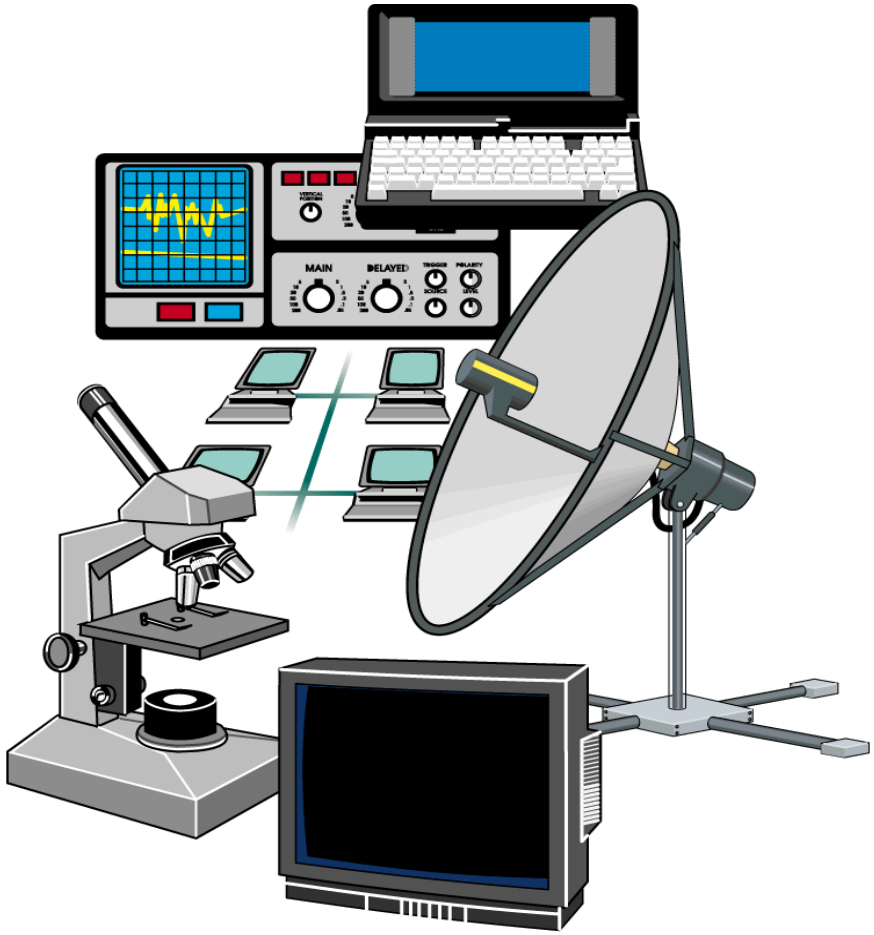
Where Programmable Logic Fits into Engineering Curriculums

- Engineering Labs
- Research Projects
- Senior Design Projects
- Design Contests



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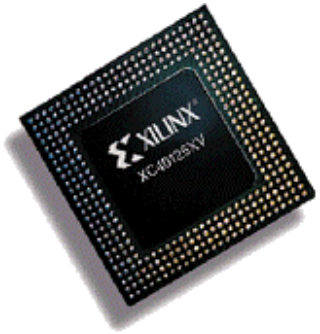
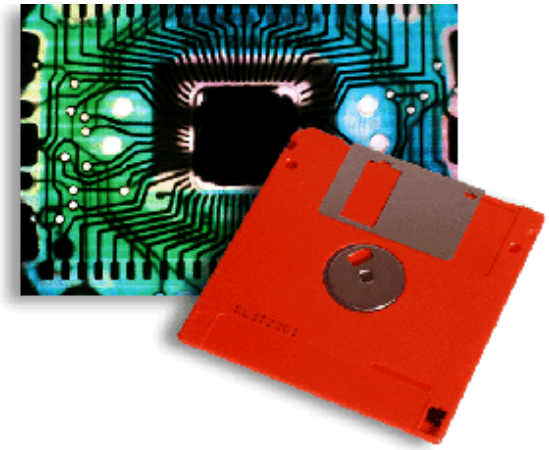
How Universities Use Programmable Logic

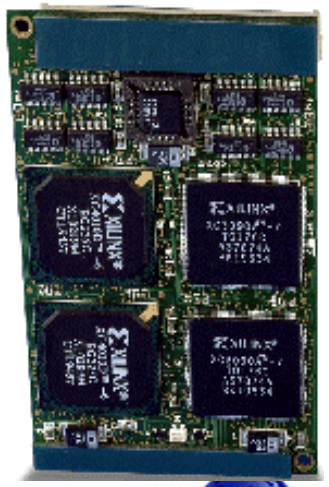
1) Professor assigns application (Project, Lab Assignment, etc.)





2) Student creates application with Xilinx Software Tools

3) When Application Is Final, Student implements design in hardware



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Why Universities Turn to Xilinx

- Can be used in various engineering labs
  - Digital Design
  - Intro/Advanced Digital Design
  - Computer Architecture
  - Networking and Communications
  - Control Systems
- Projects and Labs can focus on concept, not wire wrapping
- Complete Software Package for Design, Synthesis, Implementation and download
- Immediate results in hardware
- Xilinx Design Series of Books from Prentice Hall
- Free XUP Professor's Workshops available worldwide
- Xilinx University Resource Center

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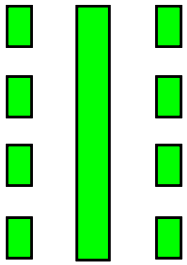
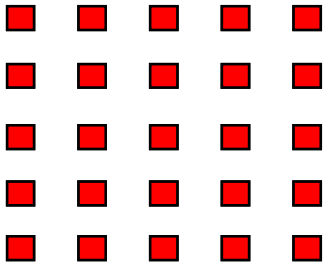
Xilinx Products

CPLDs and FPGAs

	Complex Programmable Logic Device (CPLD)	Field-Programmable Gate Array (FPGA)
		
Architecture	PAL/22V10-like More Combinational	Gate array-like More Registers + RAM
Density	Low-to-medium 0.5-10K logic gates	Medium-to-high 1K to 3.2M system gates
Performance	Predictable timing Up to 250 MHz today	Application dependent Up to 200 MHz today
Interconnect	“Crossbar Switch”	Incremental

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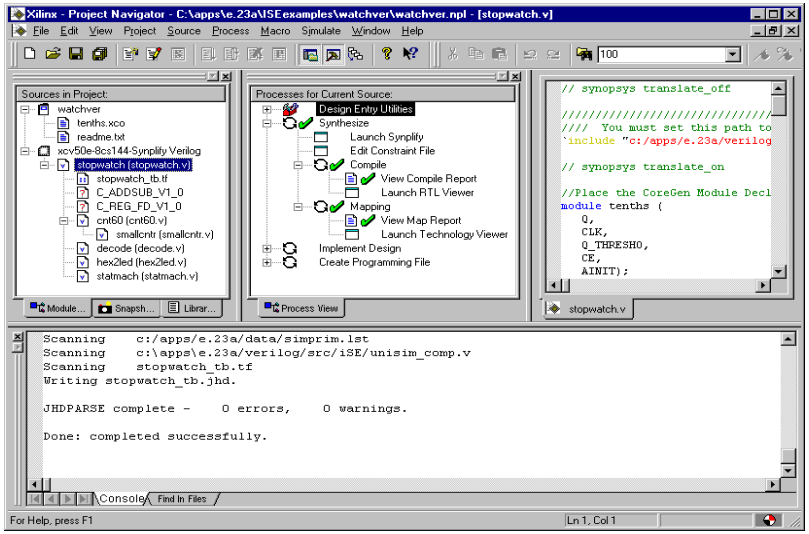
Xilinx Products

Design Tools

V5.1i ISE Software

- Complete Software Package
  - Design Entry (Schematic, VHDL, Verilog)
  - Synthesis (XST)
  - Implementation (Translate, Map, Place & Route)
  - Simulation (ModelsimXE-II)
  - iMPACT Programmer (Download Bistream)
- CORE Generator
  - Parameterizable Cores
- StateCAD/State Bencher
  - State Machine Design
- HDL Bencher
  - Test Bench Generation

- Unix & PC Platforms



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5.1i Device Support

all Xilinx leading FPGA/CPLD families

- New leading-edge device families

- ISE advantages can be leveraged across various Engineering courses
  - Across all device families and design sizes

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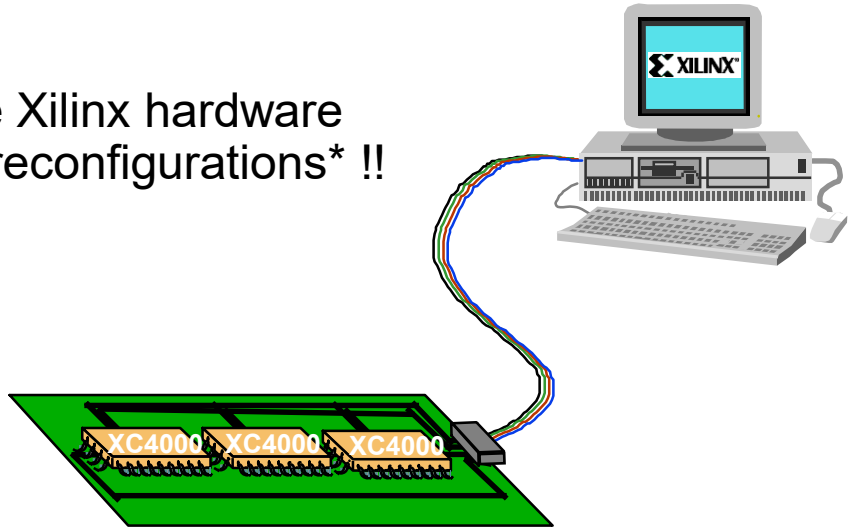
Programmable Logic Design Flow

1. **Design Entry** in schematic, ABEL, VHDL, and/or Verilog.

2. **Implementation** includes Placement & Routing and bitstream generation using Xilinx's M1 Technology. Also, analyze timing, view layout, and more.

3. **Download** directly to the Xilinx hardware device(s) with unlimited reconfigurations* !!



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Xilinx Programmable Logic in your Curriculum

Family	Density	Digital Design	Adv Digital	Embedded Processing	Computer Architecture	DSP	SOC
XC9500	36-288 MacroCells	X					
CoolRunner	32-512 MacroCells	X					
Spartan-IIE	Up to 300K System Gates	X	X	X			
Virtex-E	58K to 4M System Gates		X	X	X		
Virtex-II	40K to 8M System Gates + up to 168 Multier Blocks		X	X	X	X	
Virtex-II Pro	Virtex-II + Up to 4 PPC Processors and 24 Rocket I/O Transceivers			X	X	X	X

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