

<p style="text-align: center;"><b>國立中興大學 電機工程研究所</b> <b>超大型積體電路訊號處理架構 課程簡介 (2022, Spring)</b></p>
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一、授課老師 黃穎聰

e-mail : hwangyt@ dragon.nchu.edu.tw

二、上課時間

- Tuesday                      09:10AM~12:00PM                      EE102

三、課程內容介紹

This course is designed to give you a comprehensive coverage of the VLSI architectures for digital signal processing. The main theme of the course is to design efficient VLSI architectures for computing algorithms frequently encountered in DSP systems. In other words, this course will teach you how to map DSP algorithms onto VLSI. You will learn the basic properties of VLSI algorithms and their relations with the VLSI implementation. You will also learn a lot of algorithm transformation and architecture design techniques to improve your design. A systematic introduction to this design process will be elaborated. Fundamental knowledge toward DSP, computer architecture and parallel processing is preferred but not a prerequisite. The detailed contents of this course include

- introduction to VLSI digital signal processing
- review of DSP algorithms
- algorithm representations and iteration bound
- mapping algorithms onto array structures
- QR factorization design example
- retiming
- unfolding
- folding
- pipelining and parallel processing for low power
- pipelined and parallel recursive and adaptive filters
- Deep learning architecture for CNN network

四、課程要求

The grading of this course is based on homeworks, exam and term project. There are two types of homeworks, that is,

- **regular** - this is the ordinary written homework, mostly from the problems of the textbook
- **simulation** - you will be asked to use Verilog to simulate and verify small design

There will be mid-term and final exams. For the term project, you will be assigned a DSP module and derive its VLSI design using the techniques learned

from the class for optimization. You should give a performance evaluation and include simulation result of your design.

## 五、評分標準

The following is only a tentative grading system

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|-----------------|-----|
| • homework      | 30% |
| • mid-term exam | 25% |
| • final exam    | 30% |
| • term project  | 15% |

## 六、教科書

- “VLSI Digital Signal Processing Systems – Design and Implementation,” by Keshab Parhi, John Wiley & Sons, 1999

## 七、上課講義

The lecture note (in .pdf format) can be downloaded from the “iLearning” system prior to each lecture. A password (socdsp826) is required to open the materials.