VLSI DSP 2022 期末考試題型提示

Part A 簡答題

A1. What is a node delay transfer function?

A2. L-slow delay in block processing of size L

A3. How would the number of delays in a DFG change if unfolding with a factor of 2 is applied?

A4. What is time scaling?

A5. For a DFG loop contains 6 delays in it, how many loops are there in the unfolded DFG with an unfolding factor J=2?

A6. What is the retiming result if the following node delay transfers are applied to the DFG shown in Fig. 1?

r(1) = 1, r(2) = 1, r(3) = 0, r(4) = -1

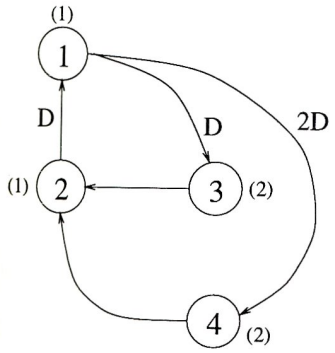

Fig 1

A7. Lifetime of a variable

A8. What is the difference between clustered and scattered look ahead transform

Part B. 計算與設計題

B1. Given a circuit, apply pipelining or parallel processing to achieve low power, calculate the voltage scaling factor and the power saving

B2. Given a DFG (with or without switches), derive its unfolded design

B3. For a DFG, verify if given folding sets are correct not by checking folding equations. If incorrect, apply retiming to achieve a valid design

B4. Given a lifetime table, assume the iteration period is 3

- **a)** Please derive its circular life time chart
- **b)** Determine the minimal number of registers needed for allocation
- **c)** Perform data allocation using forward-backward register allocation

B5. Consider a transfer function H(z), please derive its clustered and scattered look ahead designs for pipeline stage M = 3.