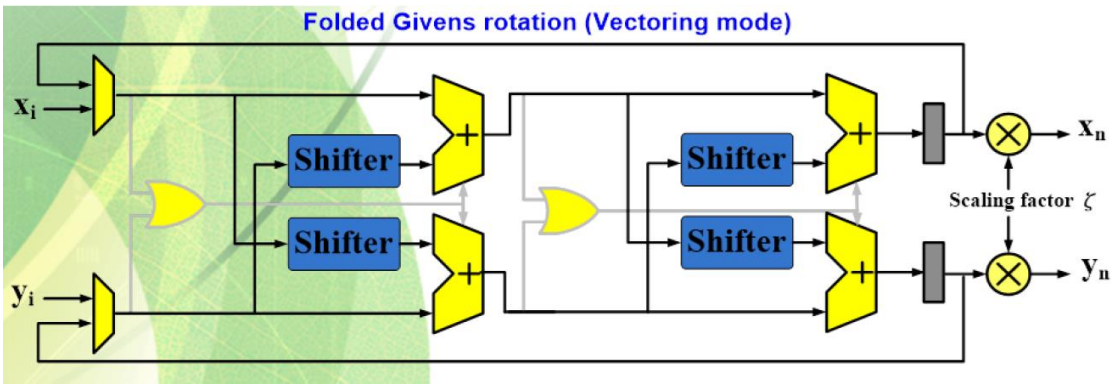
▪ Architecture design



一個 clk 做兩個 micro rotation；

一個 module(vector mode、rotation mode)做 8 次 micro rotation(4 clk)；

Synthesized report：如附檔

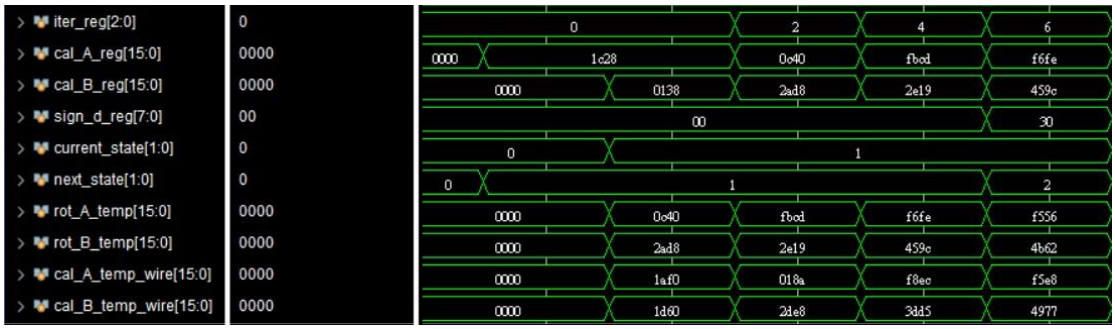
cell area: 47608.676336

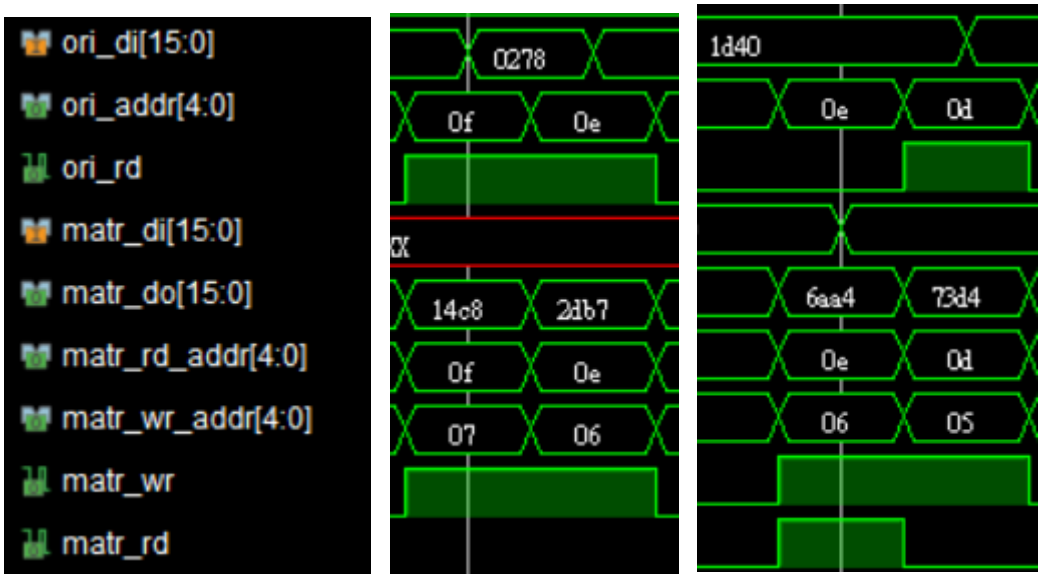
slack:2.24

▪ Memory configuration

Memory configuration : 13 * 32 rom × 1；13*32ram × 1；

▪ Simulation waveform





▪ Word length, iteration number, δ

Word length：13 bit(sign:1;decimal:2;fraction:10)

Iteration number：8

δ = 0.0049

▪ Number of clock cycle

Clk period：20ns；

Clk cycle：500；

▪ Hardware complexity

Shifter： 2 ；

Adder： 2 (for shif and adder)、 2 (for counter) {vector mode、rotation mode 各 1 份}

4(for counter) {QR top module}

Multiplier：2{vector mode、rotation mode 各 1 份}