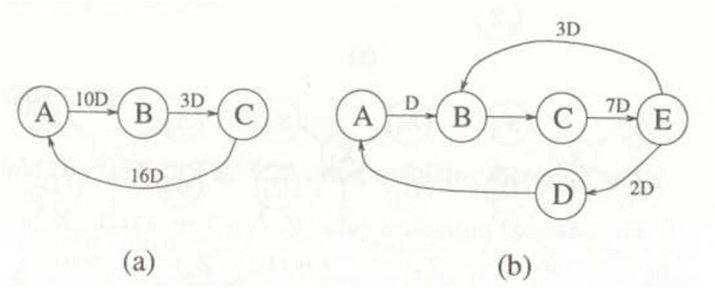
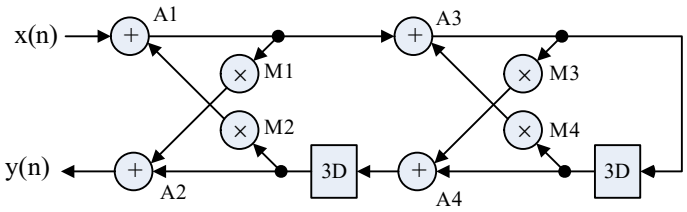
2021 Spring VLSI DSP Homework Assignment #3

Due date: 2021/6/14

Q1. Unfold the DFG shown below using unfolding factors 2 and 3



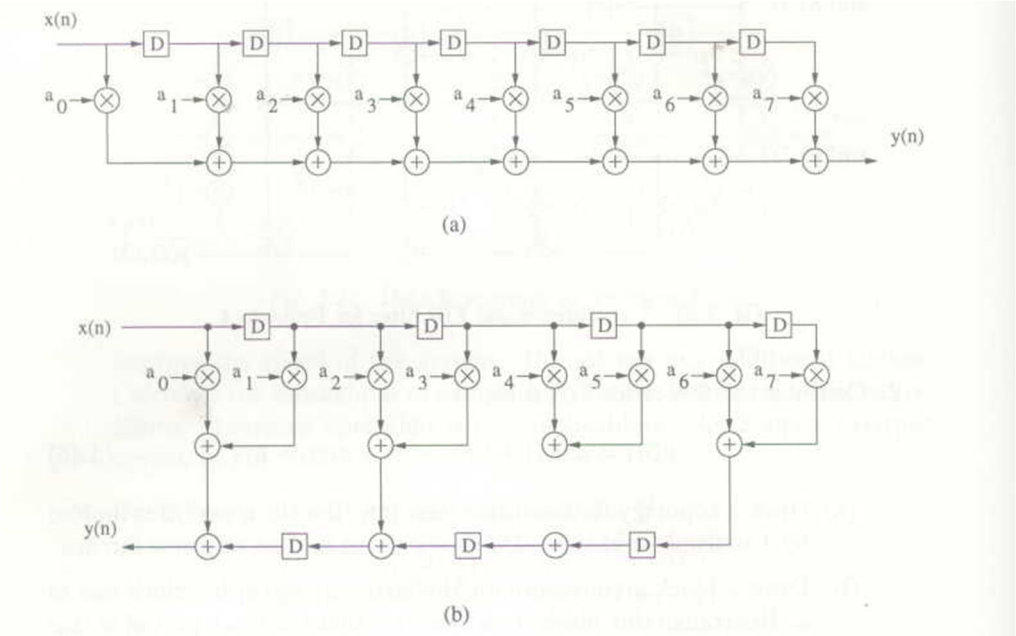
Q2. For the DFG shown below, assume the computing times of multiplier and adder are 3 u.t and 1 u.t., respectively. Unfold the design by a factor of 2 and apply retiming to achieve a critical path delay of 6 u.t..



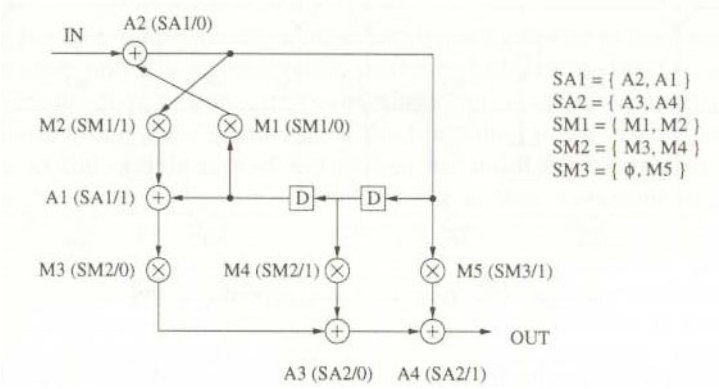
Q3. For the two implementations of an 8-tap FIR filter below, assume the propagation delay of a multiplier is twice that of an adder, i.e. $T_m = 2T_a$. Also assume the capacitance of a multiplier is 10 times that of an adder, i.e. $C_m = 10\ C_a$. Design (a) is the original design version operating with $V_{dd} = 4V$, $V_{th} = 0.5V$, and clock cycle $Ts = T_m + 7T_a$ (the critical path delay). Design (b) is the low power version design operating at the same speed but with a lower V_{dd}. Note that the value of V_{dd} should not be lower than 1.2V for an acceptable noise margin.

a) Please calculate the V_{dd} scaling factor β

b) Please calculate the % of power saving compared with the original design



Q4. For the design shown below.



a) For a folded design with 5 folding sets (SA1, SA2, SM1, SM2, SM3) and a folding factor equal to 2, verify if this is a valid folding

b) If it is not, find a new valid folding design by modifying the folding orders in each set and/or applying retiming.

c) Derive your folded design by using the forward backward register allocation scheme to minimize the register usage. **Note:** you need to show the derivation details, e.g. life time chart, register allocation table, and so on.

d) Write corresponding Verilog design and conduct Verilog simulation to verify the correctness of your folded design. Assume inputs are 8-bit wide signed integers. Multiplier coefficients are all 8-bit wide and have magnitudes between 0.5 and 1. You may determine the word length of other variables so that no overflow occurs.