

# Introduction to SOC design

Ch. 1

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「超大型積體電路與系統設計」教育改進計畫  
SOC聯盟編製

SOC 聯盟計畫



# Outline

## 1. Introduction to SOC

1. Semiconductor Market
2. What is SOC?
3. Why Do We Need SOC ? (Advantage)
4. A Typical SOC Design Example
5. Current Status of SOC

## 2. Design methodologies and trends for SOC

1. SOC design flow and Tools
2. Platforms Based SOC Design
3. Hardware & Software Co-design/ Co-simulation/ Co-Emulation and Prototyping
4. Embedded RTOS
5. Mixed Mode Design
6. SOC Design Tasks
7. IP reuse
8. The Trends of SOC

## 3. System integration issues for SOC

1. Establish a Complete SOC Development Infrastructure
2. System Integration Issues in Physical Design
3. System Integration Issues in Synthesis
4. System Integration Issues in System-Level Designs
5. IP Related Issues
6. System Integration Issues in Testing & Verification
7. Integration-Centric Approach

## 4. Conclusions



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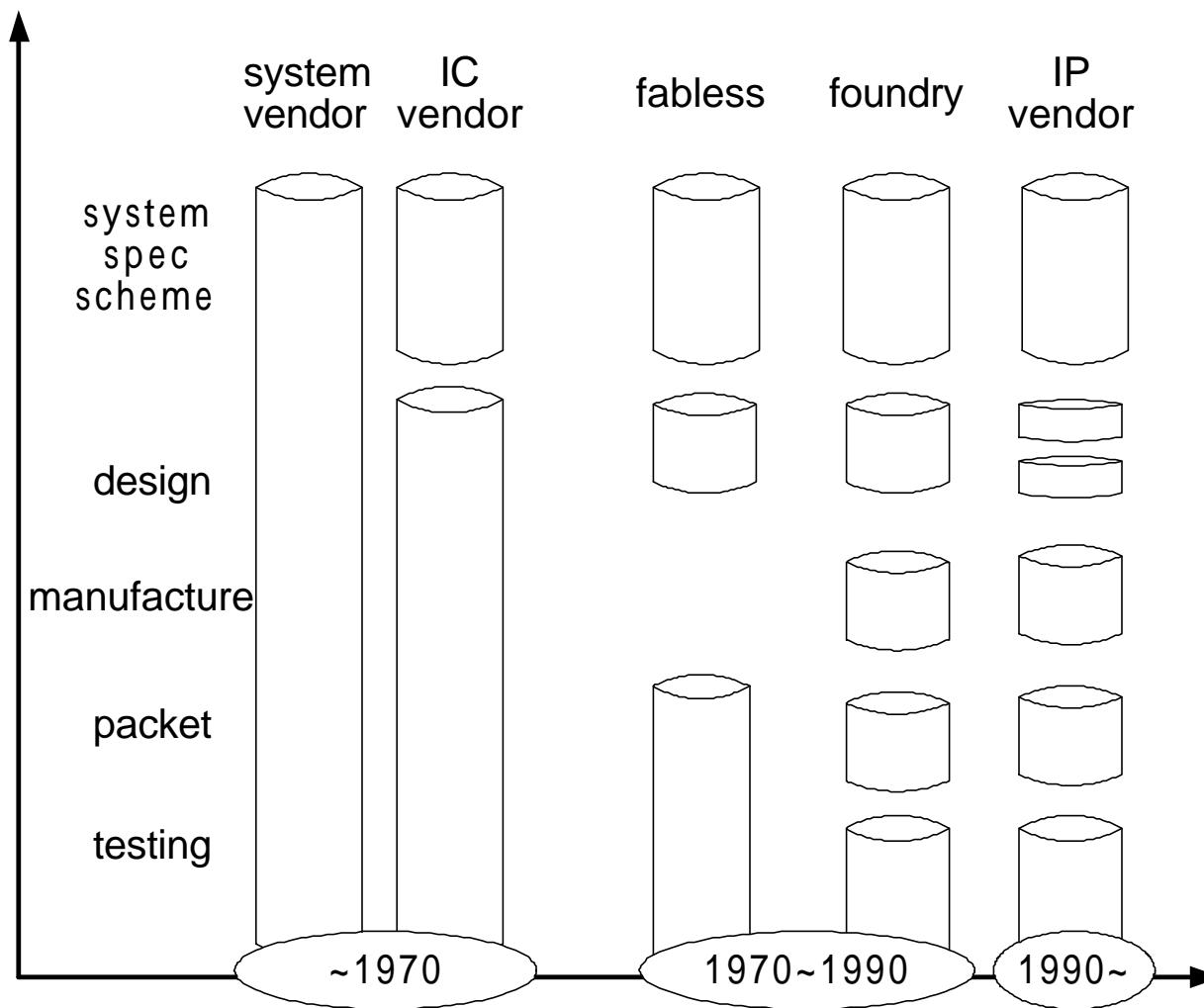


# Semiconductor Market

- ◆ Revolution 1 : Element Standardization
  - 1960~1970 , the computer system vendor supplied all the software/hardware component.
  - 1970 , IC is invented , the process is dived into system integration and IC provider.
- ◆ Revolution 2 : ASIC
  - 1980~1990 , the efficiency and timing are not enough for the speed requirements , the ASIC is coming up!!
- ◆ Revolution 3 : SIP
  - For the Time-to-market , the concept of SIP is provided.
  - The IP design companies appear.



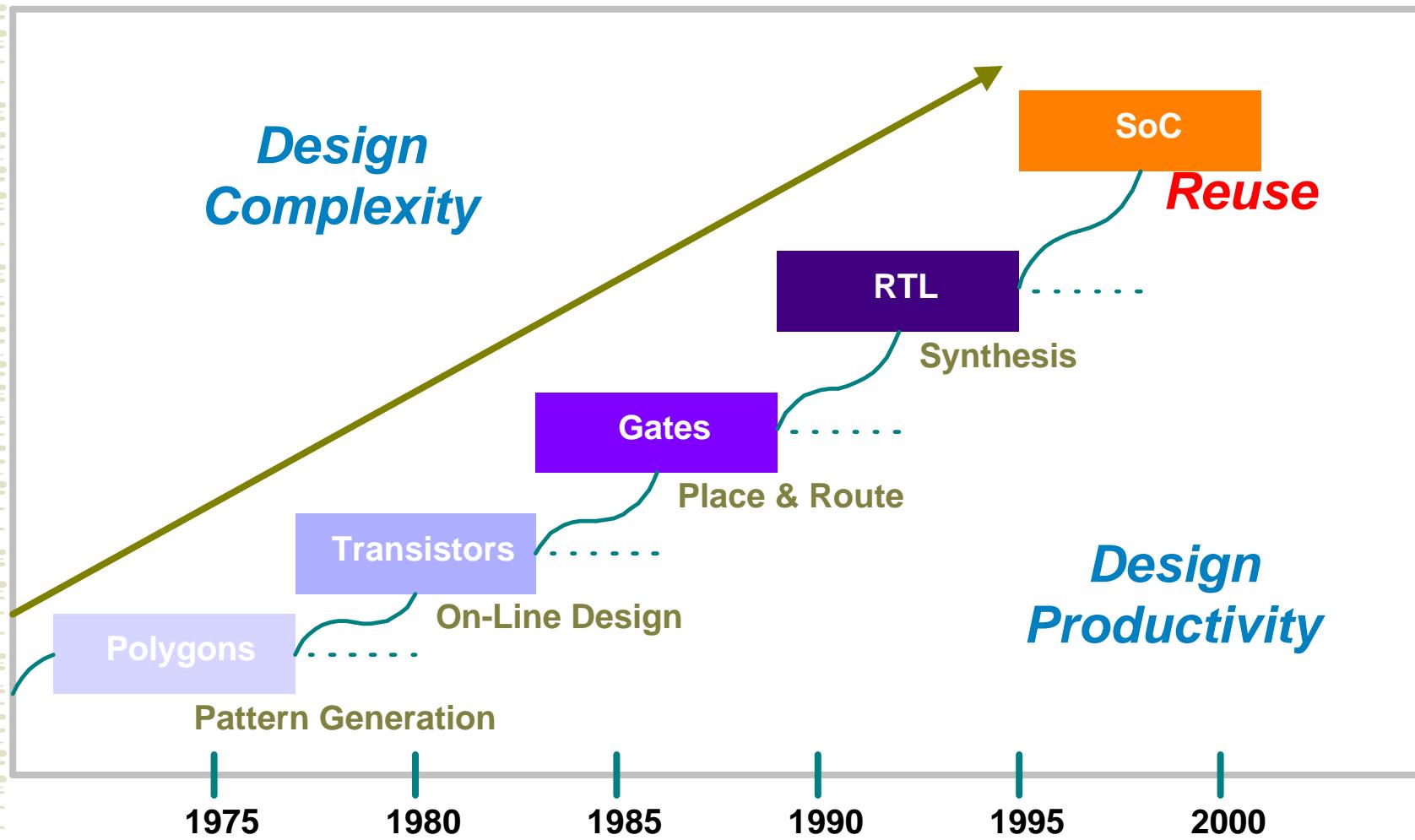
# Semiconductor Market (2)





# 1. Semiconductor Market (3)

## Trends of VLSI Design





# 1. Semiconductor Market (4)

## General Technology Trends

Table 1

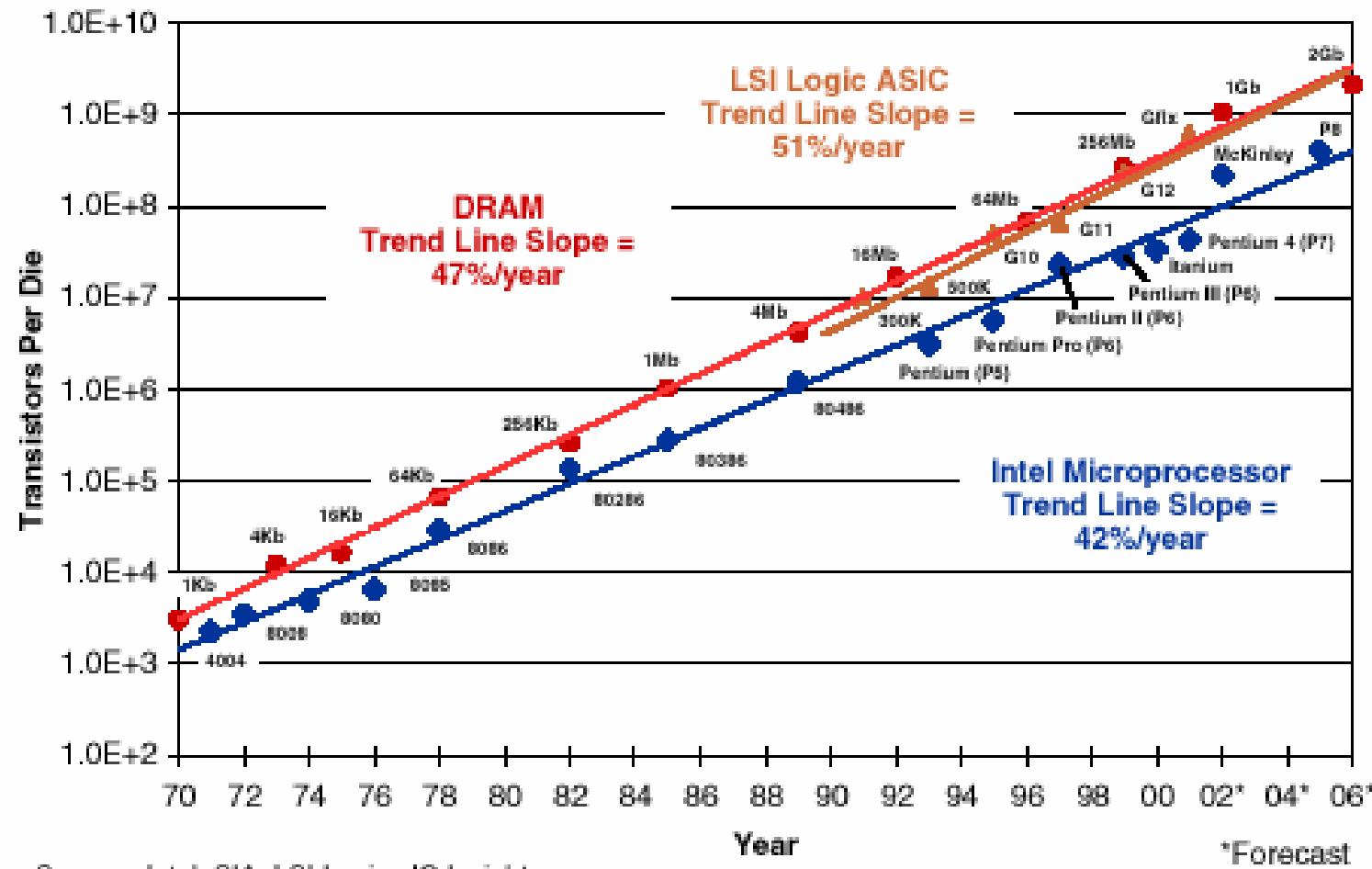
### General Technology Trends (from SIA Roadmap)

Year	1999	2001	2003	2006	2009
Min Feature Size ( $\mu\text{m}$ )	0.18	0.15	0.13	0.10	0.07
Gate Count (M)	5	10	19	50	130
Total Net Length (km)	1.48	2.16	2.84	5.14	10
# Metal Layers	6	7	7	7-8	8-9
Metal Aspect Ratio	1.8	2.0	2.2	2.4	2.7
Metal Resistivity (microOhm-cm)	3.3	2.2	2.2	2.2	<1.8
ILD Constant	>3.0	2.5-3.5	2.0-2.5	1.5-2.0	<1.5



# 1. Semiconductor Market (5)

## IC Transistor Count Trends

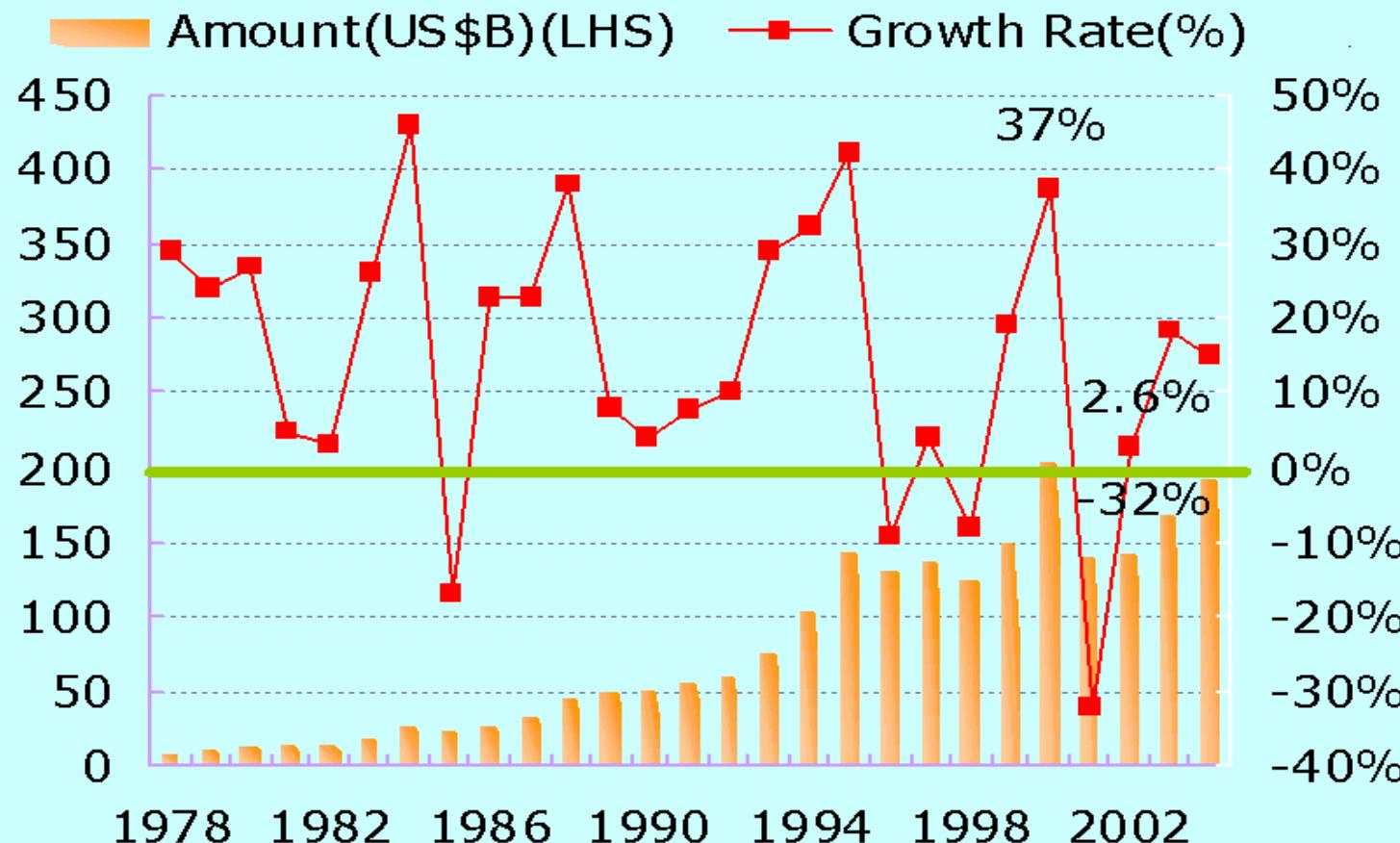




# 1. Semiconductor Market (6)

## Semiconductor Market

### WW Semiconductor Cycles



Data Source: WSTS 2002



# 1. Semiconductor Market (7)

**Popular Semiconductor Application**

Unit: M USD

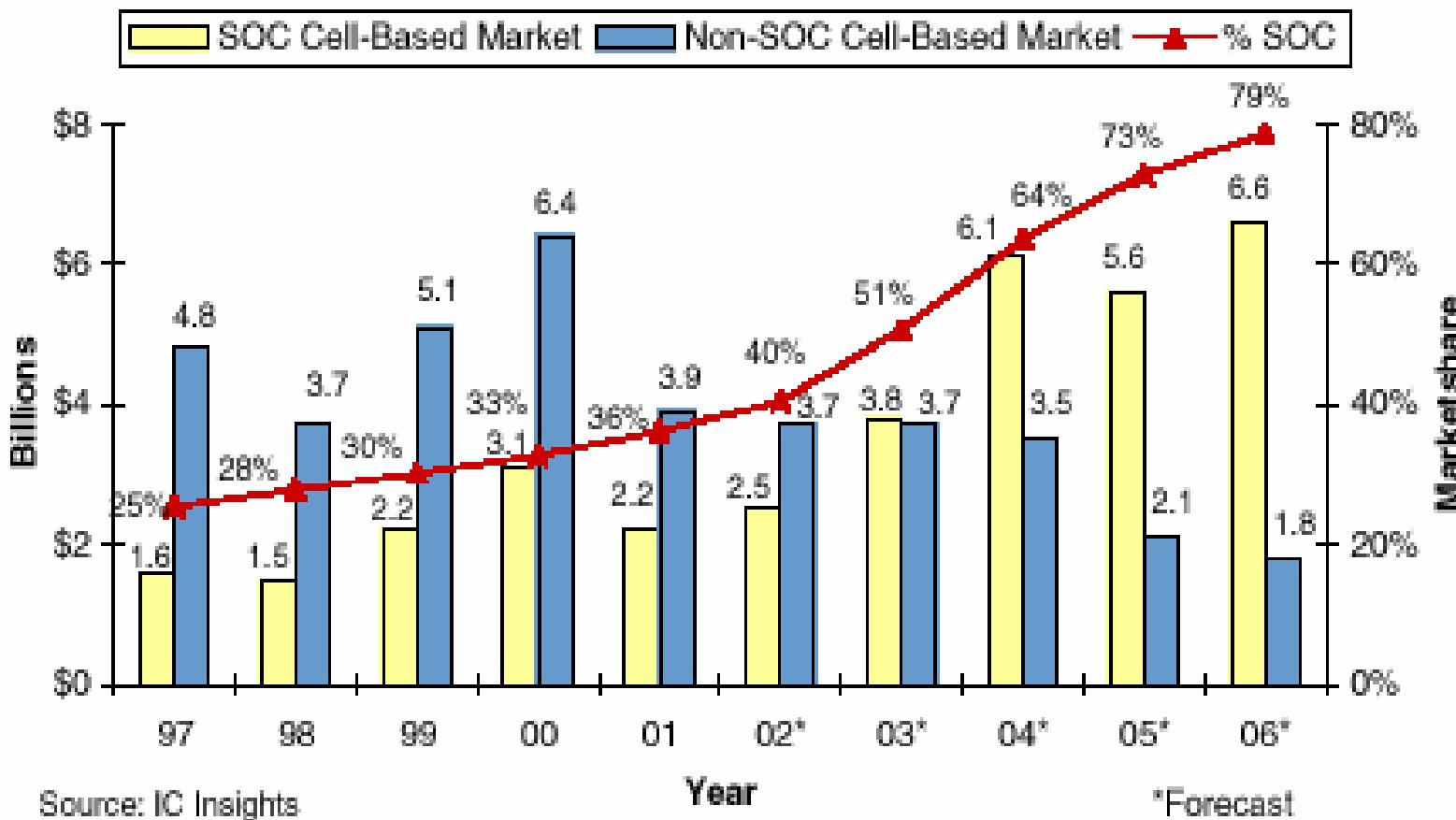


Product	2001 Market Size	2005 Market Size	CAGR (%) 01'-05'
Wireless Broadband Access	19	96	49.9%
Digital TV	373	1,671	45.4%
Internet Audio Player	234	659	29.5%
Digital Camcorder	1,401	3,705	27.5%
DVDs	1,700	4,072	24.4%
Digital Cellular	15,457	35,362	23.0%
LAN Switches	2,609	5,925	22.8%
Digital STB	2,197	4,572	20.1%
Other Portable Stereos	227	416	16.4%
Video Game Controller	3,983	6,625	13.6%
xDSL CPE	773	1,274	13.3%
Digital Still Cameras	3,103	4,513	9.8%

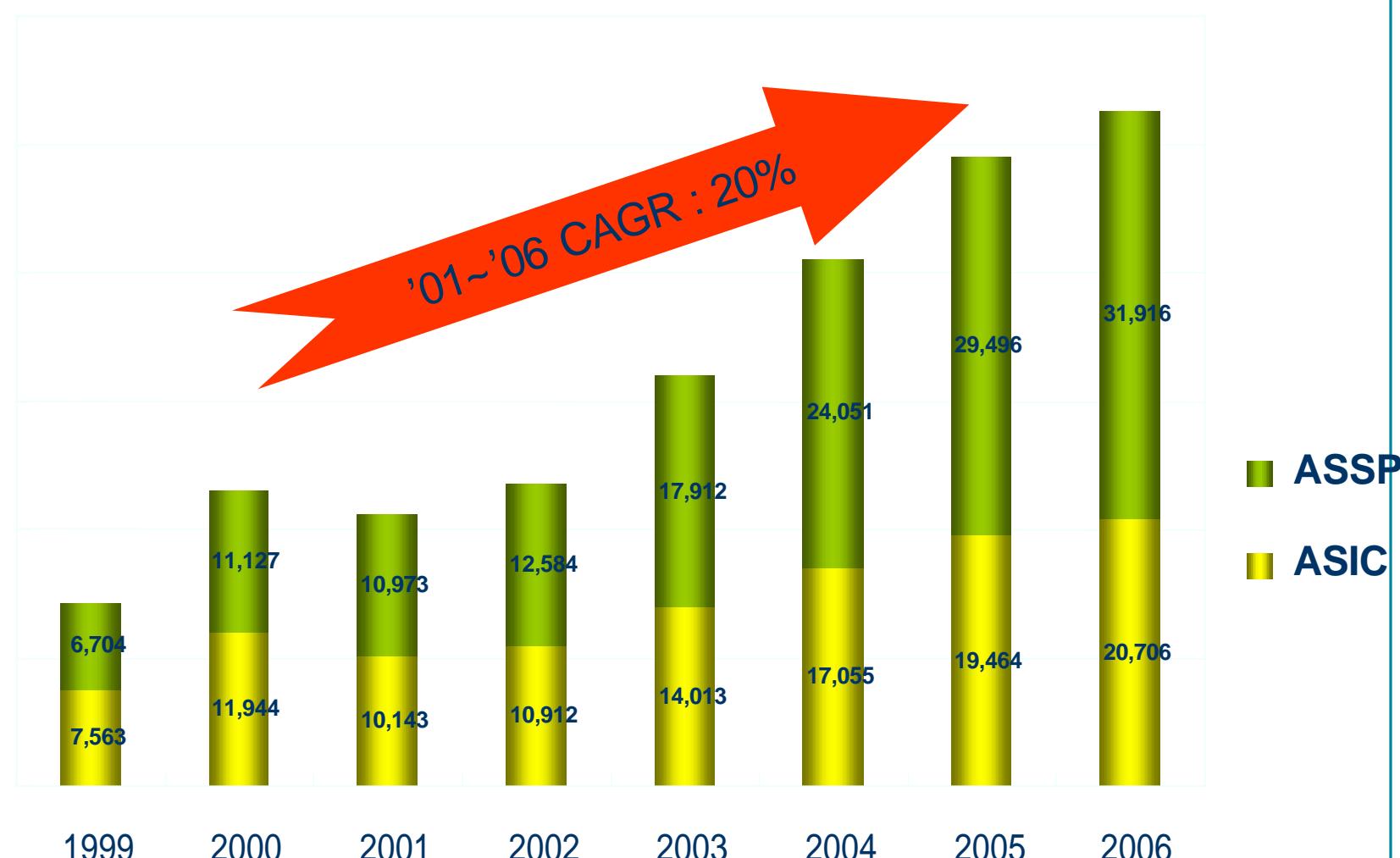


# 1. Semiconductor Market (8)

## SOC Cell-Based IC Market (1997-2006)



# 1. Semiconductor Market (9)



Source: Gartner Dataquest(May 2002)

ASSP---Application -Specific Standard Product

CAGR---Compounded Annual Growth Rate

成功大學電機系 王駿發



# 1. Semiconductor Market (10)

## Successful SOC Products

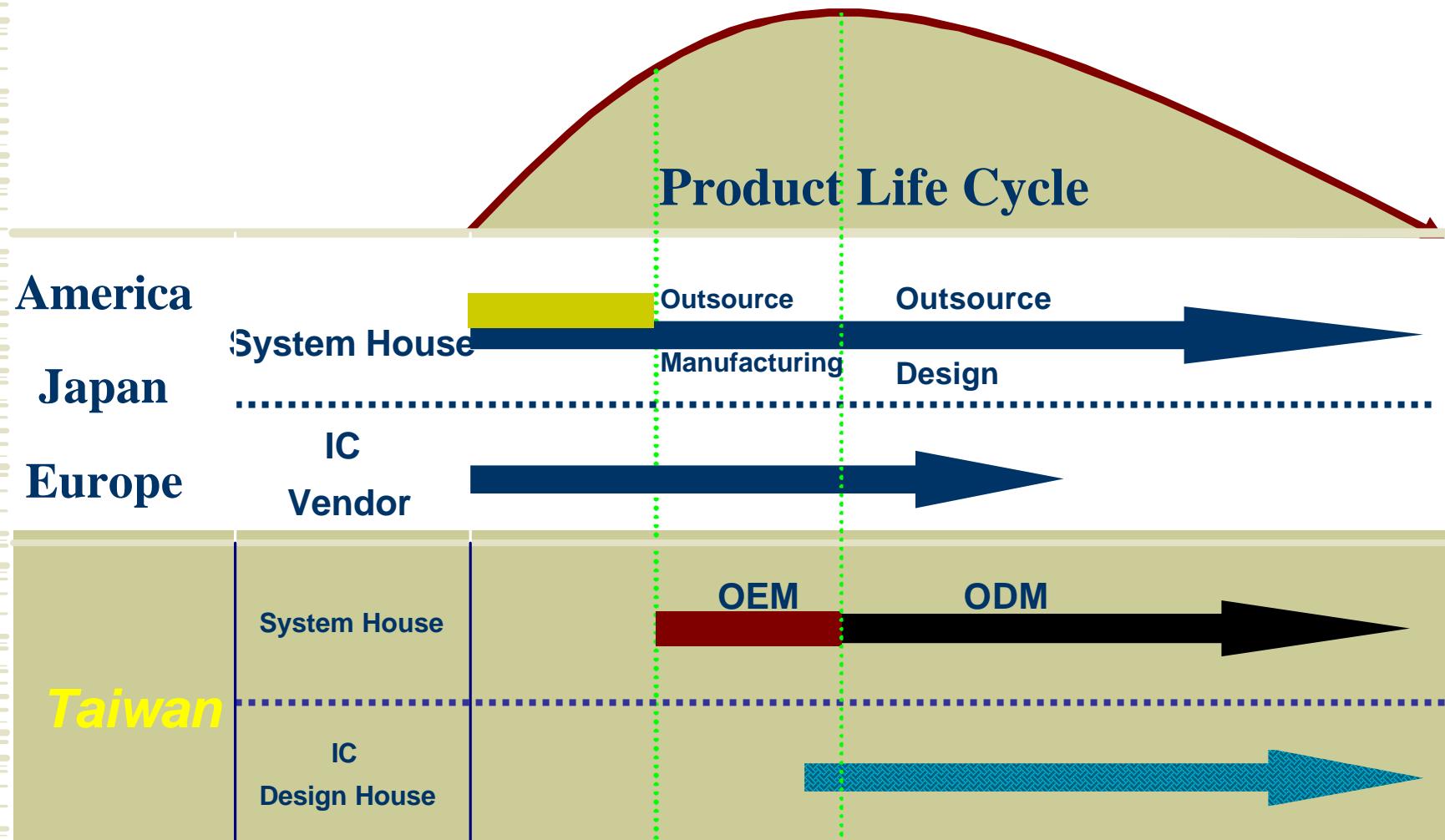




# 1. Semiconductor Market (11)

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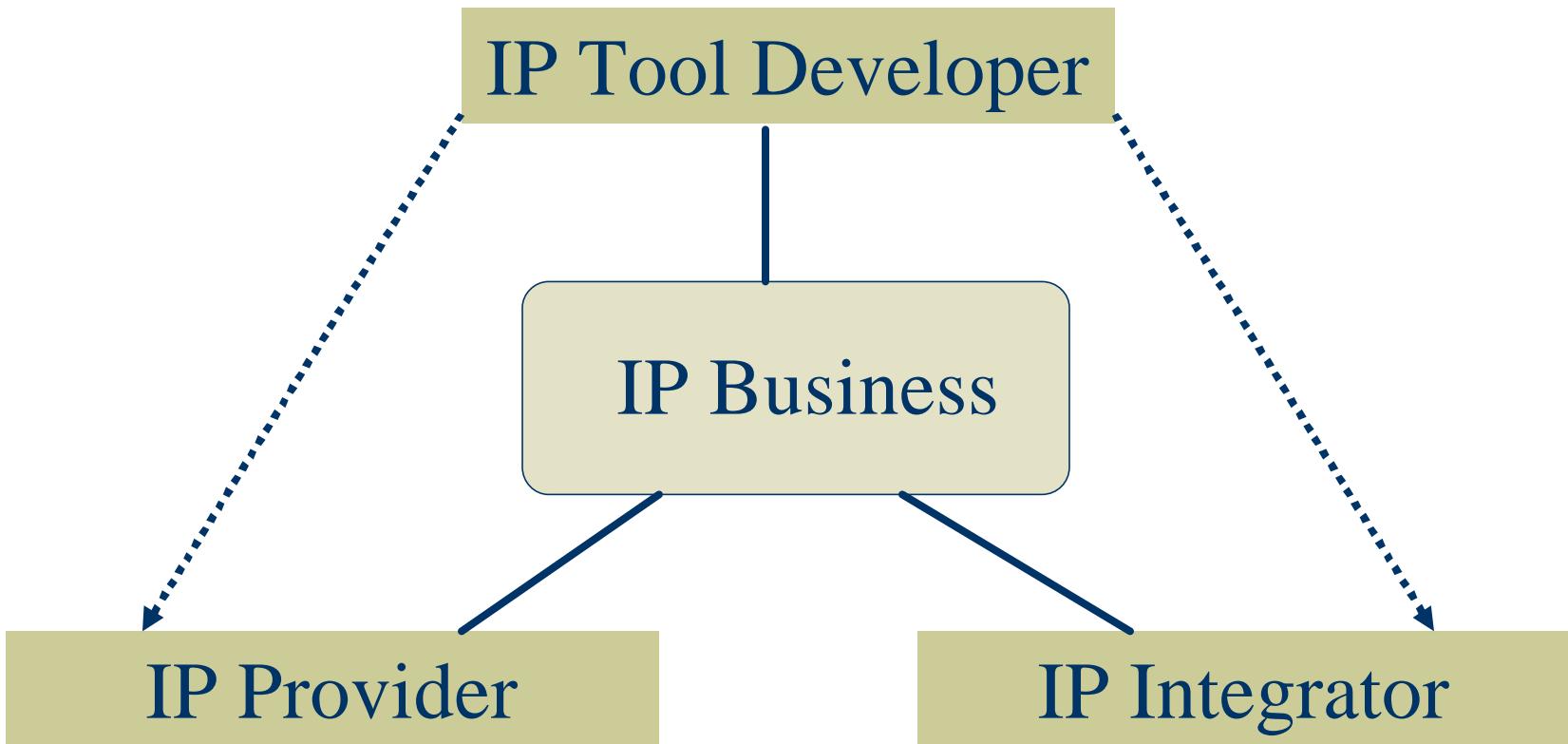
## Taiwan's Unique IC Development Model





# 1. Semiconductor Market (12)

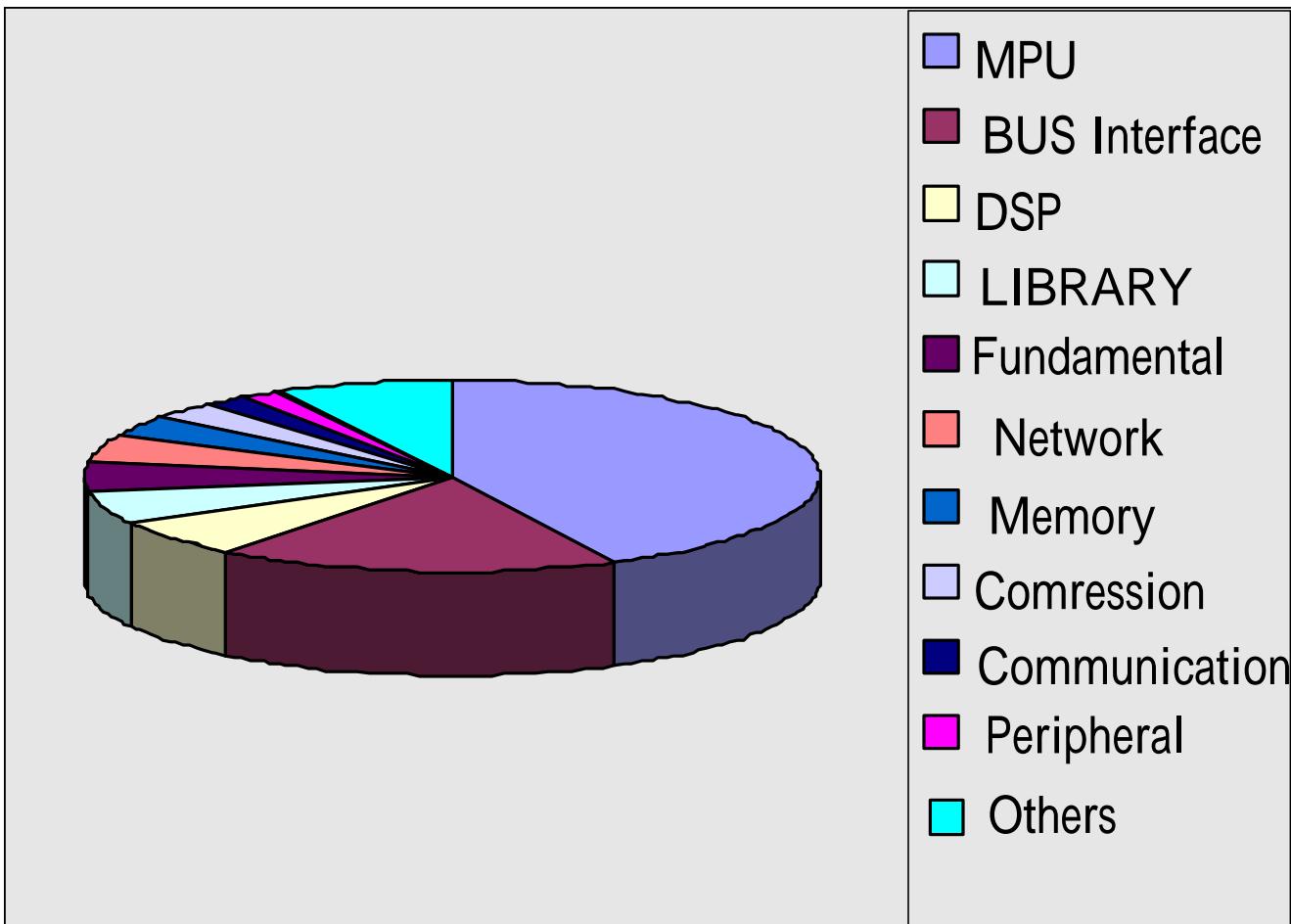
## IP Business Model





# 1. Semiconductor Market (13)

## The IP SCOPR of 2001





# 1. Semiconductor Market (14)

## The outstanding IP providers in the world

排名	公司	2001營收 (\$M)	2000 营收(\$M)	年成長率 (%)	主要領域
1	ARM	179.0	130.1	37.6	Microprocessor
2	Rambus	107.3	95.1	12.8	Bus Interface(Memory)
3	MIPS	70.2	88.5	-20.7	Microprocessor
4	Synopsys	45.0	33.8	33.0	Design Libraries etc.
5	TTP Communications	34.9	24.1	44.9	Networking(ex:Bluetooth)
6	Virage Logic	34.8	22.8	53.0	SRAM
7	Mentor Graphics	30.5	34.1	-10.4	Bus Interface/Networking Design Libraries etc.
8	Parthus	30.0	16.1	86.8	Communication Platform IP(ex: Bluetooth)
9	Artisan	27.8	20.8	33.5	Cell Libraries(ex: Memory)
10	DSP Group	26.6	25.1	6.0	DSP
11	Tensilica	21.1	10.3	104.9	Microprocessor
12	inSilicon	19.1	26.3	-27.4	Interface Bus(ex: PCI/USB)
13	LogicVision	17.3	9.3	85.9	Embedded Test Block
14	ARC	16.2	15.0	8.0	Microprocessor
15	LEDA Systems	16.1	7.2	123.9	Analog/Mixed-signal IP
16	Tality	15.5	7.8	99.5	Bluetooth/Ethernet
17	NurLogic	15.1	12.0	25.8	Bus Interface/Physical Libraries
18	Virtual Silicon	13.7	8.2	67.1	Analog / Physical libraries
19	Monolithic System	9.5	1.4	555.2	SRAM
20	Zoran	7.8	6.8	15.0	MPEG 2/Data Transmission
	Total	891.6	713.5	25.0	



# 1. Semiconductor Market (15)

## Taiwan IP Providers

Actrans System, Inc.	(前訊系統股份有限公司)
Altera Co., Ltd.	
AVNET Asia Pte, Ltd., Taiwan Branch	(新加坡商安富利股份有限公司台灣分公司)
Faraday Technology Corp.	(智原科技)
Galaxy Far East Corp.	(茂綸股份有限公司)
Gerent Technologies, Inc.	(傑倫科技股份有限公司)
Global UniChip Corp.	(創意電子股份有限公司)
Goya Technology, Inc.	(科雅科技股份有限公司)
HwaCom Systems, Inc.	(華電聯網)
Maojet Technology Corp.	(茂積股份有限公司)
Progate Group Corp.	(巨有科技股份有限公司)
RDC Semiconductor, Inc.	(金麗半導體股份有限公司)
Sino Matrix Technology, Inc.	
SOTA Design Technology, Inc.	(方陣科技)
Terax Communication Technologies, Inc.	(源捷科技)
Xilinx	(力原通訊股份有限公司)



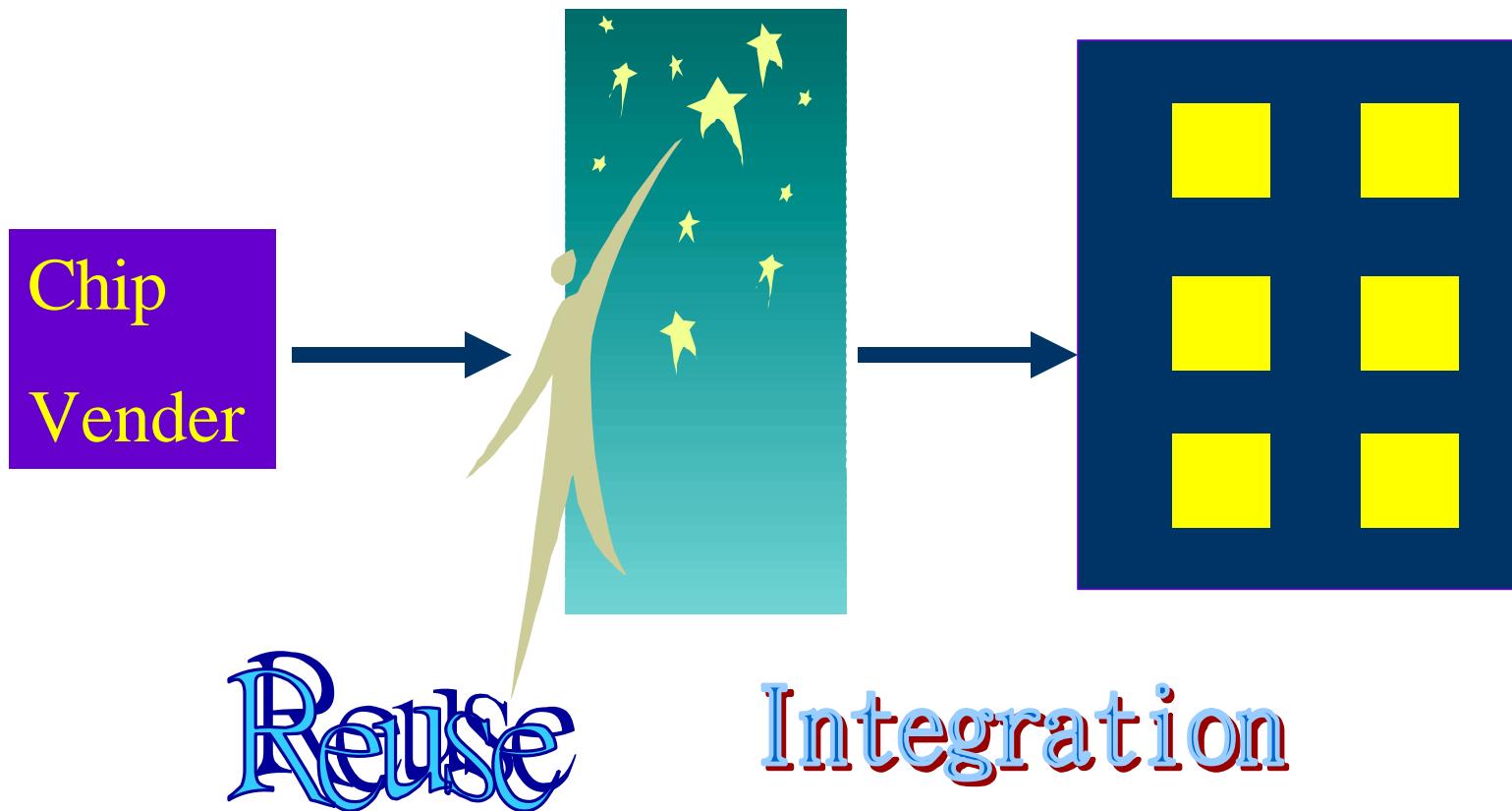
## 2 What is SOC ?

- ◆ System On-a-Chip
  - Hundreds of millions of transistors are integrated on a chip.
  - To build a system on a chip
  - Design reuse
  - Deep submicron technologies
- ◆ System LSI
- ◆ Sound of Century
- ◆ Society of Culture



## 2. What is SOC ? (2)

### Traditional System Design : System On a Board





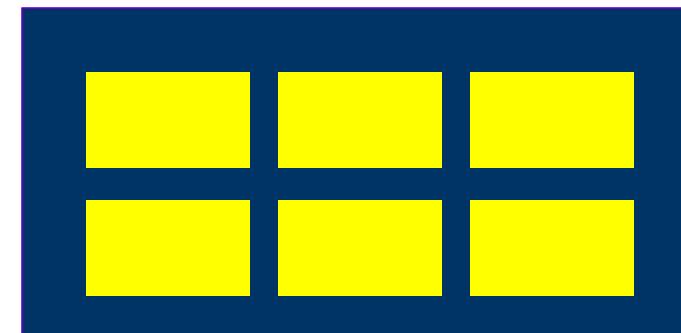
## 2. What is SOC ? (3)

System Design  
Trend

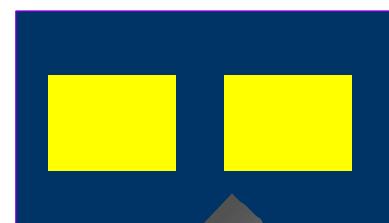
Integration



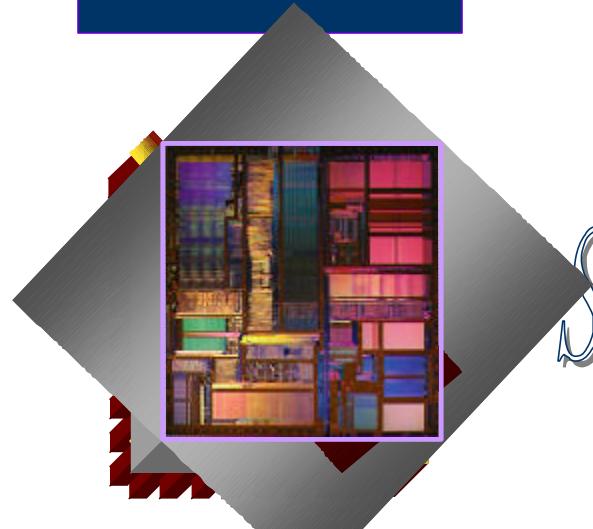
Complexity



Tens to hundreds  
of chips



Chip-set



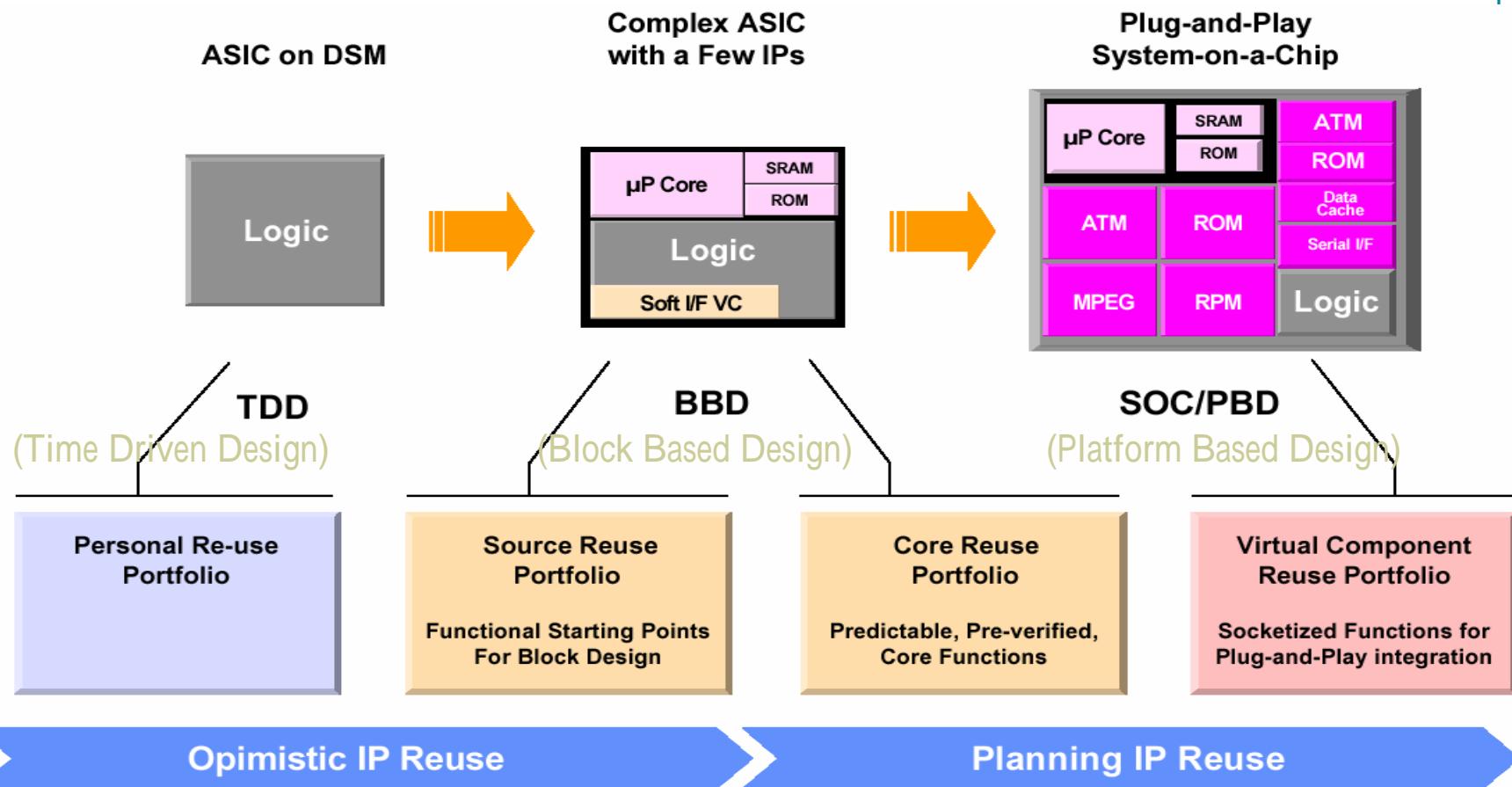
Single chip



## 2.What is SOC ? (4)

### Transition of SOC Design Methodology

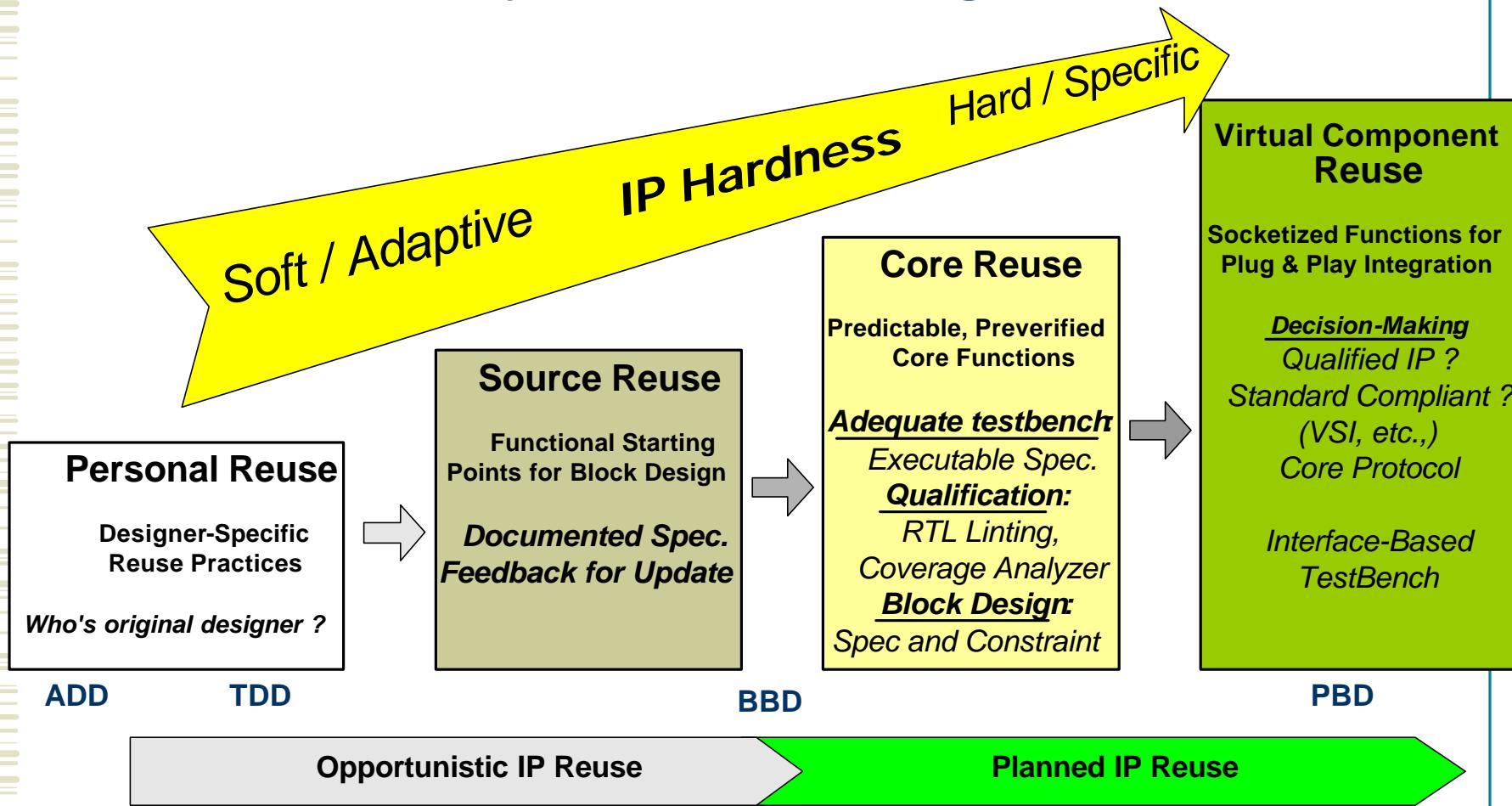
- ❖ From Area-Driven To Timing-Driven Design
- ❖ From Block-Based To Platform-Based Design





## 2.What is SOC ? (5)

### Reuse :The Key to SOC Design





## 2. What is SOC ? (6)

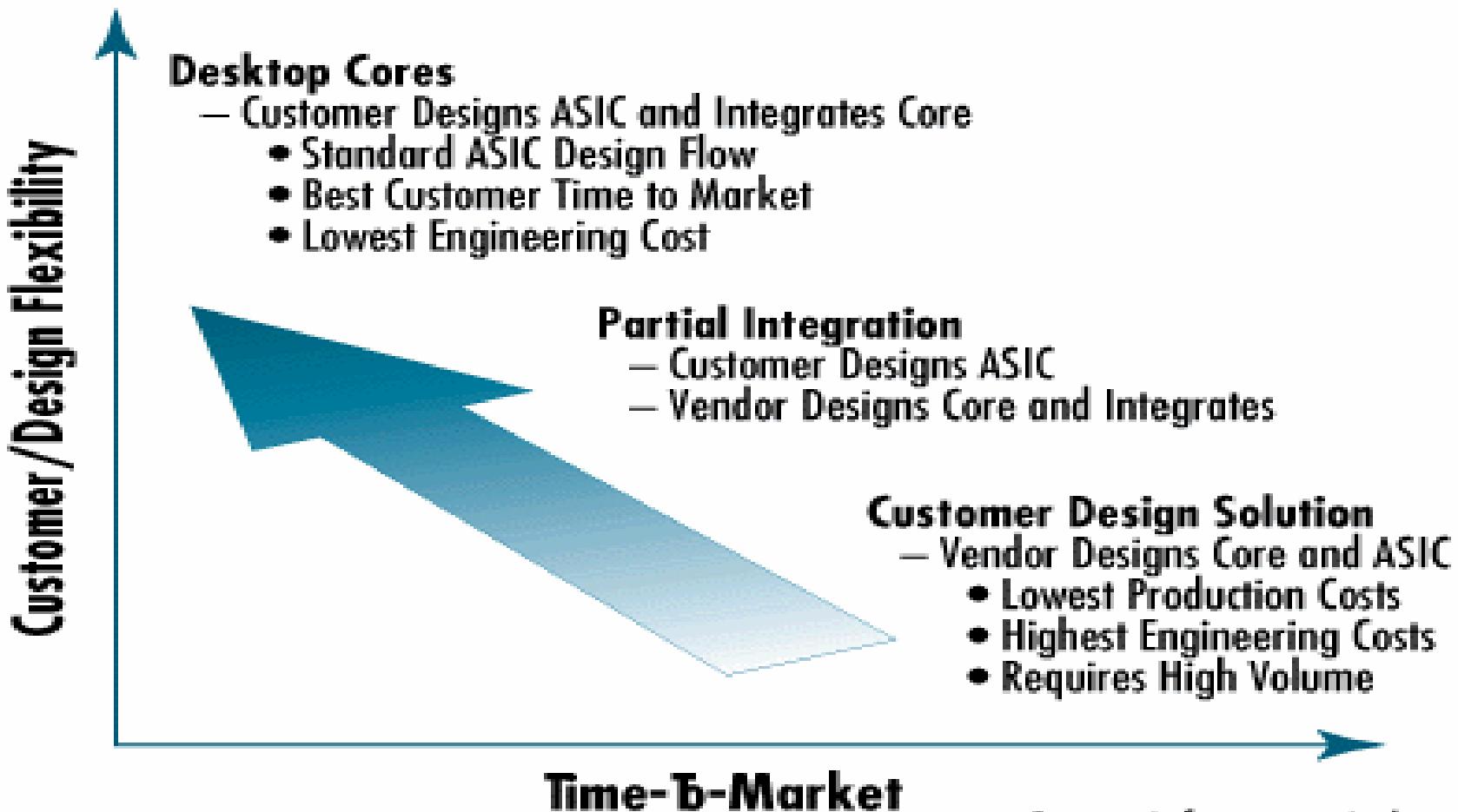
### **SOC: System On a Chip**

- **System**  
A collection of all kinds of components and/or subsystems that are appropriately interconnected to perform the specified functions for end users.
- A SoC design is a “product creation process” which
  - Starts at identifying the end-user needs
  - Ends at delivering a product with enough functional satisfaction to overcome the payment from the end-user



## 2. What is SOC ? (7)

### Types of System-on-a-Chip Designs





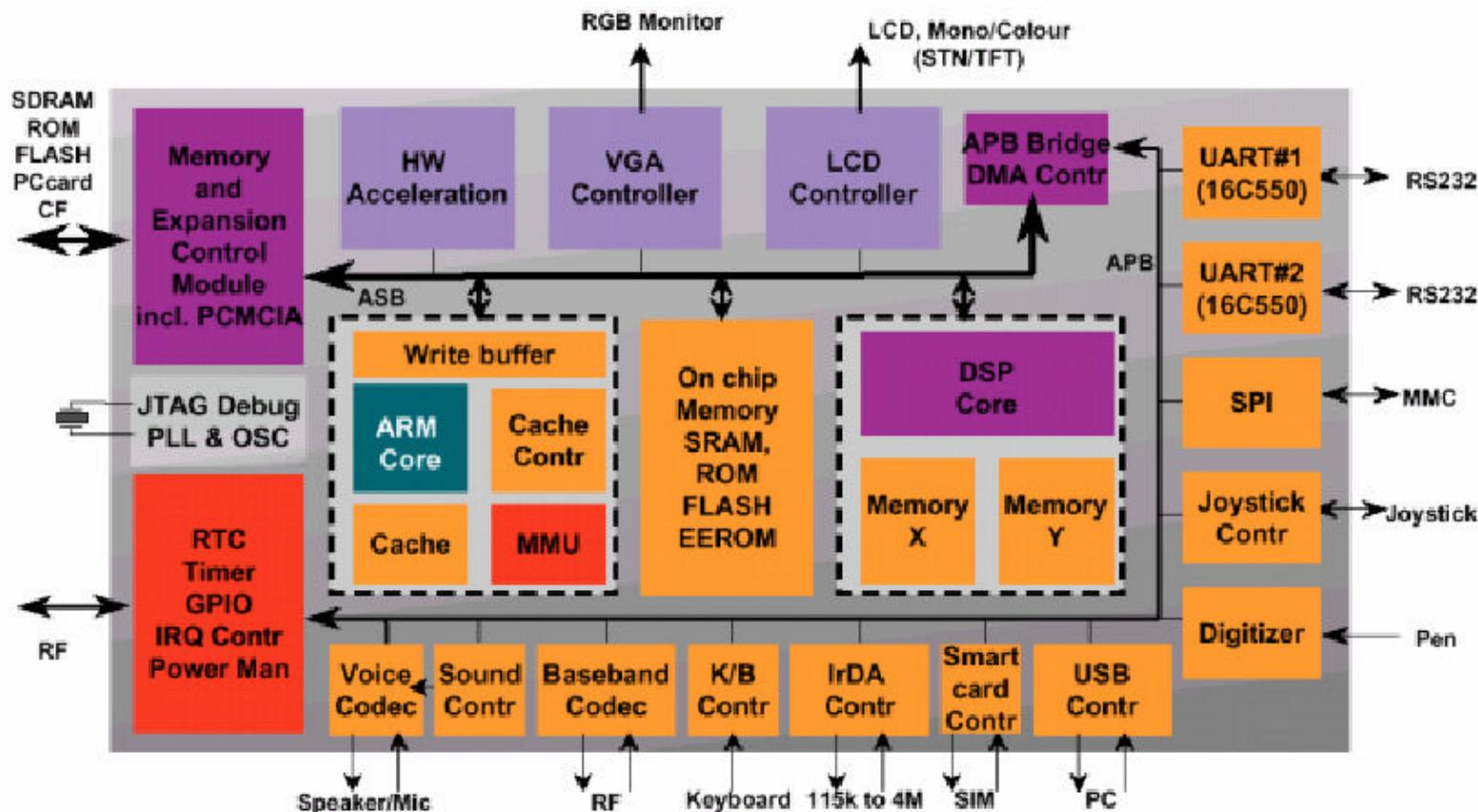
### 3. Why Do We Need SOC ? (Advantage)

- ◆ Cost
  - Low cost
- ◆ Compactness
  - Portable, hand-held
- ◆ Increase Performance
  - Quality
- ◆ Low Power Consumption
- ◆ Design reusable



## 4. A Typical SOC Design Example

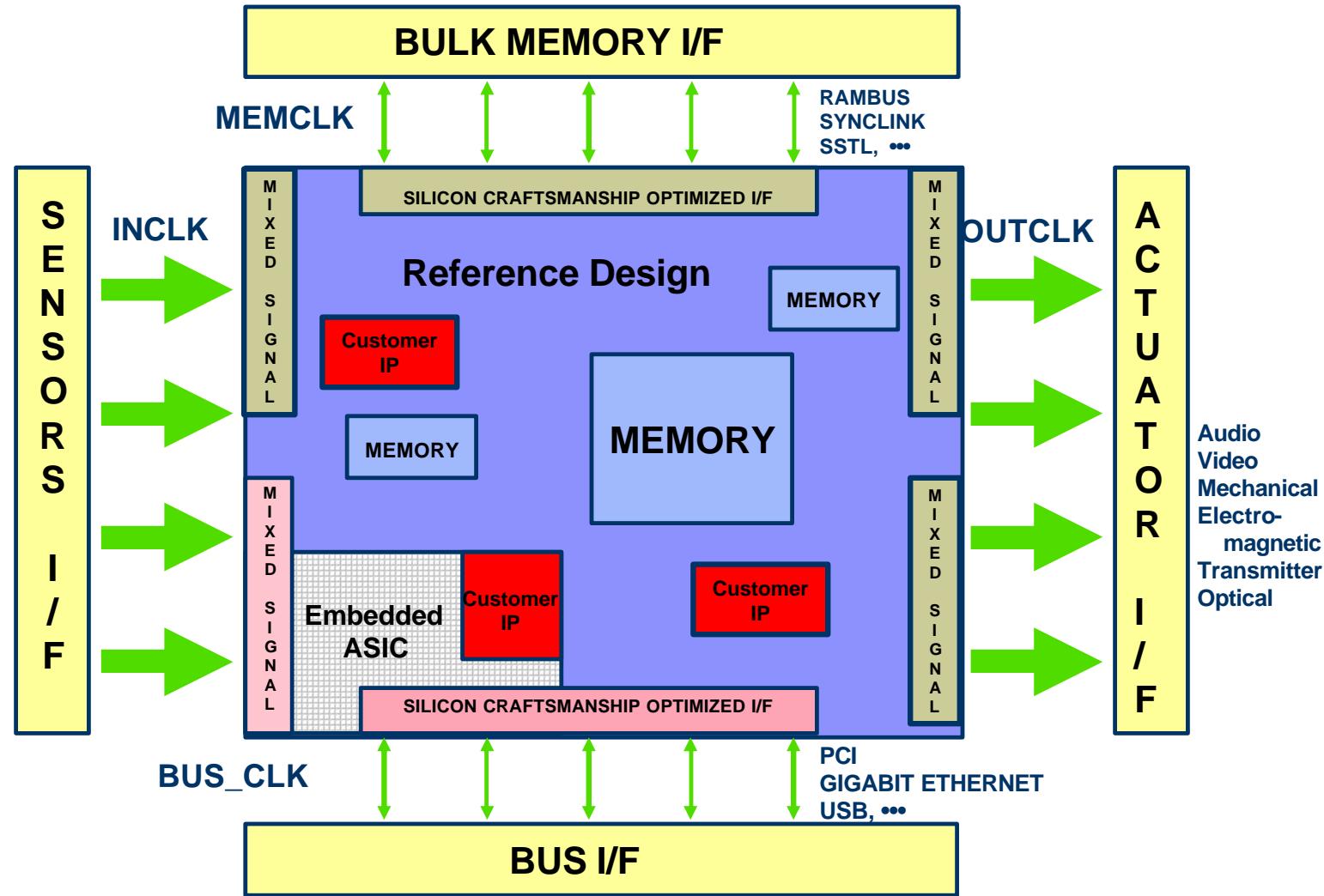
### Generic Wireless / Computing





## 4. A Typical SOC Design Example (2)

### The Hardware View of SOC





## 5. Current Status of SOC

### The Phenomenon after SOC appearance

- ◆ Education :
  - The topics of SOC design is worth to research , such as : Physical design, synthesis, system-level design, programmable components and systems, testing and verification.
  - The academic conferences focus on the SOC Design
- ◆ Industry :
  - The SOC environment is building for design, simulation and testing.
    - Motorola : System On a Chip Design Technology Center (SoCDT)
    - VSIA&VCX : building the IP reuse protocols.



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5. Mixed Mode Design
6. SOC Design Tasks
7. IP reuse
8. The Trends of SOC

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# 1. SOC Design Flow and Tools

Traditional ASIC design flow

Specification development

RTL code development

Functional verification

Synthesis

Timing verification

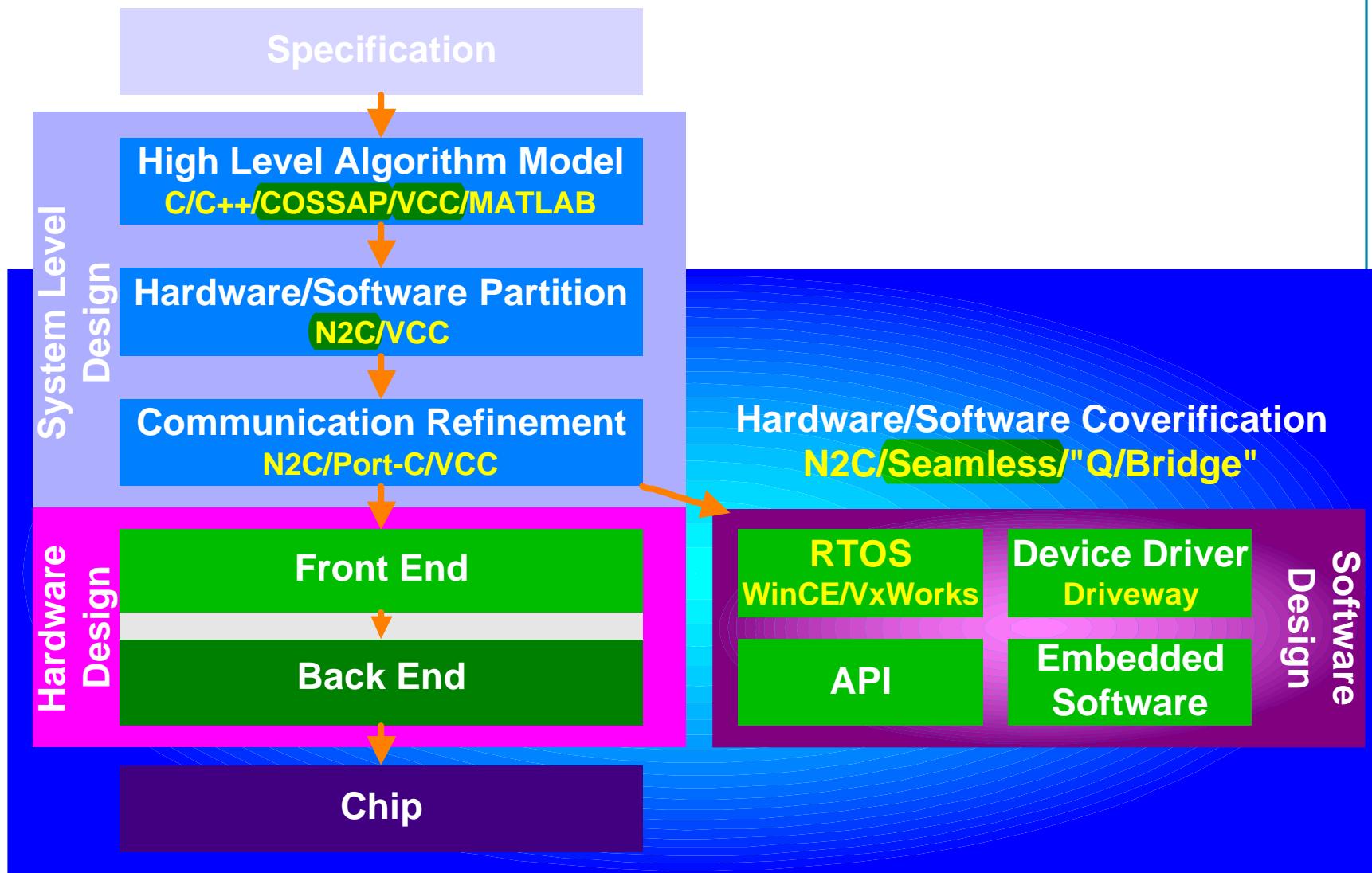
Place and route

Prototype build and test

Deliver to system integration and software test

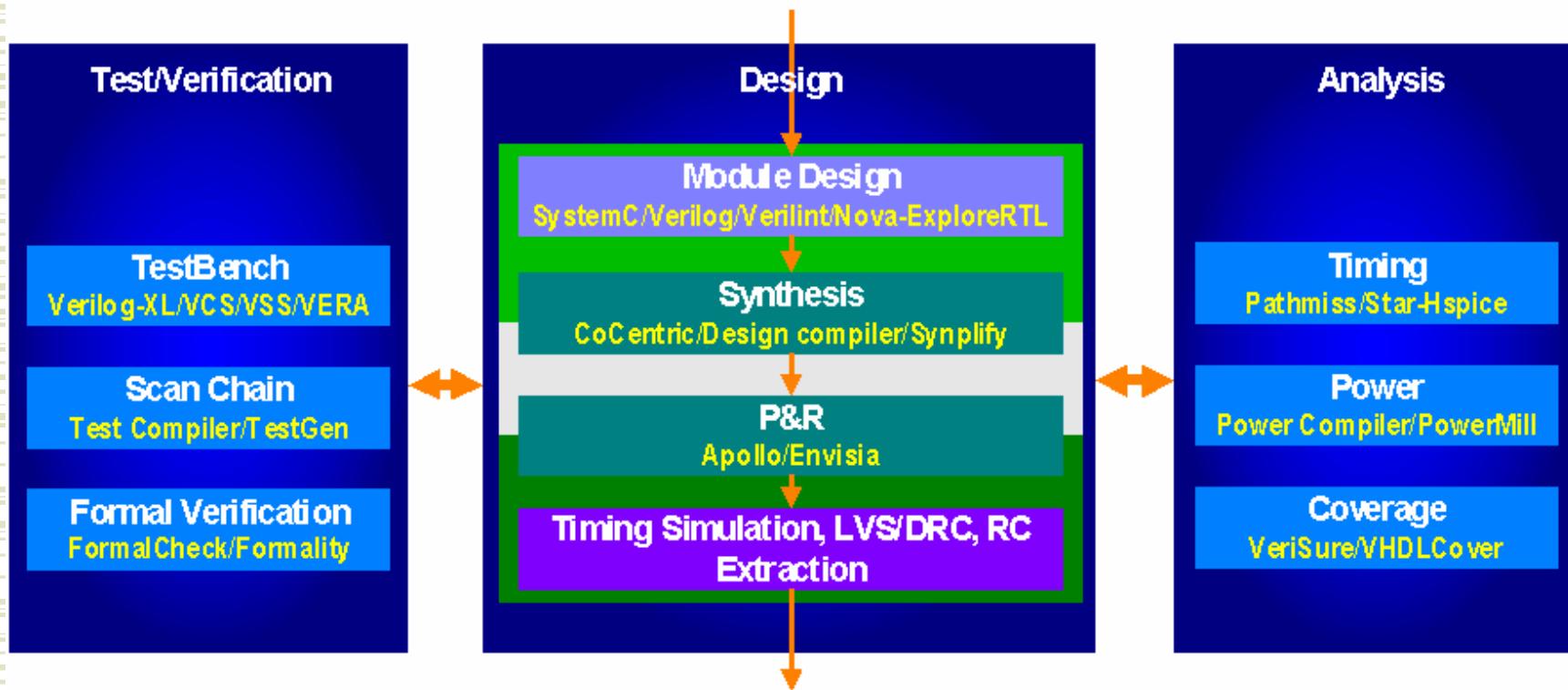


# 1. SOC Design Flow and Tools(2)





# 1. SOC Design Flow and Tools(3)





# 1. SOC Design Flow and Tools(4)

## Tools in Taiwan

- ◆ Full-Custom IC Design
  - Composer : Schematic Editor/Symbol Editor
  - Cadence/Virtuoso : Layout
  - Dracula/DIVA : Layout Verification
  - HSPICE : Timing Simulation
  - TimeMill/PowerMill/PathMill : Timing/ Power Simulation
- ◆ Cell-Based IC Design
  - Verilog、VHDL、VCS : RTL Level or Gate Level Simulation
  - Debussy : Verilog or VHDL
  - Synopsys、Ambit : Logic Synthesis
  - Cadence、Apollo : Layout (Flowplan & Placement & Routing)
  - TimeMill/PowerMill/PathMill or Star-sim : Circuit Level Timing Simulation / Power Simulation



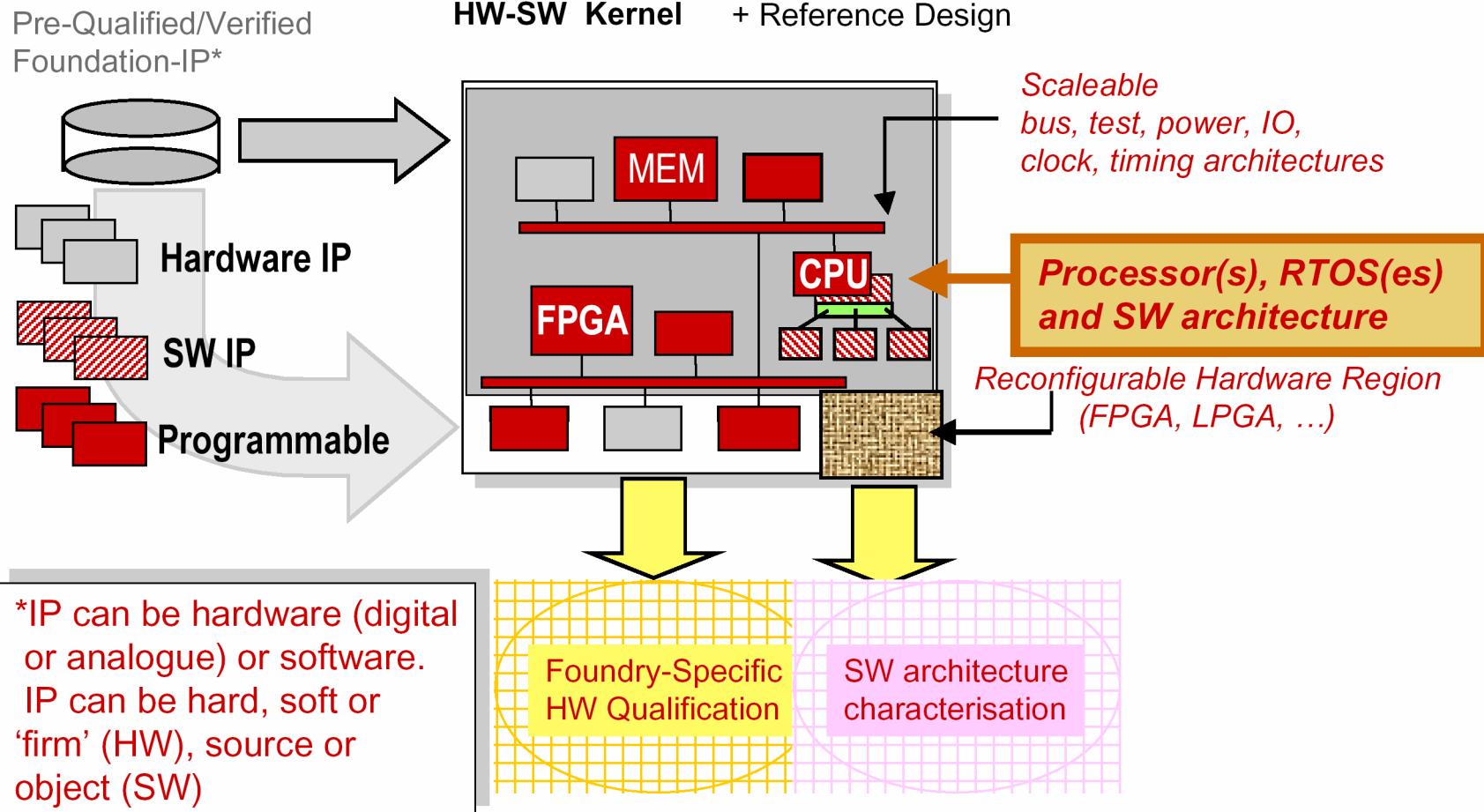
# 1. SOC Design Flow and Tools(5)

- ◆ **FPGA or CPLD Design**
  - Xilinx / Altera
  - Synplify
- ◆ **MM/RF IC Design**
  - Harmonica
  - Symphony (linear、nonlinear system simulation)
- ◆ **Testing**
  - SYNTEST
  - METOR
  - IMS testing station



## 2. Platforms Based SOC Design

### A Hardware-centric View of a Platform

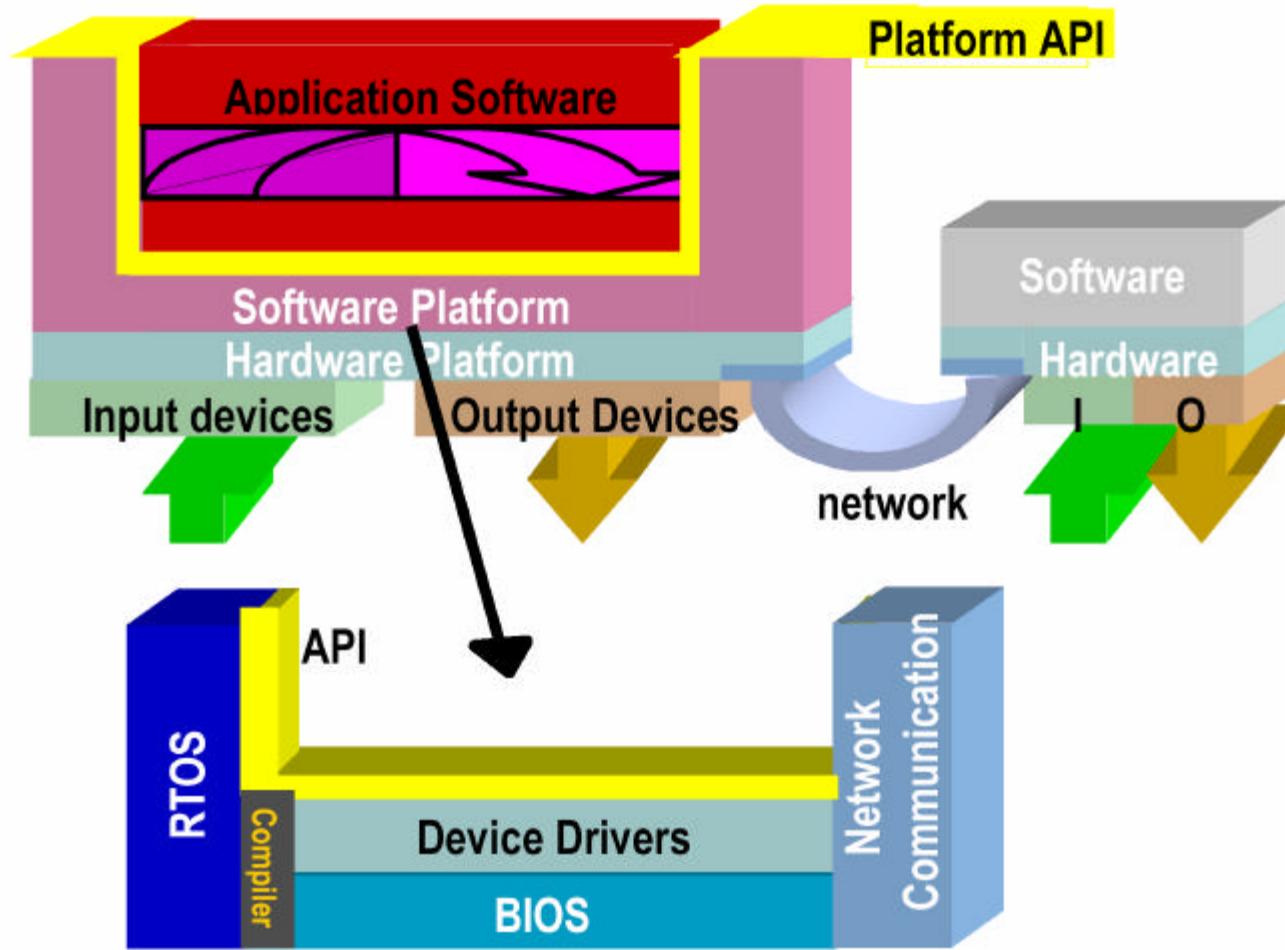


Source: Grant Martin and Henry Chang, ISQED 2002 Tutorial



## 2. Platforms Based SOC Design(2)

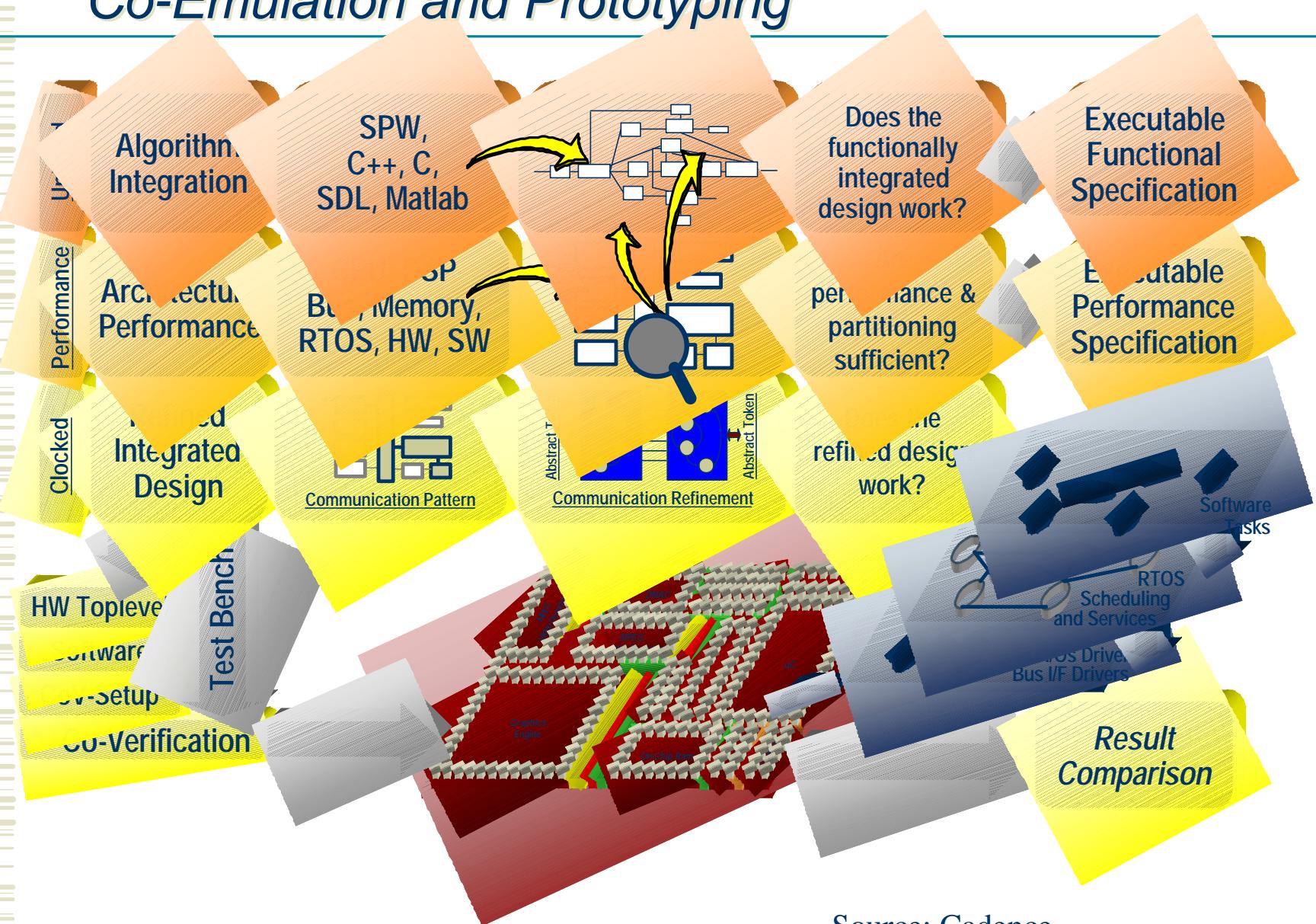
### A Software-centric View of a Platform



Source: Grant Martin and Henry Chang, ISQED 2002 Tutorial



### 3. Hardware & Software Co-design/ Co-simulation/ Co-Emulation and Prototyping





## 4. Embedded RTOS

### ❖ *Embedded Software Characteristics*

- Real Time
- Complex
- Robust
- Code Size
- Low Power

### ❖ *RTOS*

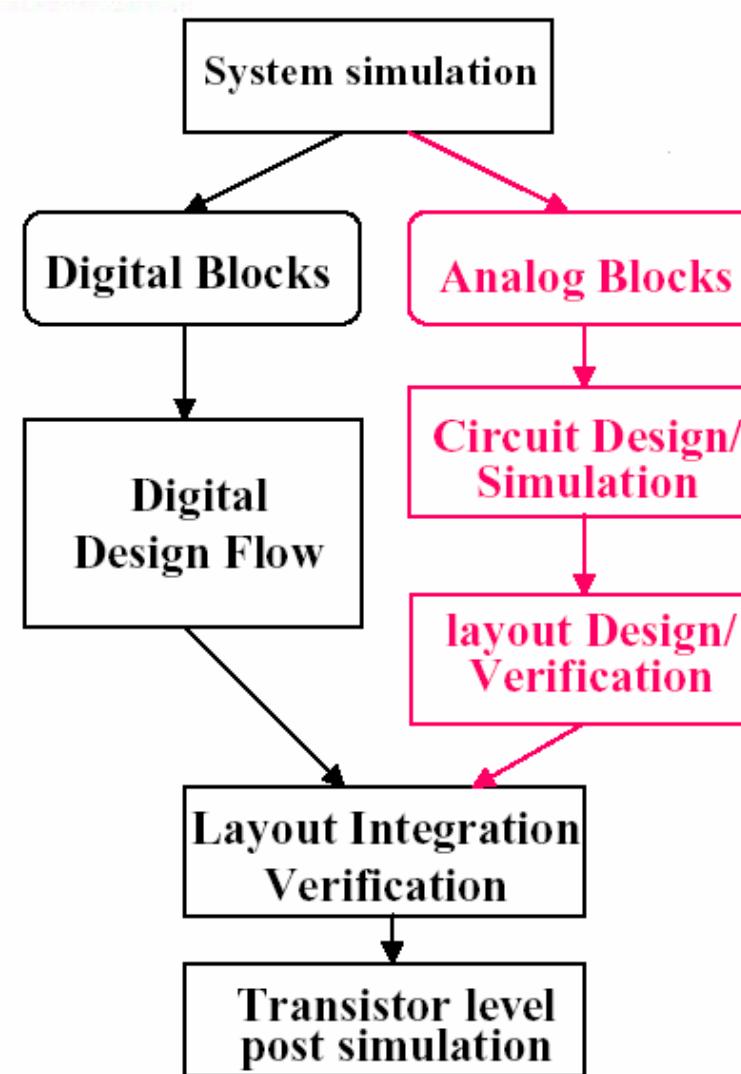
- *Correct Results must be Provided at Required Time Deadlines*

### ❖ *Commercial RTOS:*

- ❖ VxWorks
- ❖ pSOS
- ❖ Embedded Linux
- ❖ eCos



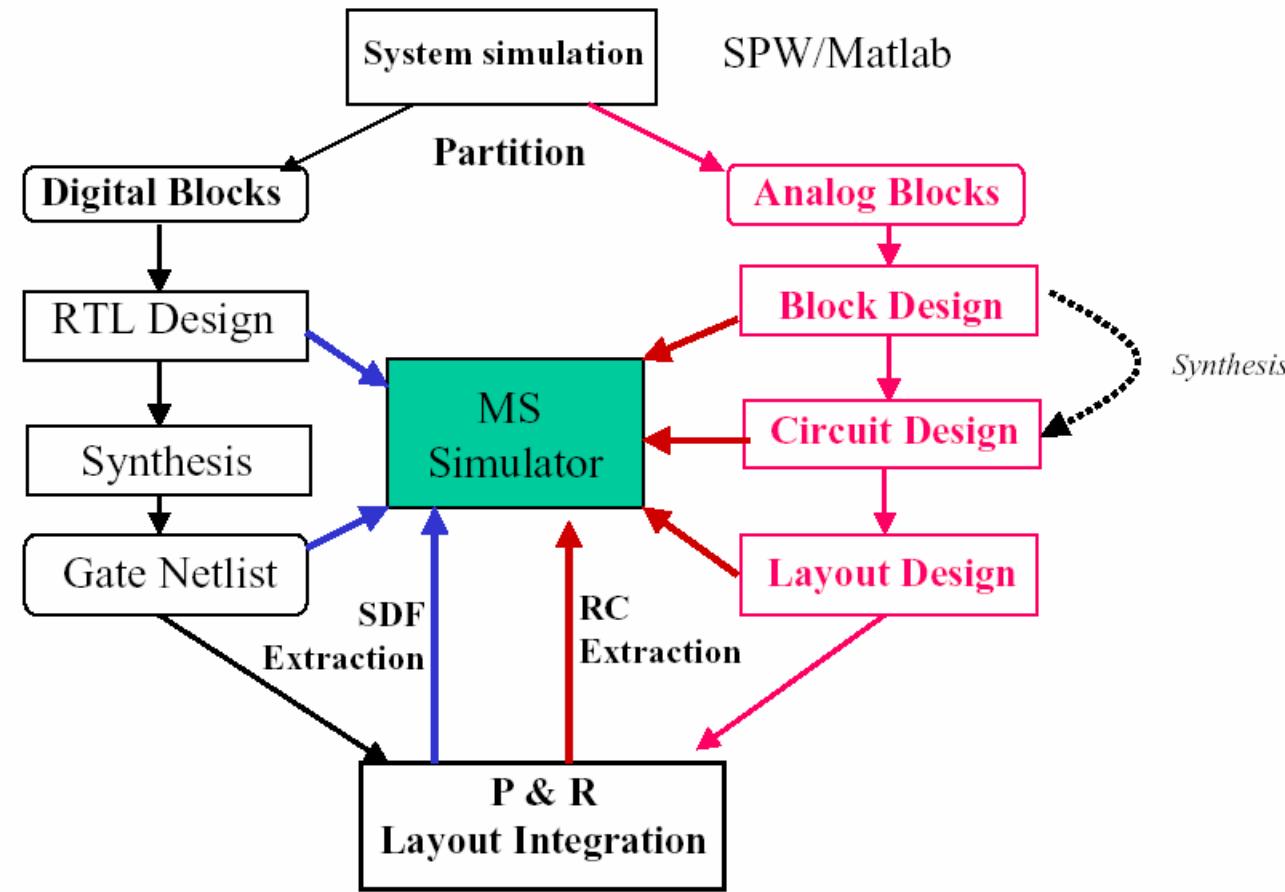
## 5. Mixed-Signal Design





# 5. Mixed-Signal Design(2)

## Mixed-Signal Top Down Design Flow





## 5. Mixed-Signal Design(3)

### ***De-efficiency of the conventional approach***

- ❖ The analog / digital design processes are almost independent, lack of horizontal link
- ❖ The spec. of analog circuit might be over-specified for ensuring correctness of system integration
- ❖ Hard of analog/Mixed Signal block reuse evaluation



## 6. SOC Design Tasks

1. Definition of system-level design specification (C-based , HDLs)
2. Design evaluation and exploration
3. Hardware/Software codesign
4. Co-verification : co-simulation and co-emulation
5. Debugging and diagnosis
6. Rapid prototyping



# 6. SOC Design Tasks(2)

## Design Technology Status

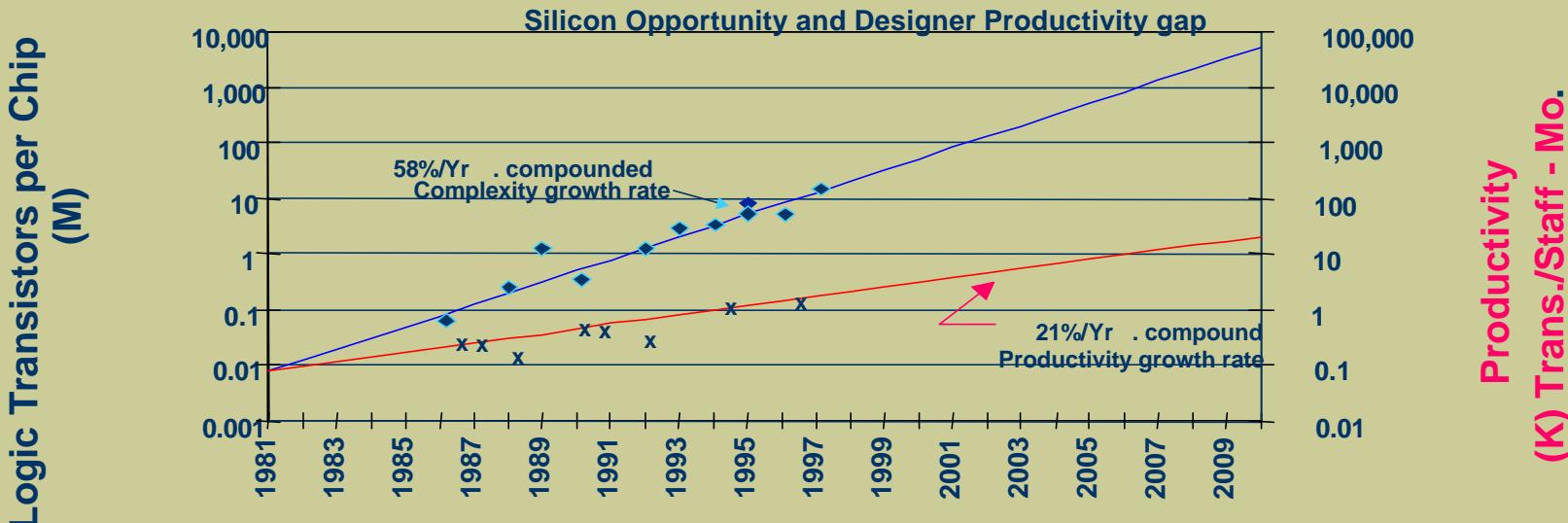
- ◆ Problems
  - Productivity gap
  - Time-to-market
  - Complex systems
  - Designer shortage
  - Deep submicron effects
- ◆ Solutions
  - Higher levels of abstraction → shorter simulation time and solve the problems of productivity gap.
  - Use a known real entity → A platform or A pre-designed component
  - Partition → Based on functionality, Hardware and software
  - Modeling → At different level, Consistent and accurate
  - New reuse methodology → shorter time-to-market
  - New business model → solve the problems of Designer shortage



# 6. SOC Design Tasks (3)

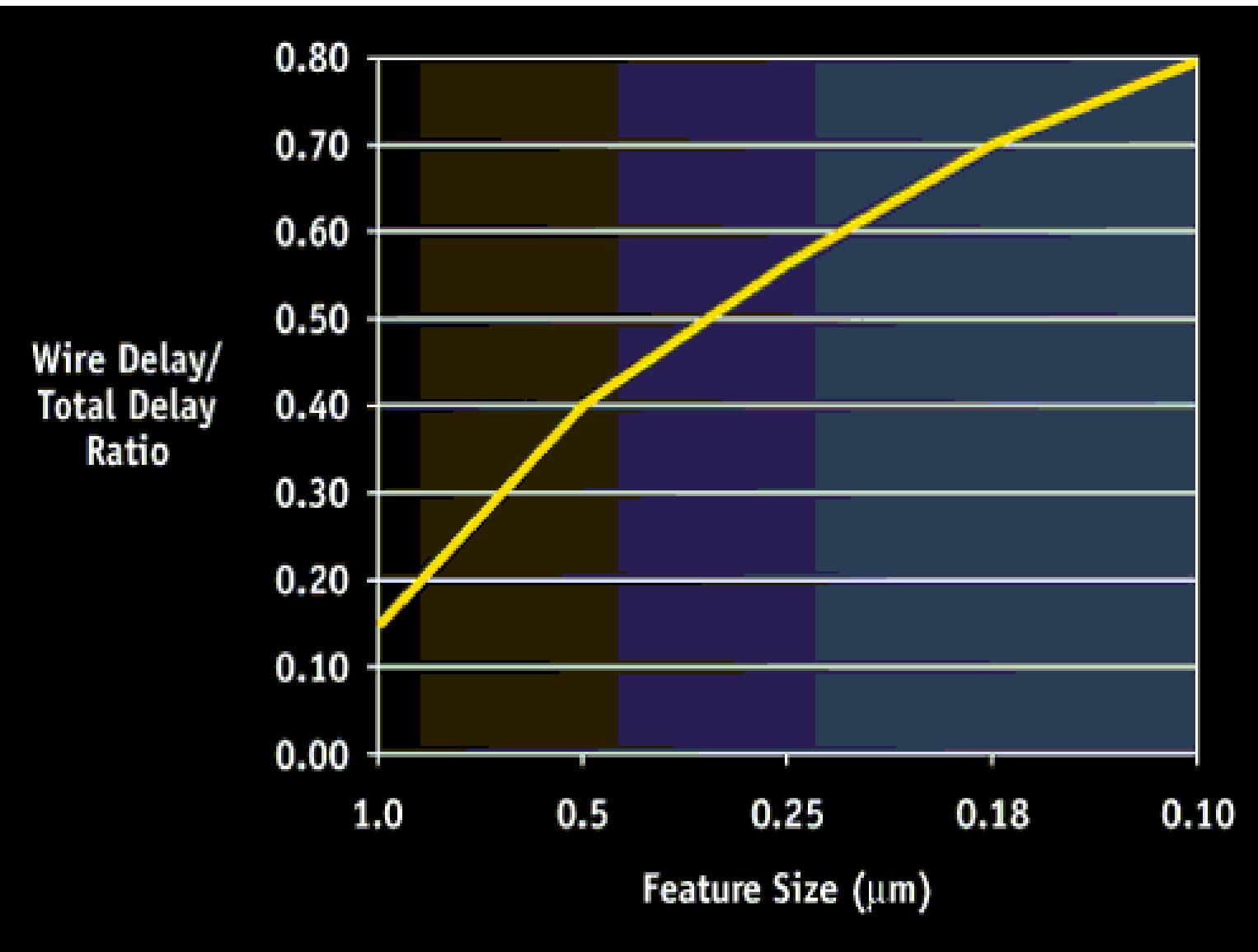
## Major design discontinuity

\* Need **methodology** and **tools** breakthrough to fill the gap!!





## 6. SOC Design Tasks (4)





## 7. IP reuse(6)

### Design Key Point

- ◆ Designed to solve a general problem.
- ◆ Designed for use in multiple technologies.
- ◆ Designed for simulation with a variety of simulators.
- ◆ Verified independently of the chip in which it will be used.
- ◆ Verified to a high level of confidence.
- ◆ Fully documented in terms of appropriate applications and restrictions.



## 7. IP reuse(7)

### Current Status of IP Reuse

- ◆ VSIA(Virtual Socket Interface Alliance) has launched a variety of Development Working Groups (DWGS) to define technical standards. (<http://www.vsi.org>)
- ◆ VCX (Virtual Component Exchange) has launched a number of DWGs to define IP trading standards and creating a safe, efficient, international marketplace for buying and selling IPs. (<http://www.vcx.org>)
- ◆ On the IP business side :
  - A small business venue (1999, 51% revenue are dominated by three big players : ARM, MIPS, and RamBus)



## 8. The Trends of SOC

- ◆ Giga-scale system-on-a-chip(SOC)
- ◆ Nanometer technologies on SOC
- ◆ High level design abstraction
- ◆ Adequate methodologies for design reuse
- ◆ Reprogrammable resources(FPSOC, Field-Programmable System-On-a-Chip) provides significant opportunities in future SOC design.



## 8. The Trends of SOC(2)

### *Megatrends of SoC Era*

- ❖ Design RE-USE becomes common
  - ◆ Quality of reusable IP
  - ◆ Ease of Use
  - ◆ Efficiency
  - ◆ Standardization of Core Protocol
- ❖ Most of design effort is focused on VERIFICATION
  - ◆ Accelerating Co-Verification
  - ◆ Real-World Stimuli
- ❖ DSM INTERCONNECT



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# 1. Establish a Complete SOC Development Infrastructure

- ❖ IP
  - Processor IP
  - Application Specific IP
  - Platform IP
- ❖ IC Design
  - Product Standard
  - System Know How
  - Software
  - Design Integration
  - SOC Design Capability
- ❖ Foundry/Package/Testing
  - Application Specific Processes
  - Foundry Dependent IP
  - Process Integration
  - Testing

- Application Specific Process/IP
- Process Dependent IP
- System Know-how
- Driven Product Standard
- Flexibility Service
- Cost Effective Solution

Design Houses

IDM



## 2. System Integration Issues in Physical Design

- ◆ Timing closure
- ◆ Power closure
- ◆ Power/Ground Network Design, Clock Distribution , and signal integrity-related problems
- ◆ Process migration
- ◆ Reliability
- ◆ Better characterization of small and IP blocks
- ◆ Performance and reliability-aware design rules
- ◆ On-chip optical interconnects



## 2. System Integration Issues in Physical Design(2)

- ◆ Mixed signal design
- ◆ On-the-fly extraction and order reduction
- ◆ New component models and CAD tools for MEMs(微機電系統) and MOEMs (微光機電元件).
- ◆ Computationally efficient , highly scalable algorithms for physical design.
- ◆ Integrated and flexible physical design tools that consider realistic operating conditions



### 3. System Integration Issues in Synthesis

#### **Synthesis problems in SOC.....**

- ❖ Today's EDA tool flow, functional realm and physical world is separate
- ❖ In deep-submicron the dominating factor is interconnect, not gates.
- ❖ The effects of inaccurate wire-load models are not discovered until after placement and rout
- ❖ The iterations between placement and rout occurs many times
- ❖ The length and unpredictability have impact on design schedule
- ❖ Tightly link between front and back-end.
  - RTL floor-plan, time budgeting.
  - Accurate predictions on inter-block delay



## 3. System Integration Issues in Synthesis (2)

- ◆ Synthesis to support IP creation
  - For SOC design , synthesis tools must be able to generate the IP blocks that are easy to integrate.
- ◆ Hierarchical Synthesis
  - In the synthesis process, we must have a better hierarchical approach methods to deal with the problems of area,timing,power and constraints.
- ◆ Low Power Synthesis



### 3. System Integration Issues in Synthesis (3)

- ◆ Analog Synthesis
- ◆ Layout-Based Synthesis
  - The internal connection delays and signal integrations are also considerable.
- ◆ Bus and Interface Synthesis
  - The internal series and bus connections are bringing out the critical path in the SOC design, the synthesis tools must consider this influence of delay, area and power.



## 4. System Integration Issues in System-Level Designs

- ◆ Design Methodology
  - Design by higher levels of abstraction methods.
- ◆ Core-based Design
  - Cores and IP reuse
- ◆ IP Issues
  - In the IP reuse, there are still many problems of importing, exporting, and documenting.
- ◆ Architectural Design Issues
  - We need better tools and methods for SOC design.
- ◆ Multi-disciplinary Design
- ◆ Increased Productivity
- ◆ Miscellaneous Challenges



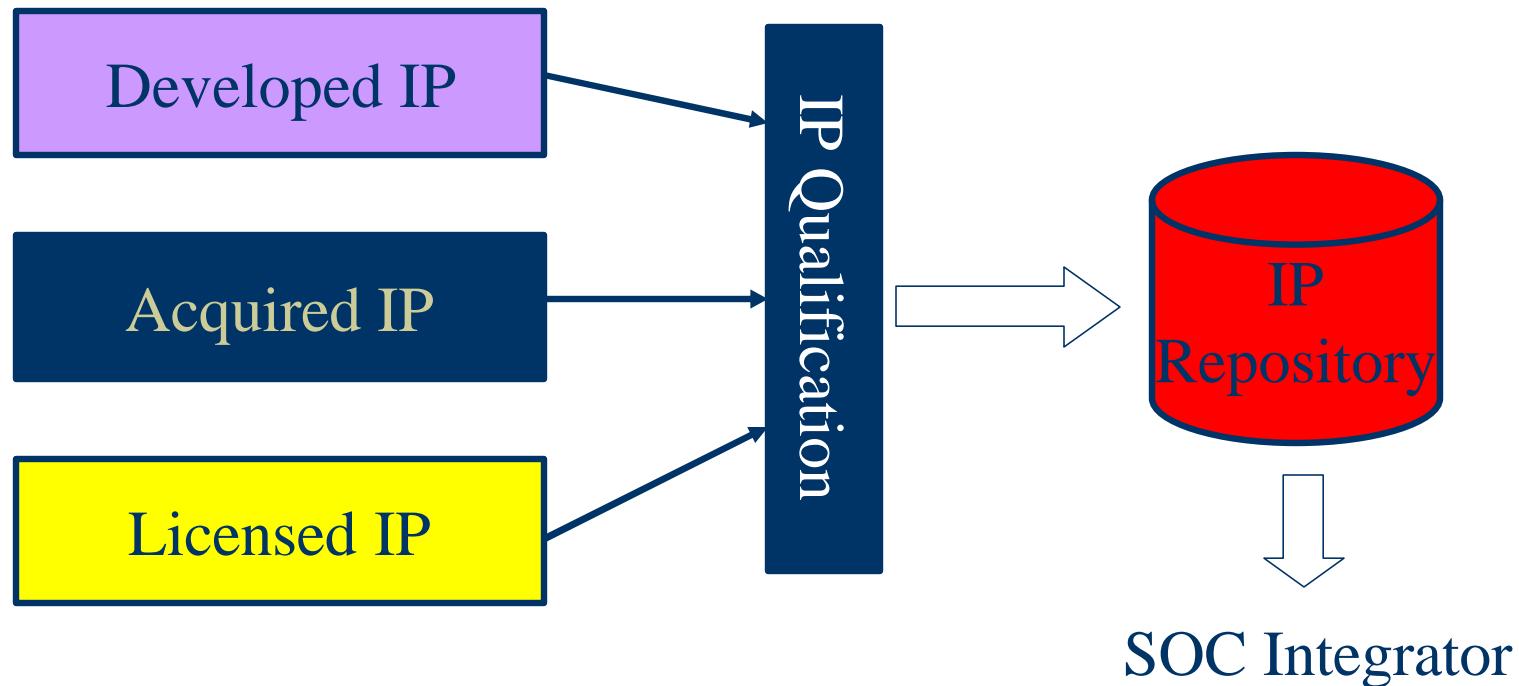
## 5. IP Related Issues

- ◆ IP protection
  - (watermarking, fingerprinting and encryption )
- ◆ IP exporting
  - (implementation, documentation creation, tool support, integrated development environments, test and customer support)
- ◆ IP importing
  - (evaluation, qualification, and computability)



## 5. IP Related Issues(2)

### IP Qualification



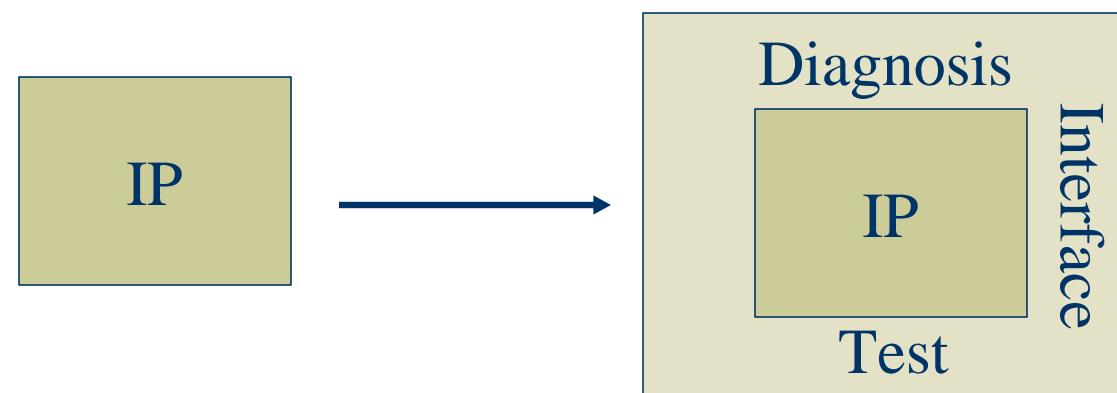
All IP must be qualified, assured.



## 5. IP Related Issues(3)

### IP Responsibility

You must be able to show that your IP works correctly within your customer's manufactured SOC, not just in your own verification environment !!





## 6. System Integration Issues in Verification and Testing

- ◆ Hybrid, Semi-Formal Verification
  - Better simulation, emulation and model checking methods and environments.
- ◆ Multi-Level/Mixed-Mode/Mixed-Technology Simulation Framework



## 6. System Integration Issues in Verification and Testing

- ◆ Testing strategy/standard for embedded IP blocks
- ◆ Full-chip self-test techniques/methodologies
- ◆ Built-in self-test, self-diagnosis and self-repair techniques for deep submicron, embedded memories
- ◆ Test scheduling and power/thermal management
- ◆ SOC test synthesis tool development



## 7. Integration-Centric Approach

Issue	IP-Centric	Integration-Centric
Create IP Apps.	Can be modified in all Apps	Can be reused /no change
Market View	IP for any market	Key market to serve
Design Flow	Make IP like ASIC Cell Lib	Create system for target market
Design Usage	Flexible and Re-verifiable	Plug into integration platform
Product Adaptation	To product requirement	To product domain
Time-To-Market	Flexible IP Can be Change easily	Solid IP NO need to Change, PnP !



# Outline

1. Introduction to SOC
2. Design methodologies and trends for SOC
3. System integration issues for SOC
4. Conclusions



# Conclusion

- ◆ SOC is Sound of Century
- ◆ SOC design methodology needs to be studied further
- ◆ New test paradigm and methodologies
- ◆ Challenges and opportunities in Giga-scale integration for SOC & Nanometer technologies
- ◆ SOC & IP Center in Taiwan



# References

- ◆ Michael Keating and Pierre Bricaud, "Reuse Methodology Manual For System-On-A-Chip Designs", KLUWER ACADEMIC PUBLISHERS, 1999.
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