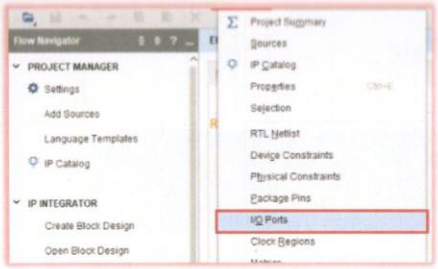
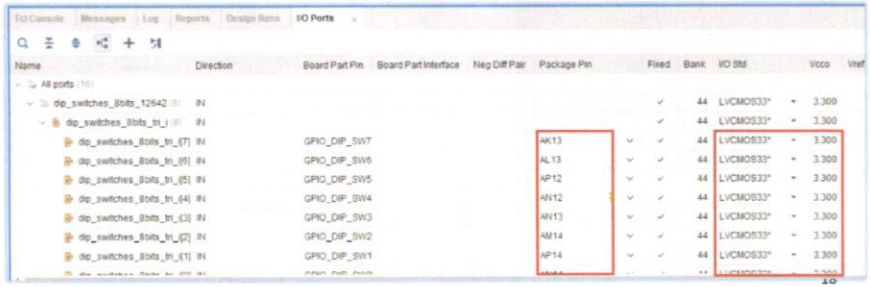
# FPGA I/O Pin Assign

NARLabs

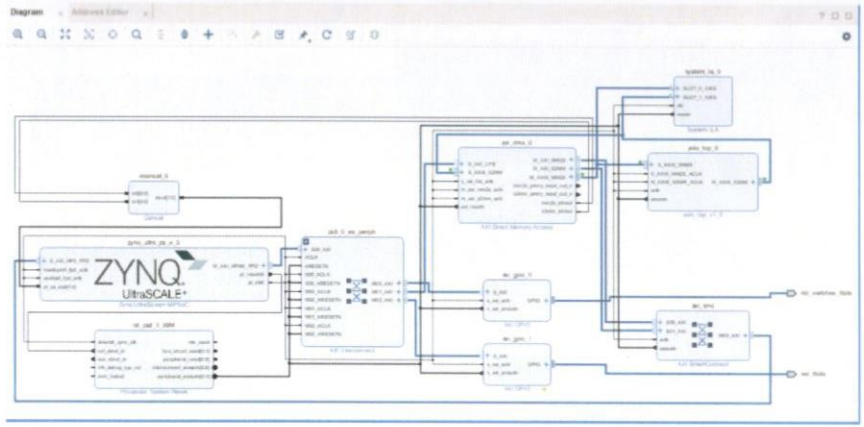
Flow Navigator→
RTL Analysis→
Open Elaborated Design




# Block Design- Diagram

NARLabs

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# Block Design- Address Editor

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# Zynq UltraScale+MSPoC

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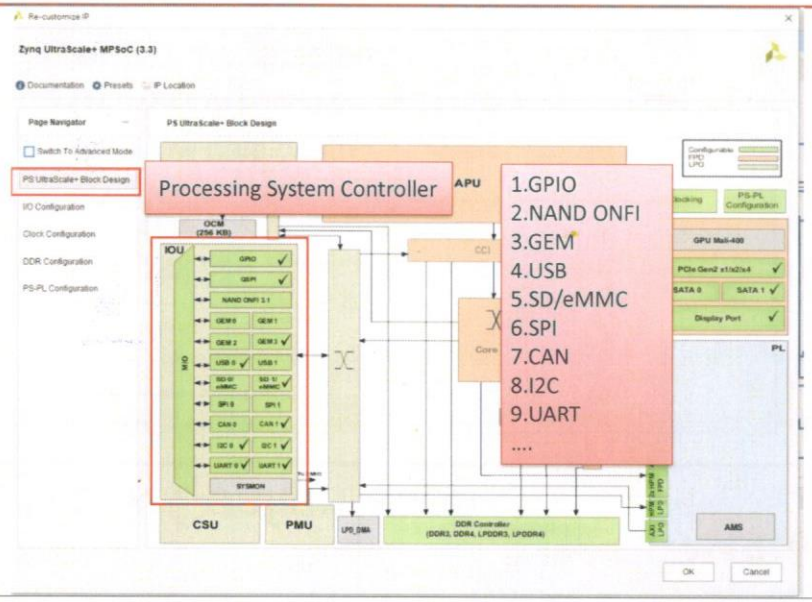


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