

Project Name & Location

NARLabs

New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

☒ Create project subdirectory

Project will be created at E:\Proj_2022\ZCU102_Lab\mpsoc_lab\system

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Project Type

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New Project

Project Type
Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☐ Do not specify sources at this time

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

☐ **IO Planning Project**
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

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Choose ZCU102 Evaluation Board

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New Project

Default Part
Choose a default Xilinx part or board for your project.

Parts: **Boards**

Reset All Filters

Vendor: All Name: All Board Rev: Latest

Search: 100 (1 match)

Display Name	Preview	Vendor	File Version	Part	I/O Pin
Zynq UltraScale+ ZCU102 Evaluation Board Add Daughter Card Connections		xilinx.com	3.3	xczu9eg-ff01156-2-e	1156

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Project Summary

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New Project

VIVADO
HLS Edition

New Project Summary

- A new RTL project named Test will be created.
- No source files or directories will be added. Use Add Sources to add them later.
- No constraints files will be added. Use Add Sources to add them later.
- The default part and product family for the new project:
Default Board: Zynq UltraScale+ ZCU102 Evaluation Board
Default Part: xczu9eg-ff01156-2-e
Product: Zynq UltraScale+ Family: Zynq UltraScale+ MPSoCs
Package: ff01156
Speed Grade: -2

XILINX To create the project, click Finish

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