

MPSoC System Design Example

NARLabs MPSoC Lab System DDR4 Processor UART AXI Bus ILA AXI DMA AXI GPIO#1 Wrapper AXI GPIO#2 FIFO DIP Switch LED User IP

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NARLabs MPSoC system design example

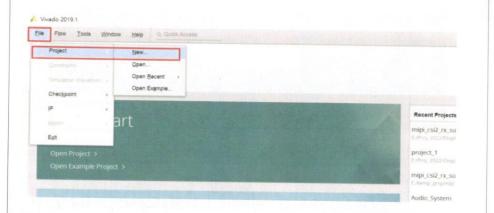
- Vivado design flow(HW)
 - Create MPSoC project
 - Set IP Repository
 - Create system block design
 - PS IP:UART
 - · PL IP:AXI GPIO, AXI DMA, User IP
 - · Bus connection
 - Interrupt
 - Memory Map (Address Editor)
 - ILA
- SDK design flow(FW / bare-metal)
 - Create application project
 - Run application
 - HW/SW debug

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Create Project

File→Project→New...



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