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416x416變數宣告

```
drawh 🖾
     typedef struct ImgS
         int h:
         int c;
         unchar *data:
     -}ImgS;
     //The first saved frame
     unchar FstFrame[TBSIZE] = {0};
     unchar chn1[CHNLSIZE] = {0}; //??B
     unchar chn2[CHNLSIZE] = {0}; //??G
     unchar chn3[CHNLSIZE] = {0}; //??R
      //Jackol define
     unchar DwnCh1[DWNSIZE] = {0}; //??B
      unchar DwnCh2[DWNSIZE] = {0}; //??G
      unchar Padding1[PADDSIZE] = {0}; //??!
      unchar Padding2[PADDSIZE] = {0}; //??G
      unchar Padding3[PADDSIZE] = {0}; //??R
      //CY add for verify AXI DMA function
     unchar Padding1 RX[PADDSIZE] = {0}; //??!
      unchar Padding2_RX[PADDSIZE] = {0}; //??
       inchar Padding3 RX[PADDSIZE] = {0}; //?3
```

- PADDSIZE=173056 (416*416)
- Downsize影像變數
 - Padding1 \ Padding2 \ Padding3
- IP運算完之變數
 - Padding1_RX \ Padding2_RX \ Padding3_RX

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AXI DMA傳輸副程式

- void AXI_DMA_Transfer(UINTPTR BuffAddr, u32 Length, int Direction)
- Direction參數說明:
 - DDR到IP: XAXIDMA DMA TO DEVICE
 - IP到DDR: XAXIDMA DEVICE TO DMA
 - PADDSIZE: 資料長度 (Byte)
- 使用範例:

```
AXI_DMA_Transfer((UINTPTR)(&Padding1) ,PADDSIZE, XAXIDMA_DMA_TO_DEVICE);

AXI_DMA_Transfer((UINTPTR)(&Padding1_RX),PADDSIZE, XAXIDMA_DEVICE_TO_DMA);

Xil_DCacheFlushRange((UINTPTR)Padding1, PADDSIZE);

Xil_DCacheFlushRange((UINTPTR)Padding1_RX, PADDSIZE);
```

DCache刷新副程式

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- void Xil_DCacheFlushRange(INTPTR adr, INTPTR len)
- 使用範例:

```
Xil_DCacheFlushRange((UINTPTR)(&Padding1),
Xil_DCacheFlushRange((UINTPTR)(&Padding1),
Xil_DCacheFlushRange((UINTPTR)(&Padding1),
Xil_DCacheFlushRange((UINTPTR)(&Padding2),
PADDSIZE);
Xil_DCacheFlushRange((UINTPTR)(&Padding2, RX),
Xil_DCacheFlushRange((UINTPTR)(&Padding3),
Xil_DCacheFlushRange((UINTPTR)(&Padding3),
PADDSIZE);
Xil_DCacheFlushRange((UINTPTR)(&Padding3),
PADDSIZE);
Xil_DCacheFlushRange((UINTPTR)(&Padding3),
PADDSIZE);

//start Padding to IP,CYCHEN add-
AXI_DMA_Transfer(&Padding1_RX,PADDSIZE, XAXIDMA_DEVICE_TO_DMA);
Xil_DCacheFlushRange((UINTPTR)Padding1_RX, PADDSIZE);
Xil_DCacheFlushRange((UINTPTR)Padding1_RX, PADDSIZE);
```

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AXI DMA/IP 驗證

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