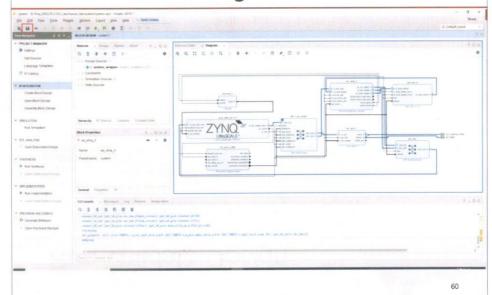


NARLabs

Save Block Design



MARLabs Debug S_AXIS_S2MM A A H N O G | * * - / H A, O V O + SLOT_S_AKS yolo top 0 M_AXI_MM2S + -# S ANS MICS M AXI SZMM + # 5 AXIS 5218M M_AXIS_MM2S + B - M AXIS SZMM ACLK M AXIS SZMM + mm2s_prmy_reset_out_n • Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its Q = 0 + 500_AXI in Hardware Manager, System LA, Rinkgräded Logic, Analyzer, IP core is a logic analozer which allows into to perform in-eystem debugging of designs, and shows interface level events in the Hardware Manager in an infusi ₹ 0 + yolo_top_0_M_AXIS_528M tions ultra on a deal clad-'peripheral aresety to the following sink reset pins # MIC MMCD, to Doctor ILA slot interface pin /evoter ile.

Create Block Design HDL Wrapper

