

# Debug M\_AXIS\_MM2S

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Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

Search:

Interface Connections

- ☒ All Automation (1 out of 1 selected)
- ☒ Interface Connections
- ☒ M\_AXIS\_MM2S

Description

Connect selected interface-connection and/or net to System I/LA Core for Debugging in Hardware Manager. System I/LA (Integrated Logic Analyzer) IP core is a logic analyzer which allows you to perform in-system debugging of designs and shows interface level events in the Hardware Manager in an intuitive way.

Options

API Stream Signal: Data and Trigger

Source Clock: sys\_clk

System I/LA: Auto

API Stream Protocol Checker: ☐

OK Cancel

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# Debug S\_AXIS\_S2MM

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Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

Search:

Interface Connections

- ☒ All Automation (2 out of 1 selected)
- ☒ Interface Connections
- ☒ S\_AXIS\_S2MM

Description

Connect selected interface-connection and/or net to System I/LA Core for Debugging in Hardware Manager. System I/LA (Integrated Logic Analyzer) IP core is a logic analyzer which allows you to perform in-system debugging of designs and shows interface level events in the Hardware Manager in an intuitive way.

Options

API Stream Signal: Data and Trigger

Source Clock: sys\_clk

System I/LA: Auto

API Stream Protocol Checker: ☐

OK Cancel

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# Save Block Design

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Save Block Design

Block Design: system

Save

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# Create Block Design HDL Wrapper

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Create HDL Wrapper

You can either add or copy the HDL wrapper file to the project. Use copy option if you would like to modify this file.

Options

- ☐ Copy generated wrapper to allow user edits
- ☒ Let Vivado manage wrapper and auto-update

OK Cancel

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