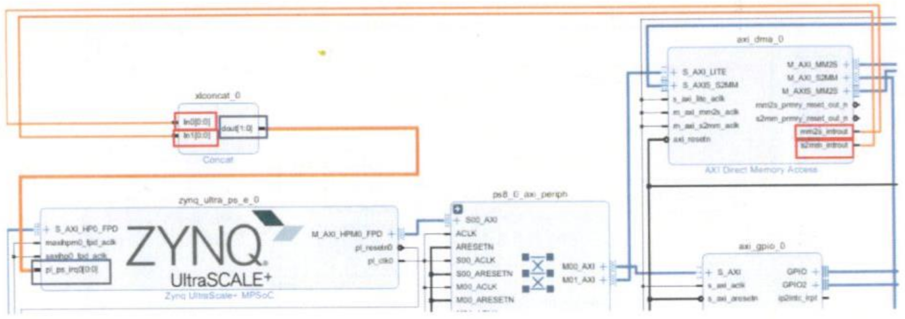
Add Concat IP & Bus Connection (AXI DMA Interrupt)

NARLabs

發出 pulse, 對 Tx, Rx



pl_ps_irq: AXI DMA Interrupt

Interrupt Handler (SDK ; for ref.)

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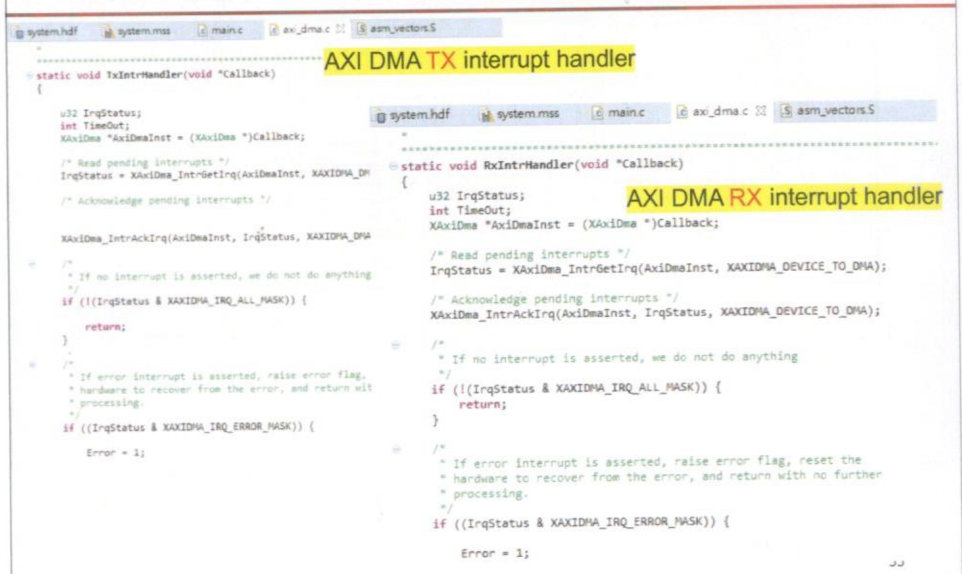

AXI DMA TX interrupt handler

```
*
*******************************************************
static void TxIntrHandler(void *Callback)
{

    u32 IrqStatus;
    int TimeOut;
    XAxiDma *AxiDmaInst = (XAxiDma *)Callback;

    /* Read pending interrupts */
    IrqStatus = XAxiDma_IntrGetIrq(AxiDmaInst, XAXIDMA_DM

    /* Acknowledge pending interrupts */


    XAxiDma_IntrAckIrq(AxiDmaInst, IrqStatus, XAXIDMA_DMA

    /*
     * If no interrupt is asserted, we do not do anything
     */
    if (!(IrqStatus & XAXIDMA_IRQ_ALL_MASK)) {

        return;
    }

    /*
     * If error interrupt is asserted, raise error flag,
     * hardware to recover from the error, and return wit
     * processing.
     */
    if ((IrqStatus & XAXIDMA_IRQ_ERROR_MASK)) {

        Error = 1;
```

AXI DMA RX interrupt handler

```
*
*******************************************************************
static void RxIntrHandler(void *Callback)
{
    u32 IrqStatus;
    int TimeOut;
    XAxiDma *AxiDmaInst = (XAxiDma *)Callback;

    /* Read pending interrupts */
    IrqStatus = XAxiDma_IntrGetIrq(AxiDmaInst, XAXIDMA_DEVICE_TO_DMA);

    /* Acknowledge pending interrupts */
    XAxiDma_IntrAckIrq(AxiDmaInst, IrqStatus, XAXIDMA_DEVICE_TO_DMA);

    /*
     * If no interrupt is asserted, we do not do anything
     */
    if (!(IrqStatus & XAXIDMA_IRQ_ALL_MASK)) {
        return;
    }

    /*
     * If error interrupt is asserted, raise error flag, reset the
     * hardware to recover from the error, and return with no further
     * processing.
     */
    if ((IrqStatus & XAXIDMA_IRQ_ERROR_MASK)) {

        Error = 1;
```

Run Connection Automation

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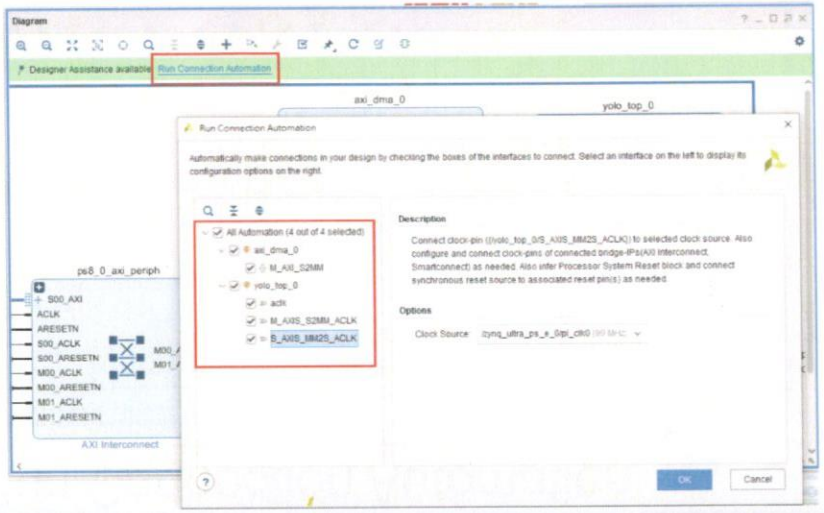

Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

- [✓] All Automation (4 out of 4 selected)
  - [✓] axi_dma_0
    - [✓] M_AXI_S2MM
  - [✓] yolo_top_0
    - [✓] aclk
    - [✓] M_AXIS_S2MM_ACLK
    - [✓] S_AXIS_MM2S_ACLK

Description

Connect clock-pin (/yolo_top_0/S_AXIS_MM2S_ACLK) to selected clock source. Also configure and connect clock-pins of connected bridge-IPs(AXI interconnect, Smartconnect) as needed. Also infer Processor System Reset block and connect synchronous reset source to associated reset pin(s) as needed.

Options

Clock Source: /zynq_ultra_ps_e_0/pl_clk0 (99 MHz)

HW Debug(ILA)

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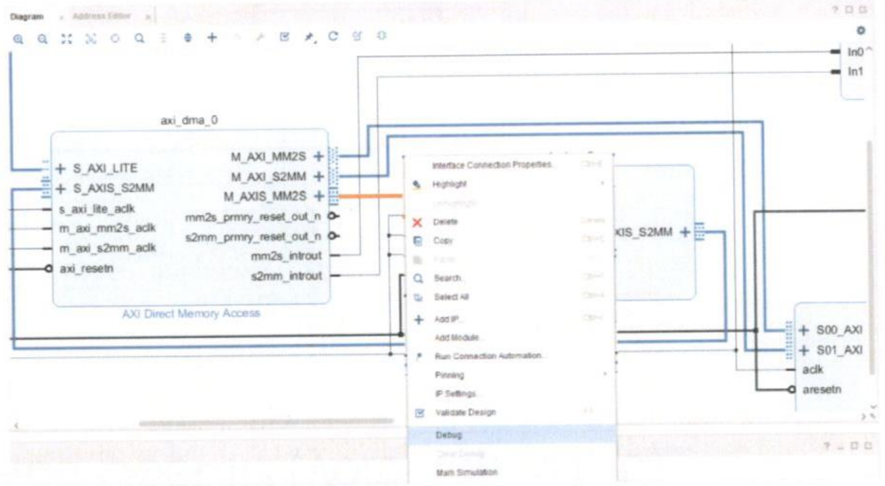

Diagram
Address Editor
axi_dma_0
S_AXI_LITE
S_AXIS_S2MM
s_axi_lite_aclk
m_axi_mm2s_aclk
m_axi_s2mm_aclk
axi_resetn
M_AXI_MM2S
M_AXI_S2MM
M_AXIS_MM2S
mm2s_prmry_reset_out_n
s2mm_prmry_reset_out_n
mm2s_introut
s2mm_introut
AXI Direct Memory Access
Interface Connection Properties...
Highlight
Delete
Copy
Search
Select All
Add IP
Add Module
Run Connection Automation
Pinning
IP Settings
Validate Design
Debug
Mark Simulation
XIS_S2MM
In0
In1
S00_AXI
S01_AXI
aclk
aresetn