A 1.4GHz 0.12pJ 4-bit Absolute-Value Detector for use in Neural Spike Sorting

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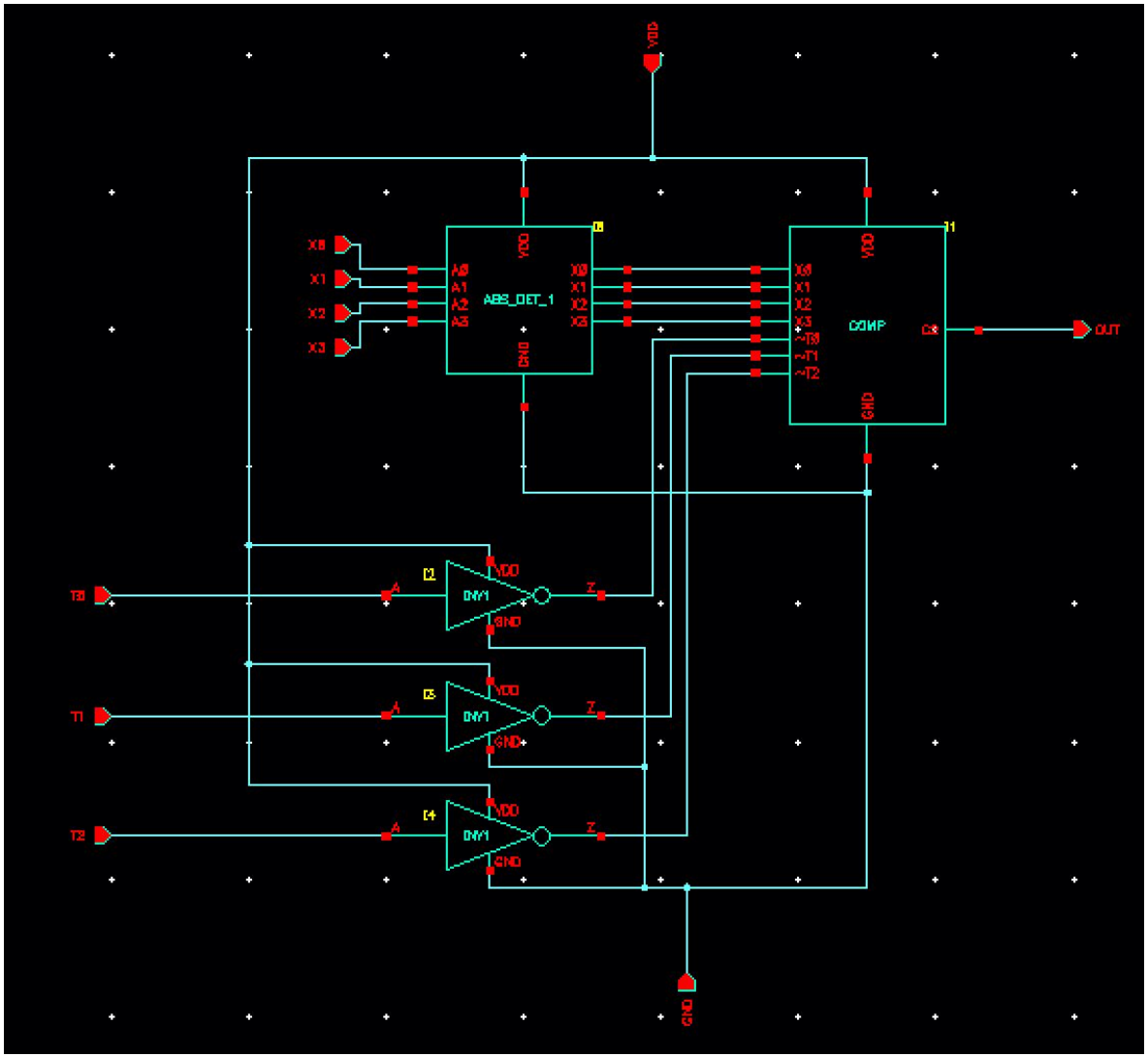
Design Summary

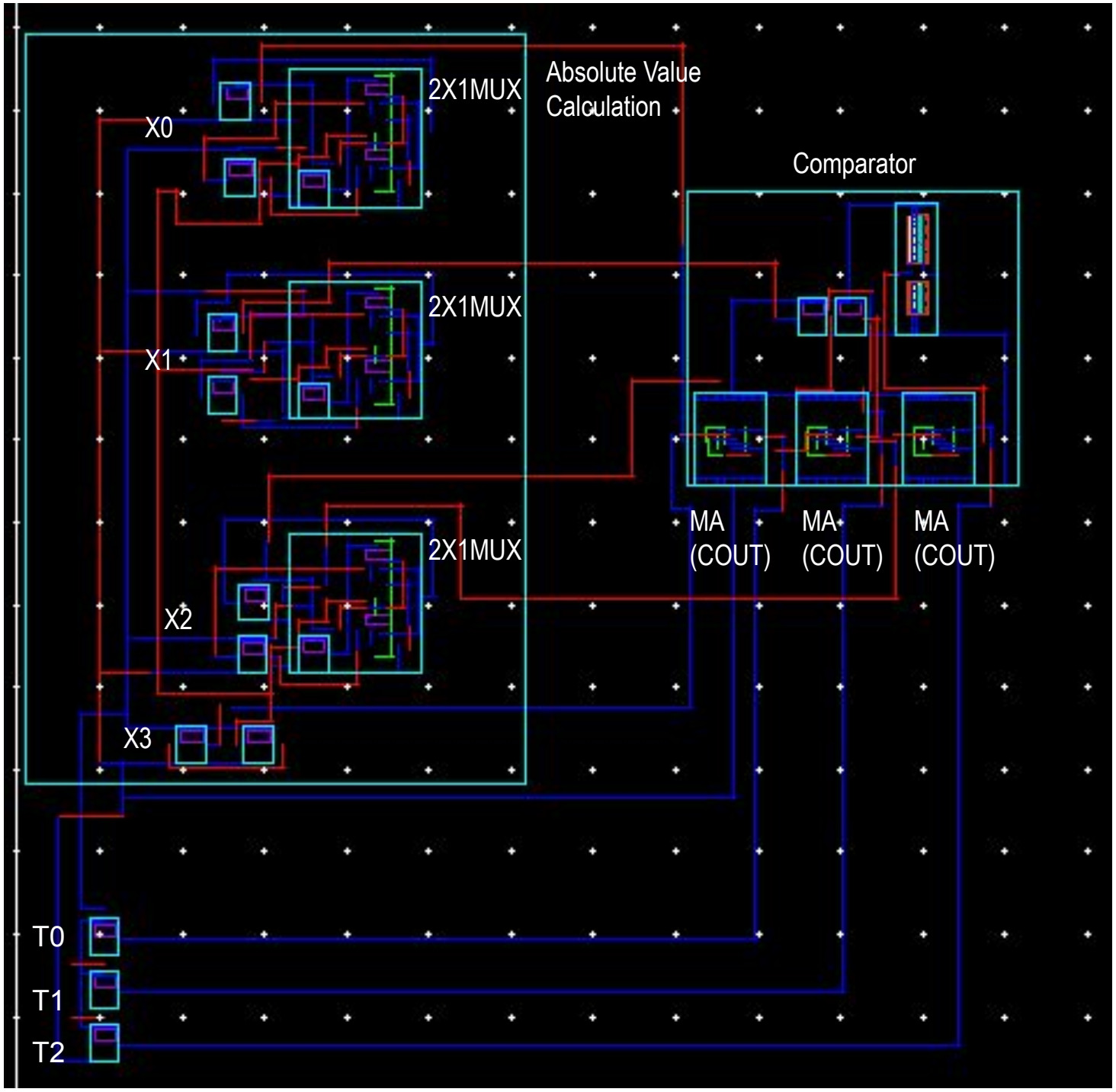
- **Mixed design with PTL and Static CMOS**
  - Reason: Minimum # of transistors, optimizes delay-energy metric
- **Stage 1 (absolute value calculation):**
  - |X| + ~T = |X| -T -1 ← nonnegative if |X| > T
  - MUX selector is X_3; determines whether X is positive or negative then |X| is sent to stage 2
  - T is inverted and sent to stage 2
- **Stage 2 (comparator):**
  - Optimized ripple-carry adder carry-out logic (using inversion property) with mirror adders to calculate 2^{nd}-last C_{out} (i.e. C_2)
  - $C_{in} = X_3$
  - C_2 = 1 --> |X| > T
  - C_2 = 0 --> |X| <= T

Sizing and Optimization

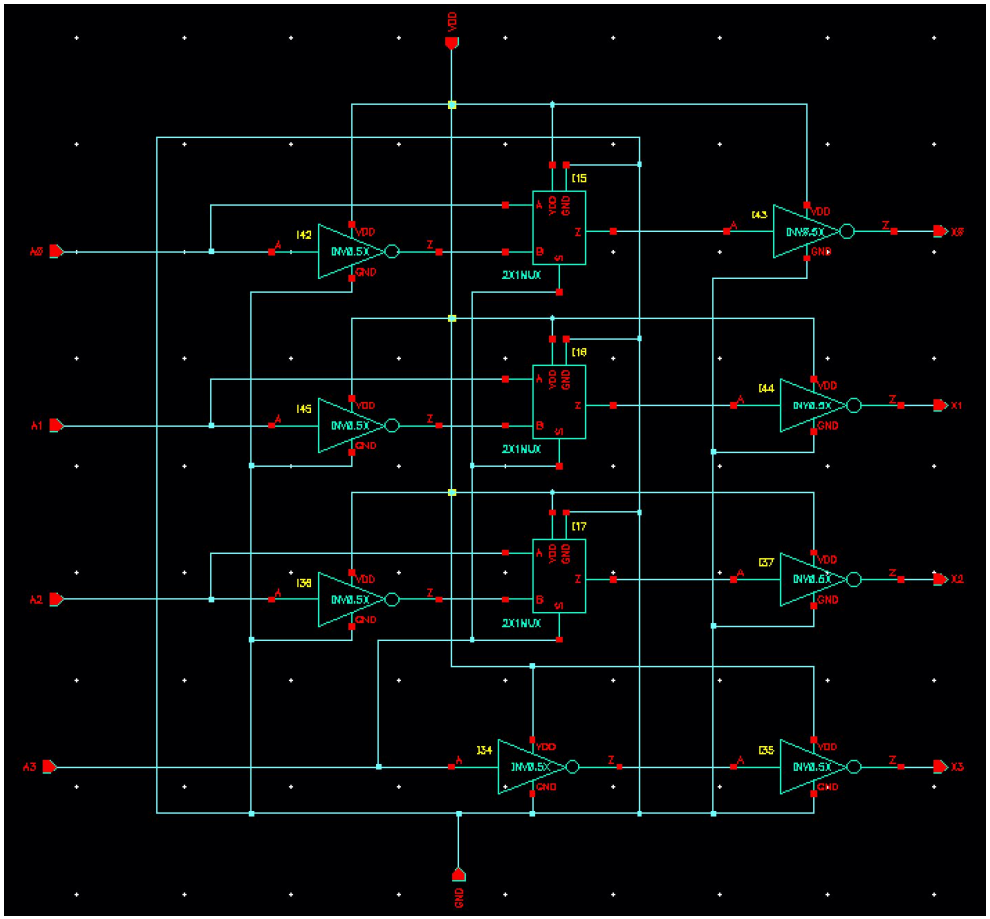
- Unit inverter: w_p = 650 nm, w_n = 430 nm
- 0.5x inverter: w_p = 325 nm, w_n = 215 nm
- 4x inverter: w_p = 2.6 µm, w_n = 1.72 µm
- We initially tried logical effort sizing and using 0.5x inverters in the critical paths, 1x inverters in the non-critical paths and 4x inverter closest to the load
- We later found that using 0.5x inverters everywhere and a 4x inverter closest to output (to invert C_2 from last mirror adder) offers the best balance of minimized delay and energy

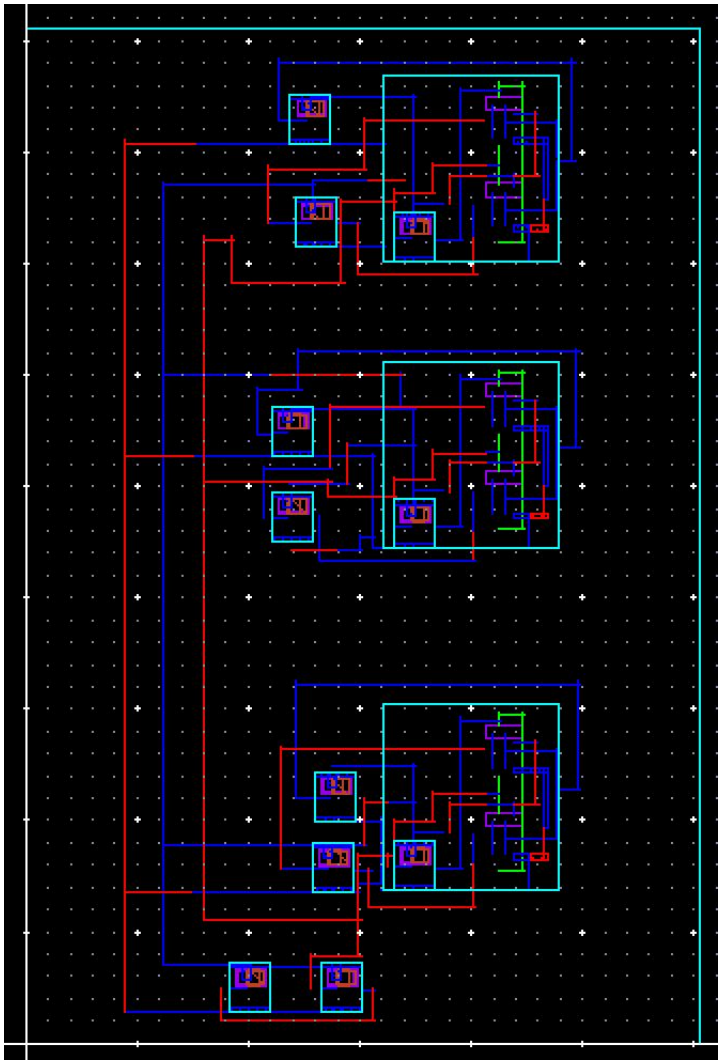
Full Absolute Value Detector



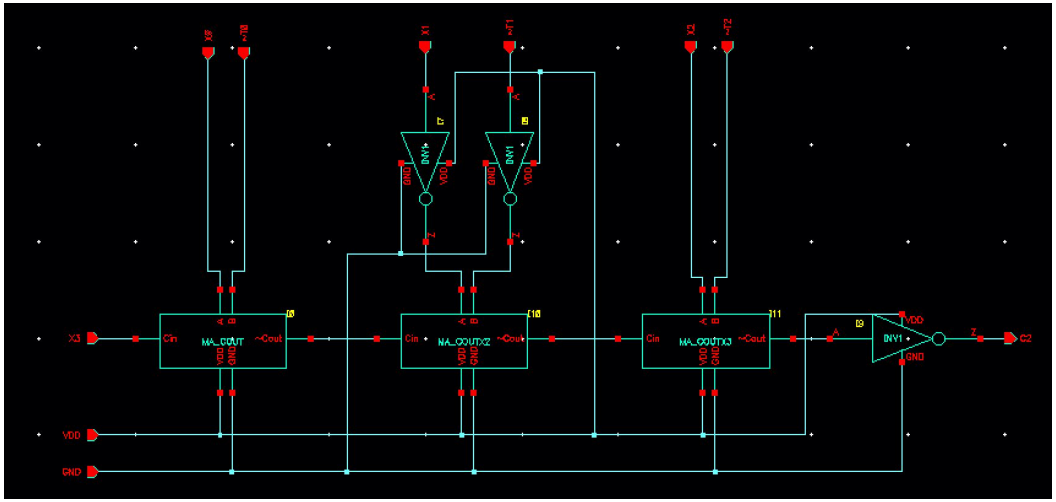

Absolute Value
Calculation
2X1MUX
2X1MUX
2X1MUX
X0
X1
X2
X3
Comparator
MA
(COUT)
MA
(COUT)
MA
(COUT)
T0
T1
T2

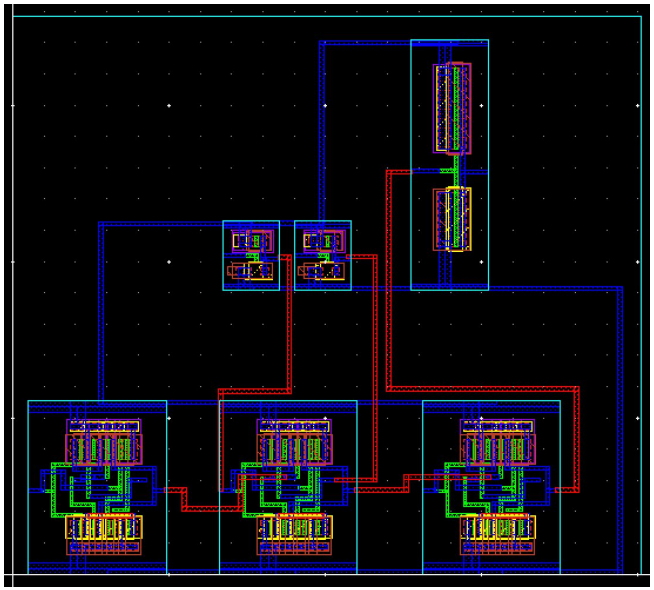
Stage 1: Absolute Value Calculation



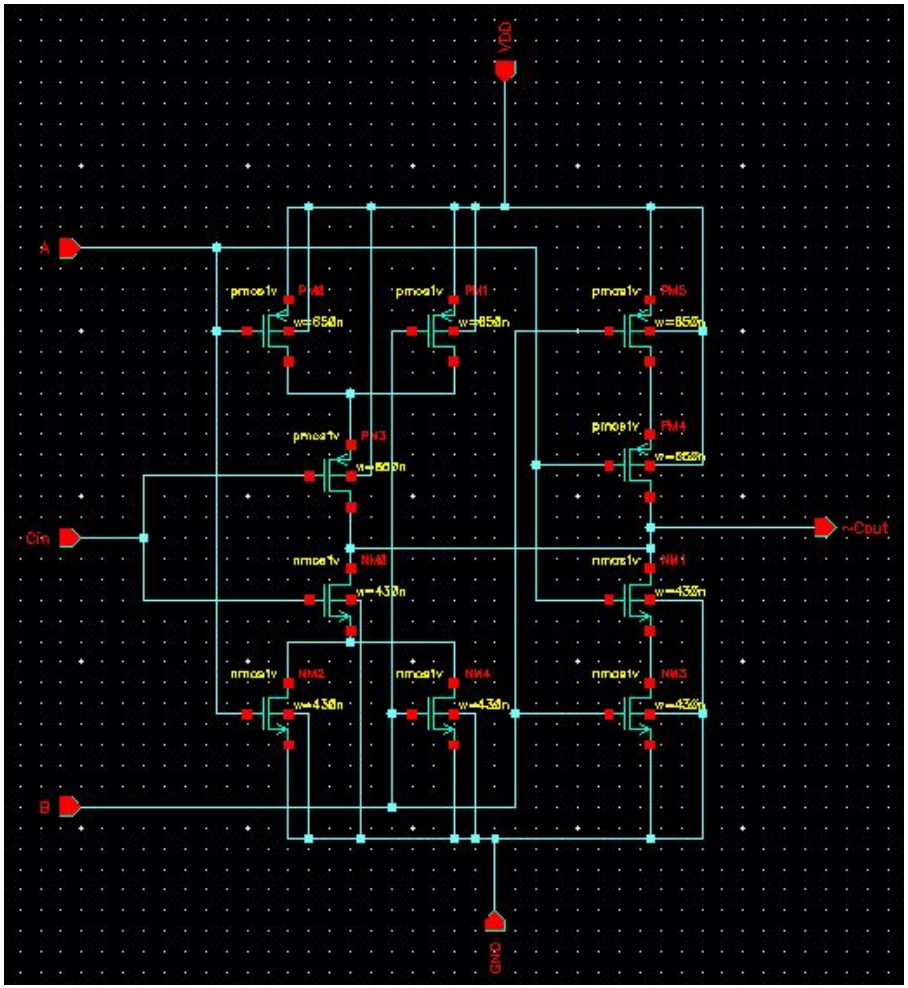


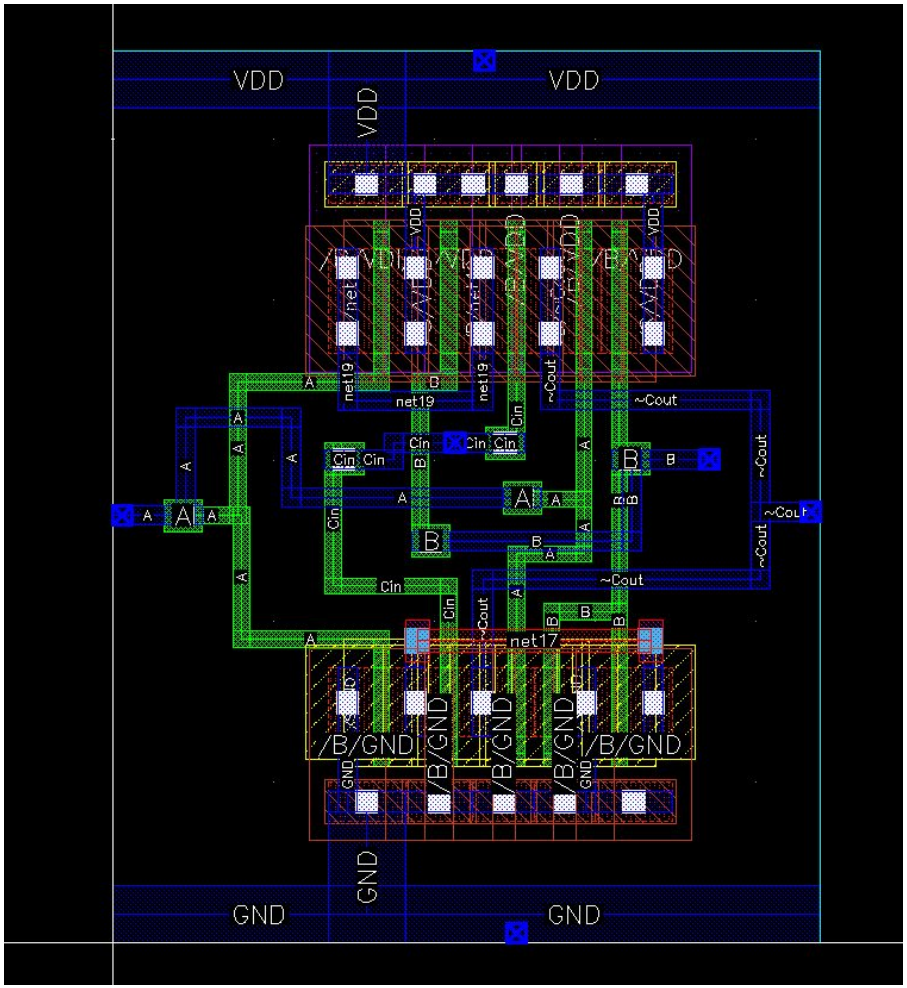
Stage 2: Comparator



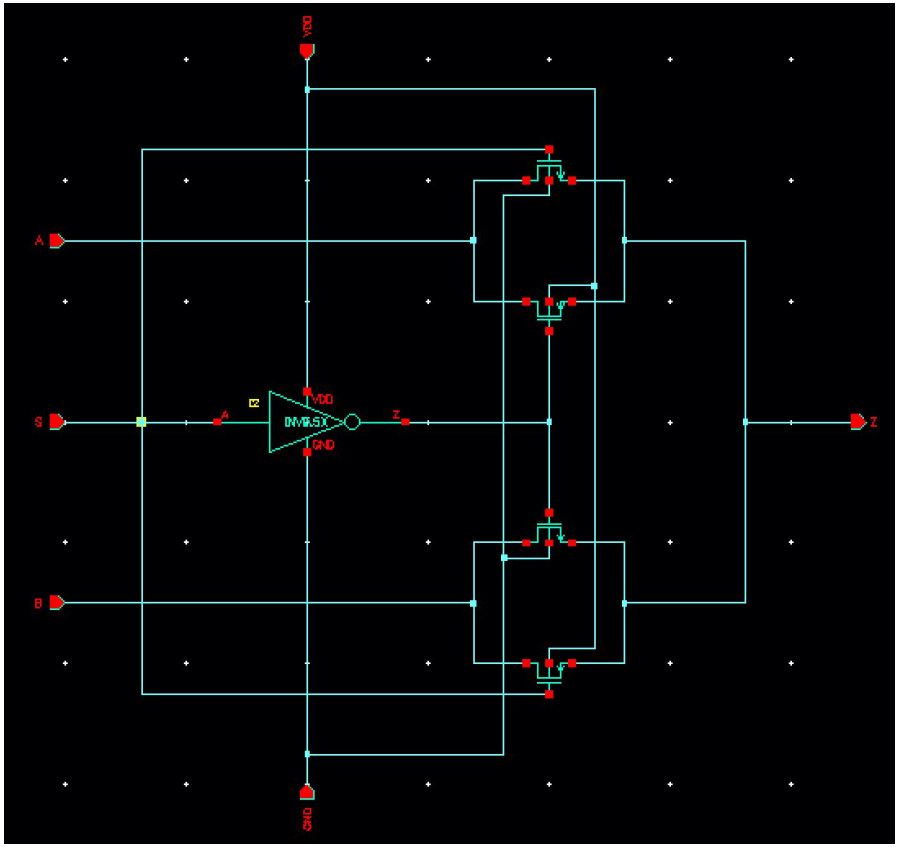


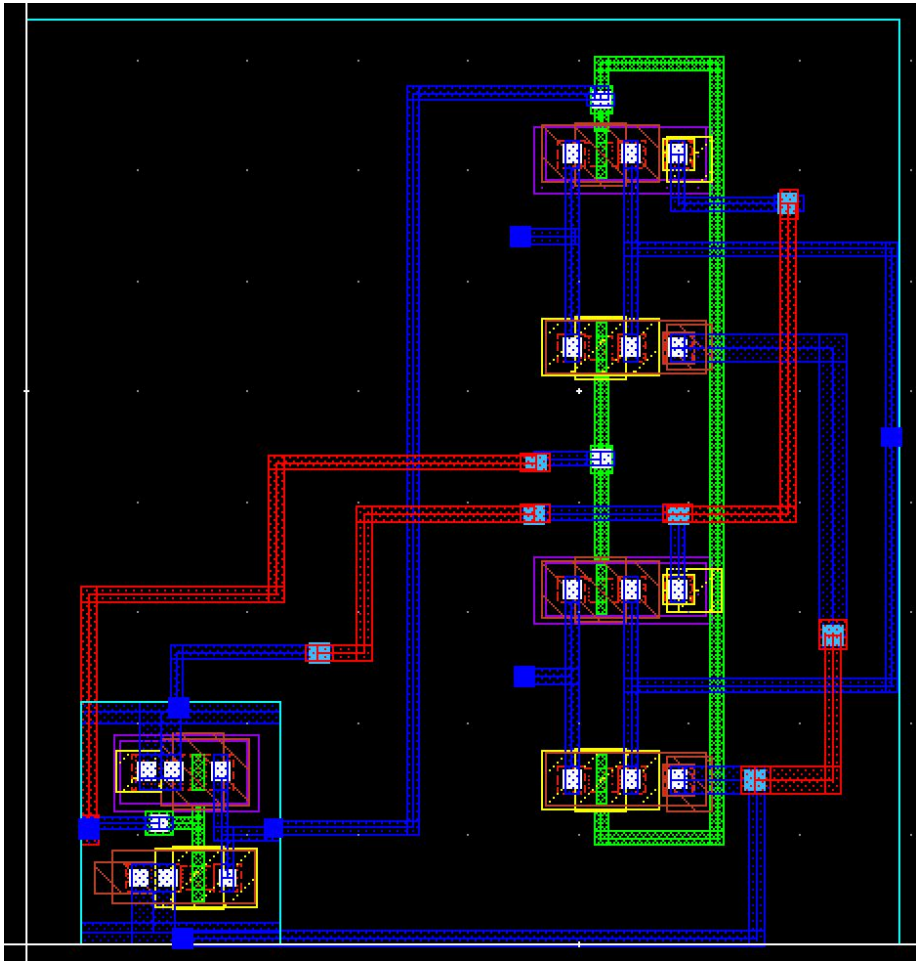
Mirror Adder (carryout only)



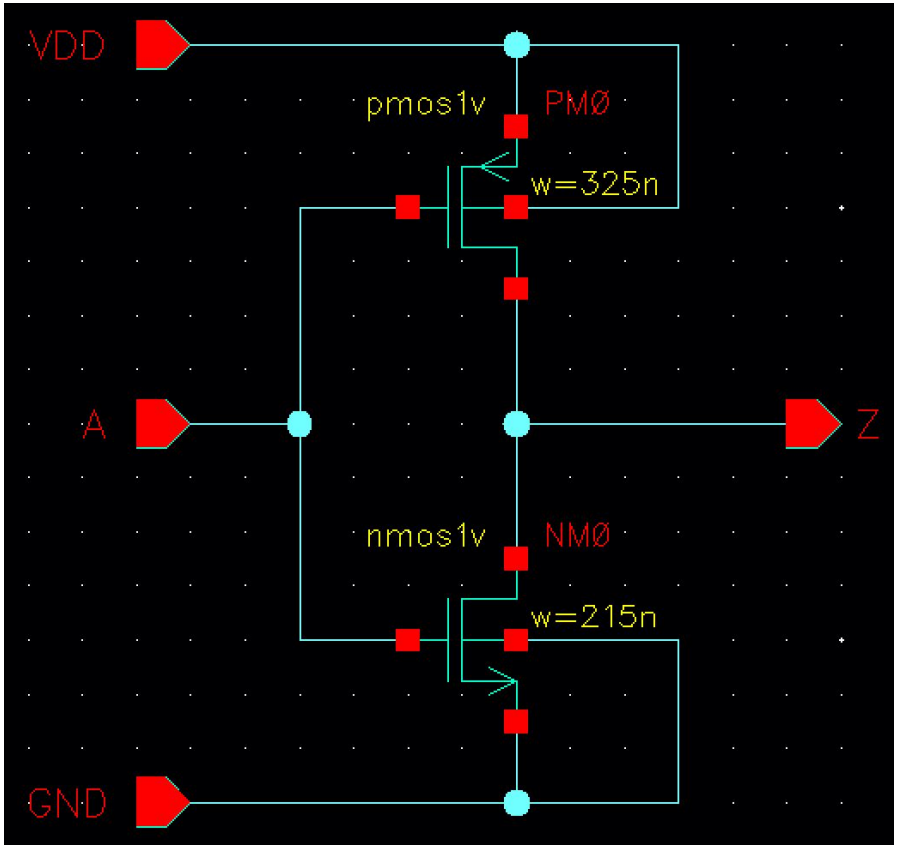


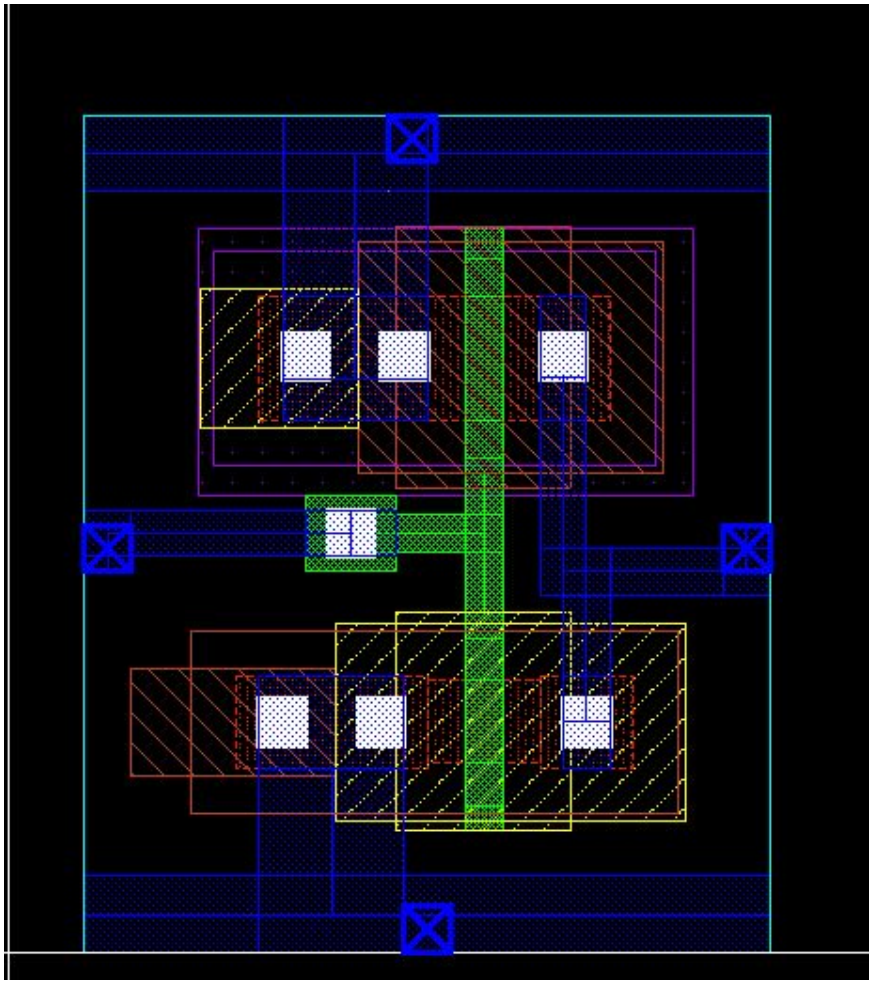
Multiplexor (2X1MUX)



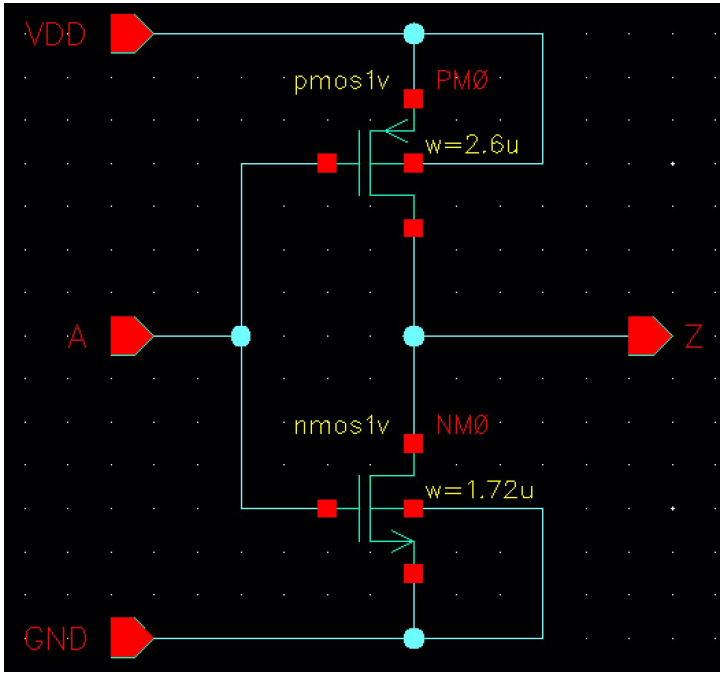


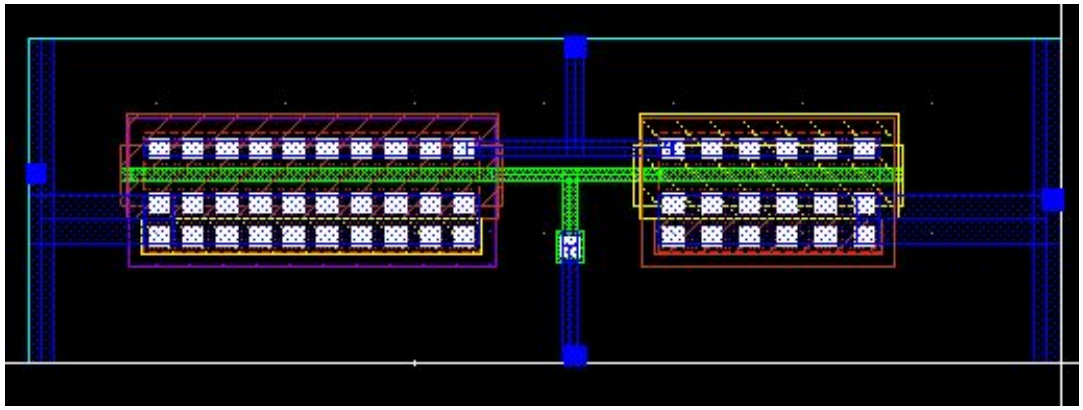
0.5X Inverter





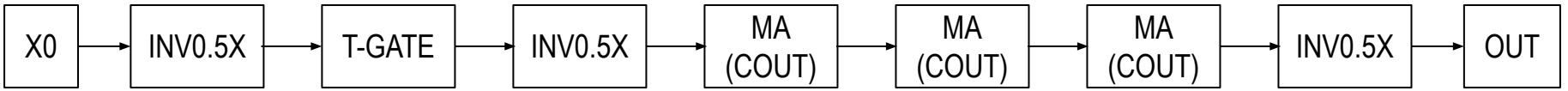
4X Inverter



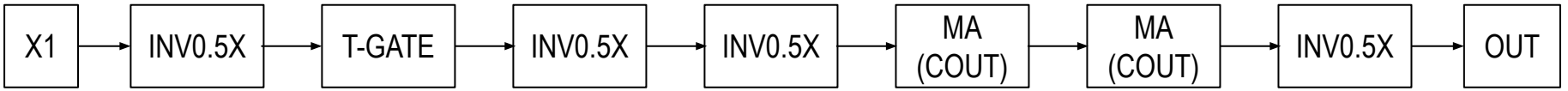


Critical Path, Delay and Energy

- The input vectors associated with the 3 worst delay paths are X_0, X_1 and X_3
  - $t_{critical\_X0} = 2t_{INV\_0.5} + t_{TG} + 3t_{MA\_COUT} + t_{INV\_4}$

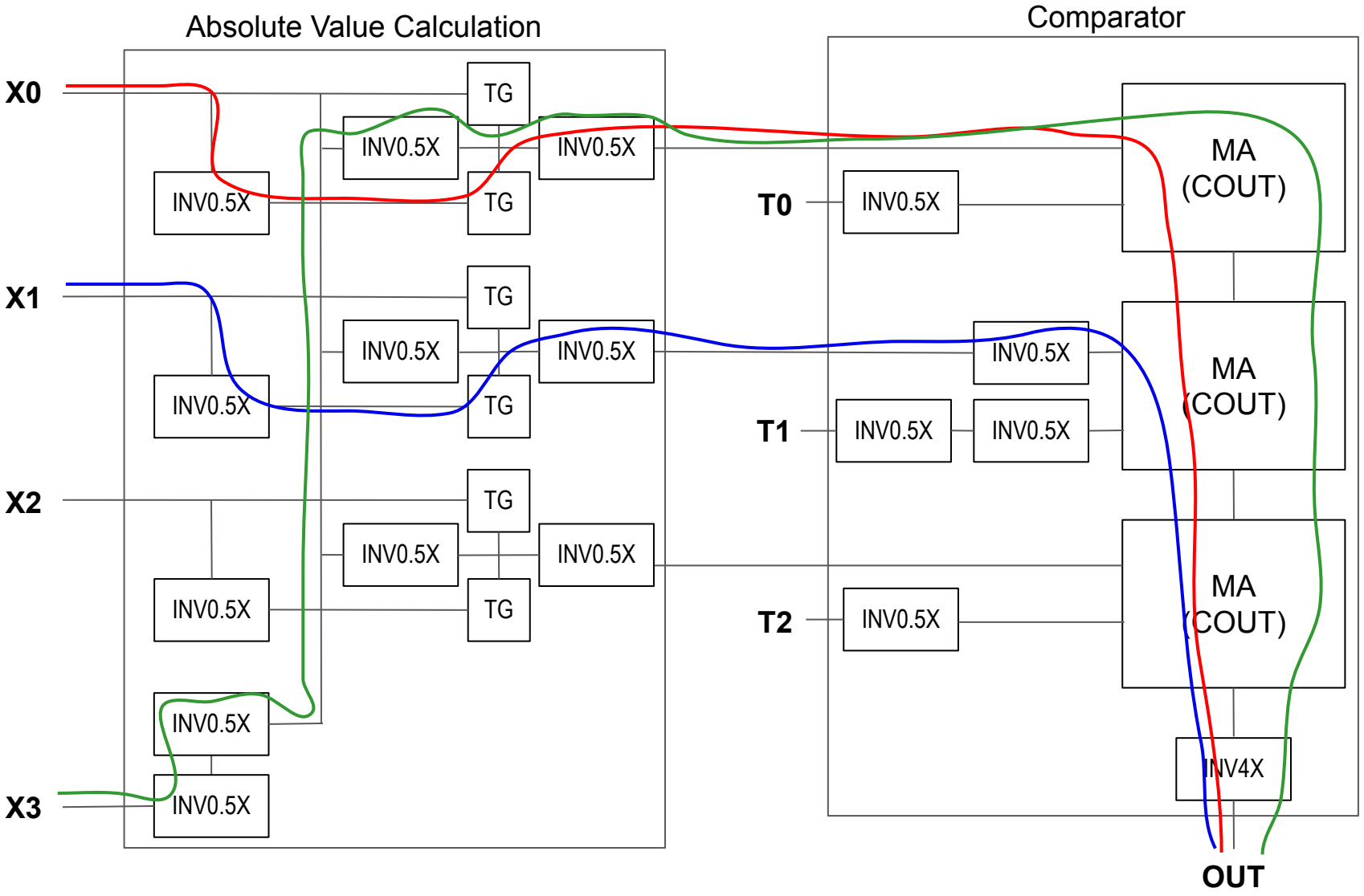


  - $t_{critical\_X1} = 3t_{INV\_0.5} + t_{TG} + 2t_{MA\_COUT} + t_{INV\_4}$



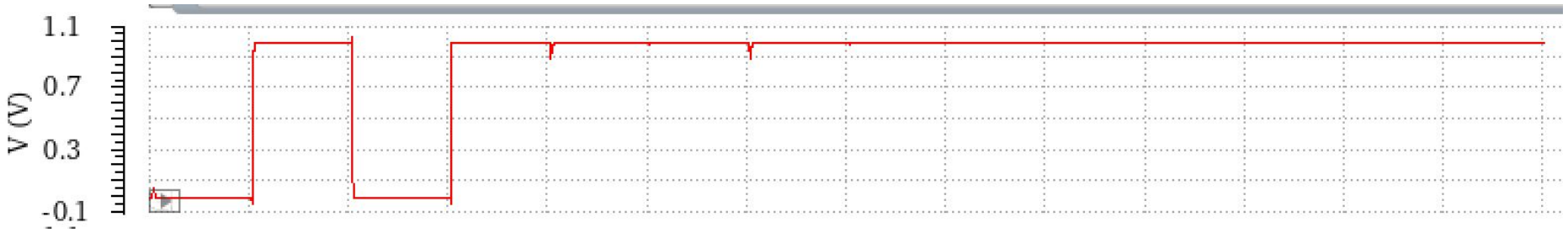
  - $t_{critical\_X3} = 4t_{INV\_0.5} + 3t_{MA\_COUT} + t_{INV\_4}$

- Final V_{DD} (post-layout): **674 mV**
- Minimum energy (post-layout): **205.15 fJ**
- **NOTE:** Critical paths used line up with critical paths given in original testbench


Absolute Value Calculation
Comparator
X0
X1
X2
X3
T0
T1
T2
TG
INV0.5X
INV4X
MA
(COUT)
OUT

Schematic	Layout size	Energy	Verification
V_{DD} = 571 mV $t_{p\_X(0)\rightarrow OUT}$ = 685.2 ps $t_{p\_X(1)\rightarrow OUT}$ = 663.4 ps $t_{p\_X(2)\rightarrow OUT}$ = 570.9 ps	X= 69.73 µm Y= 77.4 µm A = 5397.1 μm^2 Aspect Ratio = 1.11	Sch E = 119.3 fJ Layout E = 205.15 fJ V_{DD-S} = 571 mV V_{DD-L} = 674 mV	Func: Y DRC: Y LVS: Y

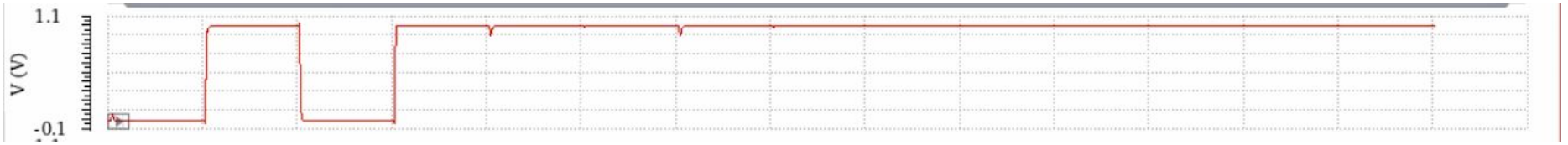
Most critical path: X_0 (Schematic)



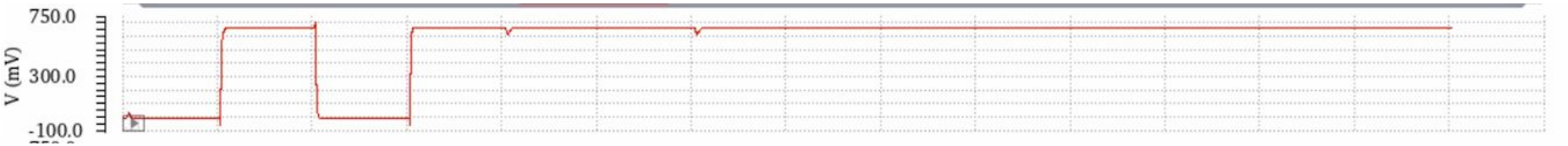
V_{DD} = 1 V

V_{DD} = 571 mV

Most critical path: X_0 (Layout)



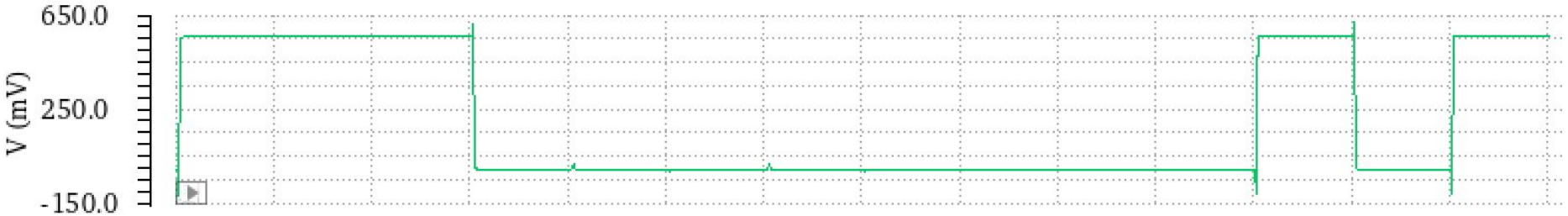
V_{DD} = 1 V



V_{DD} = 674 mV

2nd most critical path: X_1 (Schematic)

V_{DD} = 1 V



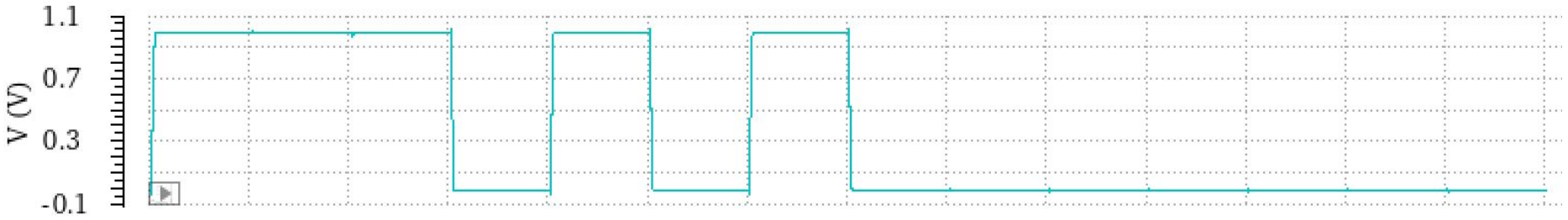
V_{DD} = 571 mV

2nd most critical path: X_1 (Layout)

V_{DD} = 1 V

V_{DD} = 674 mV

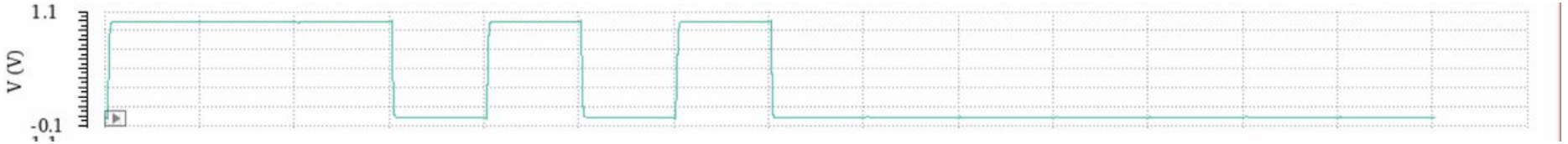
3rd most critical path: X_3 (Schematic)



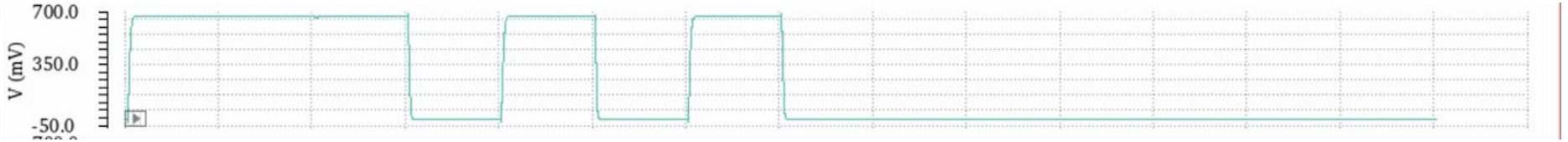
V_{DD} = 1 V

V_{DD} = 571 mV

3rd most critical path: X_3 (Layout)

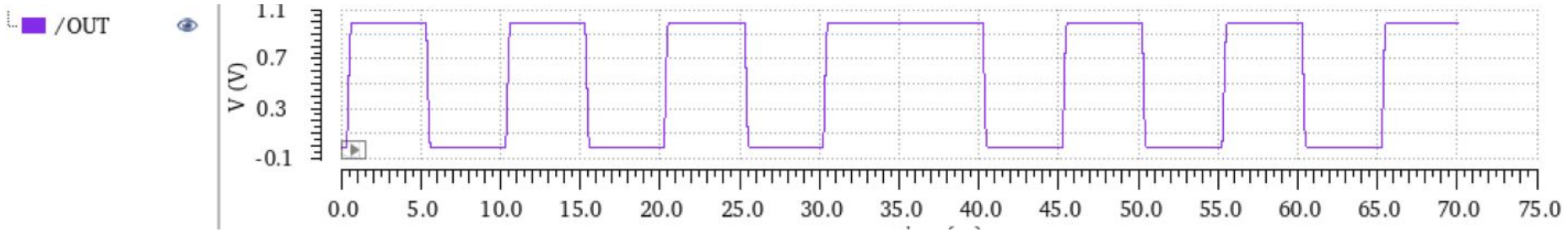


V_{DD} = 1 V

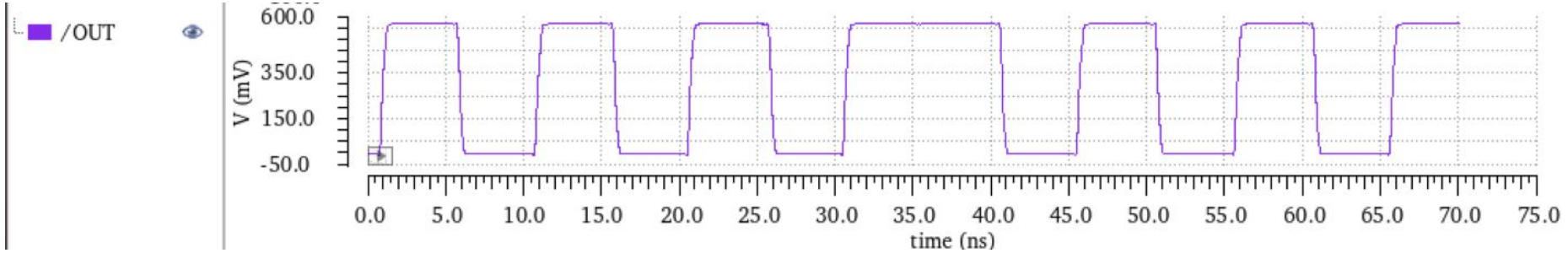


V_{DD} = 674 mV

Output (Schematic)

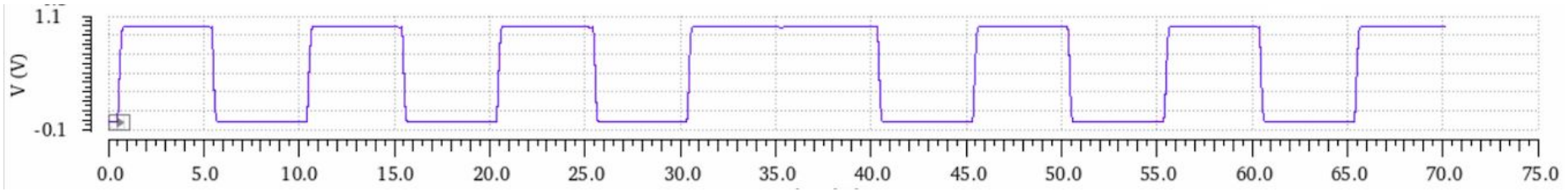


V_{DD} = 1 V

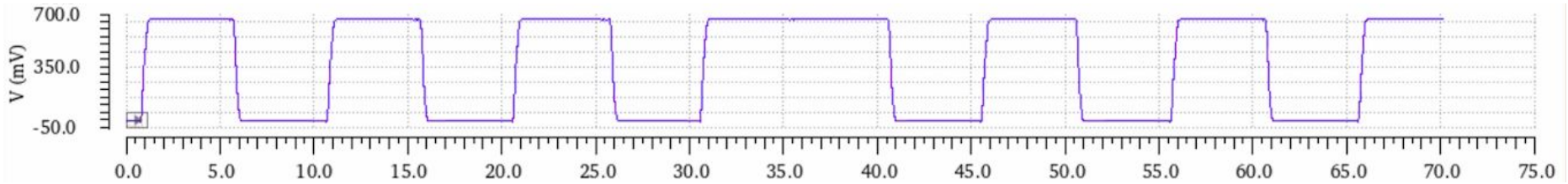


V_{DD} = 571 mV

Output (Layout)

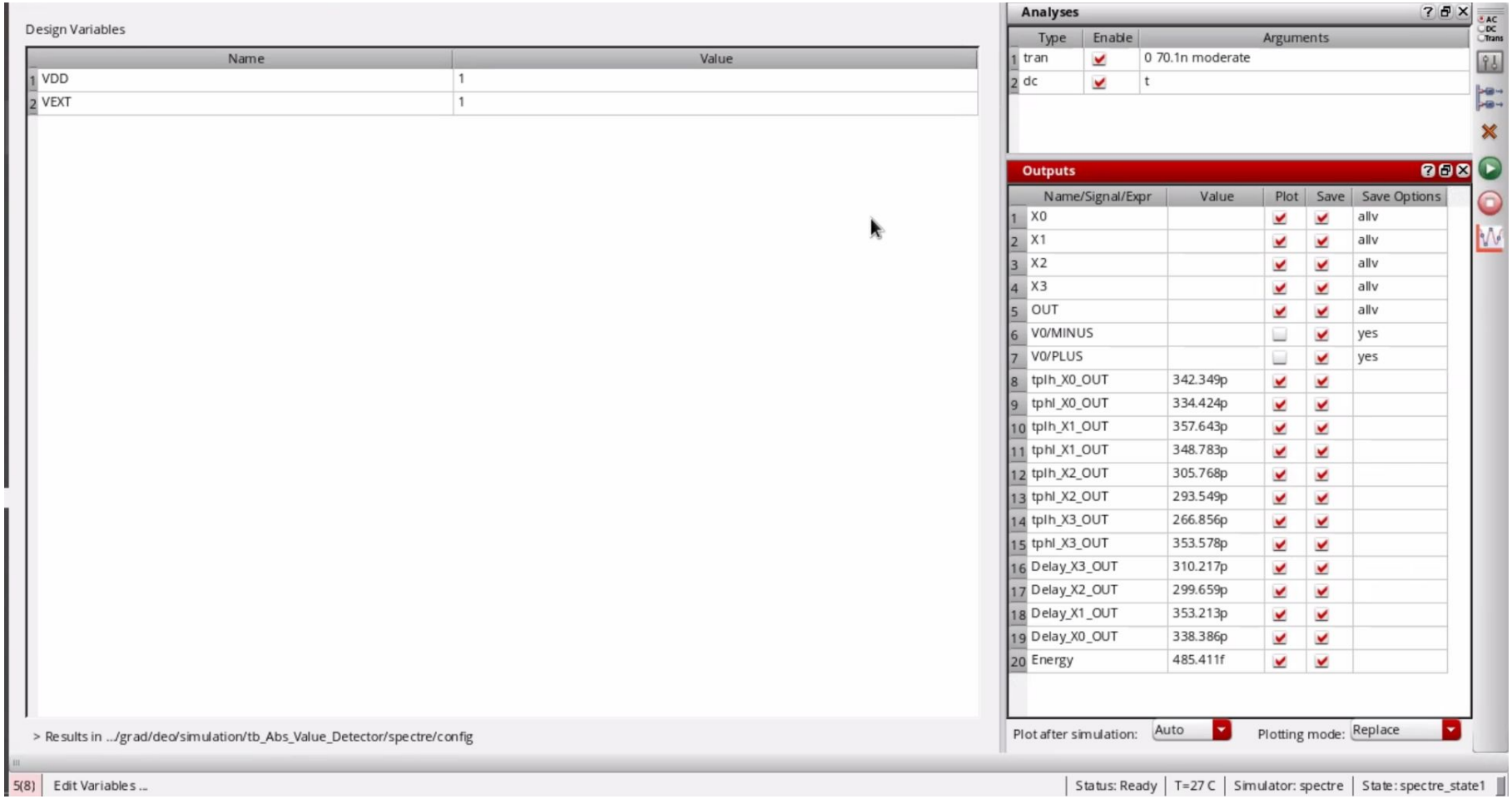


V_{DD} = 1 V

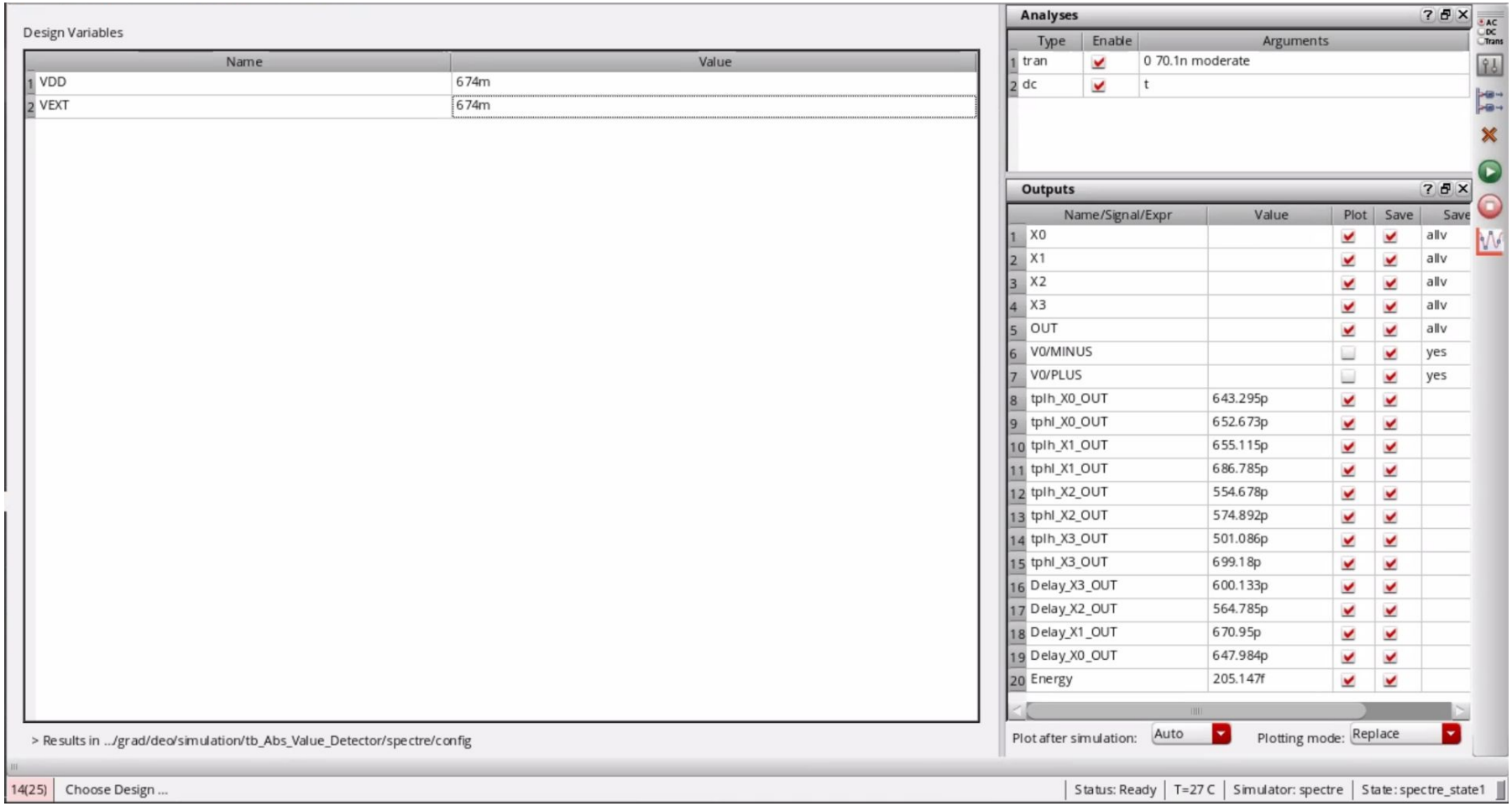


V_{DD} = 674 mV

Post-Layout Outputs for VDD = 1 V



Post-Layout Outputs for VDD = 674 mV



Design Variables

	Name	Value
1	VDD	674m
2	VEXT	674m

> Results in .../grad/deo/simulation/tb_Abs_Value_Detector/spectre/config

Analyses

	Type	Enable	Arguments
1	tran	☑	0 70.1n moderate
2	dc	☑	t

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save
1	X0		☑	☑	allv
2	X1		☑	☑	allv
3	X2		☑	☑	allv
4	X3		☑	☑	allv
5	OUT		☑	☑	allv
6	V0/MINUS		☐	☑	yes
7	V0/PLUS		☐	☑	yes
8	tplh_X0_OUT	643.295p	☑	☑	
9	tphl_X0_OUT	652.673p	☑	☑	
10	tplh_X1_OUT	655.115p	☑	☑	
11	tphl_X1_OUT	686.785p	☑	☑	
12	tplh_X2_OUT	554.678p	☑	☑	
13	tphl_X2_OUT	574.892p	☑	☑	
14	tplh_X3_OUT	501.086p	☑	☑	
15	tphl_X3_OUT	699.18p	☑	☑	
16	Delay_X3_OUT	600.133p	☑	☑	
17	Delay_X2_OUT	564.785p	☑	☑	
18	Delay_X1_OUT	670.95p	☑	☑	
19	Delay_X0_OUT	647.984p	☑	☑	
20	Energy	205.147f	☑	☑	

Plot after simulation: Auto Plotting mode: Replace

14(25) | Choose Design ... | Status: Ready | T=27 C | Simulator: spectre | State: spectre_state1

Delay and Energy

Schematic		Layout	
V_{DD} = 1 V E = 403.12 fJ	V_{DD} = 571 mV E = 119.3 fJ	V_{DD} = 1 V E = 485.41 fJ	V_{DD} = 674 mV E = 205.15 fJ
$t_{p\_X(0)\rightarrow OUT}$ = 244.3 ps $t_{plh\_X(0)->OUT}$ = 246.5 ps $t_{phl\_X(0)->OUT}$ = 242.0 ps	$t_{p\_X(0)\rightarrow OUT}$ = 685.2 ps $t_{plh\_X(0)->OUT}$ = 670.5 ps $t_{phl\_X(0)->OUT}$ = 699.9 ps	$t_{p\_X(0)\rightarrow OUT}$ = 338.4 ps $t_{plh\_X(0)->OUT}$ = 342.3 ps $t_{phl\_X(0)->OUT}$ = 334.4 ps	$t_{p\_X(0)\rightarrow OUT}$ = 648.0 ps $t_{plh\_X(0)->OUT}$ = 643.3 ps $t_{phl\_X(0)->OUT}$ = 652.7 ps
$t_{p\_X(1)\rightarrow OUT}$ = 240.4 ps $t_{plh\_X(1)->OUT}$ = 243.9 ps $t_{phl\_X(1)->OUT}$ = 236.9 ps	$t_{p\_X(1)\rightarrow OUT}$ = 663.4 ps $t_{plh\_X(1)->OUT}$ = 637.6 ps $t_{phl\_X(1)->OUT}$ = 689.2 ps	$t_{p\_X(1)\rightarrow OUT}$ = 353.2 ps $t_{plh\_X(1)->OUT}$ = 357.6 ps $t_{phl\_X(1)->OUT}$ = 348.8 ps	$t_{p\_X(1)\rightarrow OUT}$ = 671.0 ps $t_{plh\_X(1)->OUT}$ = 655.1 ps $t_{phl\_X(1)->OUT}$ = 686.8 ps
$t_{p\_X(3)\rightarrow OUT}$ = 203.3 ps $t_{plh\_X(3)->OUT}$ = 174.1 ps $t_{phl\_X(3)->OUT}$ = 232.5 ps	$t_{p\_X(3)\rightarrow OUT}$ = 570.9 ps $t_{plh\_X(3)->OUT}$ = 463.3 ps $t_{phl\_X(3)->OUT}$ = 678.5 ps	$t_{p\_X(3)\rightarrow OUT}$ = 310.2 ps $t_{plh\_X(3)->OUT}$ = 266.9 ps $t_{phl\_X(3)->OUT}$ = 353.6 ps	$t_{p\_X(3)\rightarrow OUT}$ = 600.1 ps $t_{plh\_X(3)->OUT}$ = 501.1 ps $t_{phl\_X(3)->OUT}$ = 699.2 ps

Discussion