### Fabrication and characterization of Fano nanobeam cavities

Based on the parameters developed in section 2.1.2, we performed the device fabrication with mask generated using python package. The fabrication process introduced in this part is used throughout the manuscript which is shown Figure 32. The fabrication of SOI chip can be separated in several steps in which most of these fabrication steps have been carried out by Mr. Xavier Le Roux from the C2N laboratory.

**Cleaning**; The silicon on insulator (SOI) wafer can be first cleaned using NH4F solution for removing the surface oxide created in the growing process. This step can provide a good adhesion with the silicon and the photo resist. Following this, acetone, isopropanol is then used step-by-step, with the ultra-sonic machine to clean the surface of silicon. Sometimes there’s some carbon contaminant stuck on the silicon surface which cannot be removed by an organic solution. In these cases, a combined solution of [concentrated](javascript:;) [sulfuric](javascript:;) [acid](javascript:;) and [hydrogen](javascript:;) [peroxide](javascript:;) can be considered.

**Spin coating**; after drying the wafer from step one (a) with a hot plate with temperature up to 120 Celsius degrees, the sample can be transferred to the spin coater for covering it with photo-resist. For different purposes and design, two kinds of photoresist can be used, i.e. a positive resist or a negative resist. A positive resist (e.g. ZEP series, PMMA) is exposed to dedicated light source and removed in a later developing process, while the exposed parts of negative resist (e.g. Ma-N 24xx series, HSQ) are the remaining areas after the developing process. After the spin coating, the sample with hundreds of nm of photoresist (the thickness of the photoresist can be easily controlled by the rotation rate of the spin coater) on top of the surface is put on the hot plate for pre-baking. In this step, the photo resist is dried out and strengthened.

**Electron-beam Lithography**; taking the sample from spin coating, an electronic lithography machine is used to transfer the pattern that were generated from Python GDS tool, as shown in Figure 32 (c) and (d).

**Developing**; the sample from exposure is soaked into the developing solution for the pattern recover (e). The solution used is chosen according to the polarity of the photoresist. Following this, the sample is again put on the hot plate for drying out.

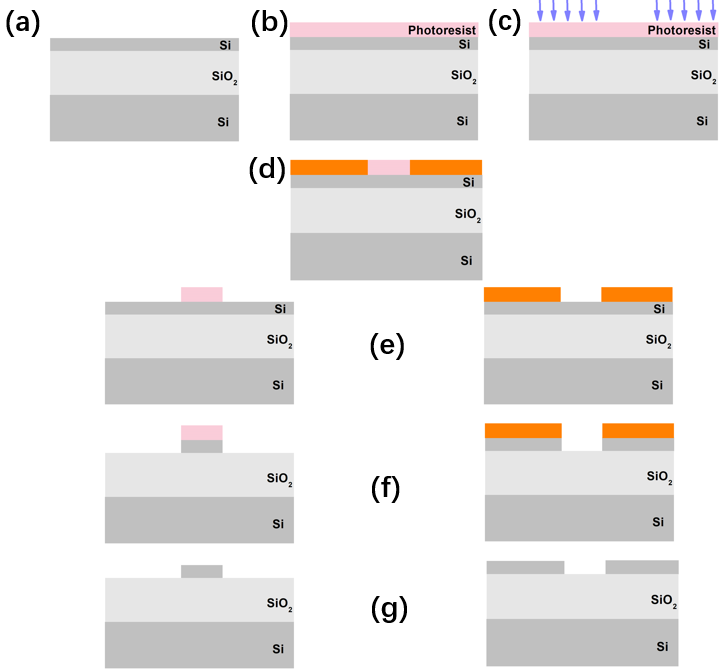
**Etching**; sample is transferred to the chamber of Induced Couple Plasmas (ICP) etching machine for pattern transfer (f). In this process, a dry run with pure oxygen is preferred before etching the sample, which can clean the chamber and stabilize the etching rate. With conductive [silicone](javascript:;) [grease](javascript:;), sample is stuck on the spacer for thermal dissipation. The gas used for silicon etching is C4F8 and SF6 while the recipe for silica and silicon nitride CF4 and CH3.

**Postprocess**; after etching, the sample is rinsed in acetone with the assistance of shaking table for roughly removing the photoresist. Then, it is followed by the fine cleaning of combined solution of [concentrated](javascript:;) [sulfuric](javascript:;) [acid](javascript:;) and [hydrogen](javascript:;) [peroxide](javascript:;) (g). Once cleaning is finished, sample can be put on the hot plate again for dehydration.

**Surface polishing**; waveguide roughness can be created during all these processes above, including patterning roughness, transfer roughness or etching roughness. To polish the surface of structures, samples are put into the high-temperature oven to generate sacrificed oxide which can be removed by rinsing fabricated samples in diluted [hydrofluoric](javascript:;) [acid](javascript:;).

**Overlay**; In cases that multi-step patterning is needed. The pattern can be again transferred to the sample by performing alignment to the labeled structures which are formerly generated during the first etching step. Then, spin coating, exposure and etching can be repeated as described above.

**Deposition**; In cases that external materials are expected (e.g. top silica cladding), we can use a plasma enhanced chemical vapor deposition (PECVD) machine for depositing amorphous material. In terms of metal (e.g. for electrode purpose), magneto sputtering and evaporation deposition technologies can be used, followed by the lift-off method.



**Figure 32.** Schematic of our silicon fabrication process flow. (a) Cleaning. (b) Spin coating. (c) Lithography. (d) Post-baking. (e) Developing. (f) Etching. (g) Post-cleaning.

A silicon-on-insulator (SOI) wafer with 220nm silicon thickness was used for fabrication. Since photonic waveguides have a high index contrast with the surroundings, the most convenient method to interface the input fiber connected with light source and the fabricated sample appeared to be the use of grating couplers, taking advantages of the efficient radiation [151, 152] A scanning electron microscope (SEM) of our fabricated grating coupler is presented in Figure 32. Since the cross-section of a single-mode on-chip silicon photonic waveguide width is usually less than 200 or 300 nm, optical waveguides are needed first to be tapered from their narrow cross-section to the larger grating one in order to interact with the grating corrugation. A simpler design to shorten the taper length is to directly combine the taper and the grating as shown in Figure 33, which is widely stated the “focusing grating coupler”.



**Figure 33.** Scanning electron microscopic image of one of our fabricated focusing grating coupler using our design and fabrication process.

With such a focusing coupler, the sample can be further considered for optical characterizations. Typical experimental conditions and optical benches are shown in Figures 34, 35, and 36. In Figure 34, a tunable/broadband coherent light source (Yenista TUNICS, operating in the 1260-1640nm wavelength range), a polarization controller, a spectrometer (Yokogawa, AQ 637x series), a power detector (Yenista CT400), and a source meter (Keithley 24xx series) are used to characterize the sample transmission. One practical picture of handling the fiber is shown in Figure 35. In the zoom-in picture of Figure 35 (b), the fiber is almost vertically placed (10-30 degrees, according to the design of the grating coupler) and placed to inject/extract the light to/from the grating coupler. Such a slight tilted angle is normally requested since a perfect vertical coupling configuration can lead to the sacrifice of half on the input energy to the backward waveguide propagation direction. With this method, coupling efficiency can be achieved experimentally up to nearly 50%), which is definitely enough for the proper characterization of the structures.