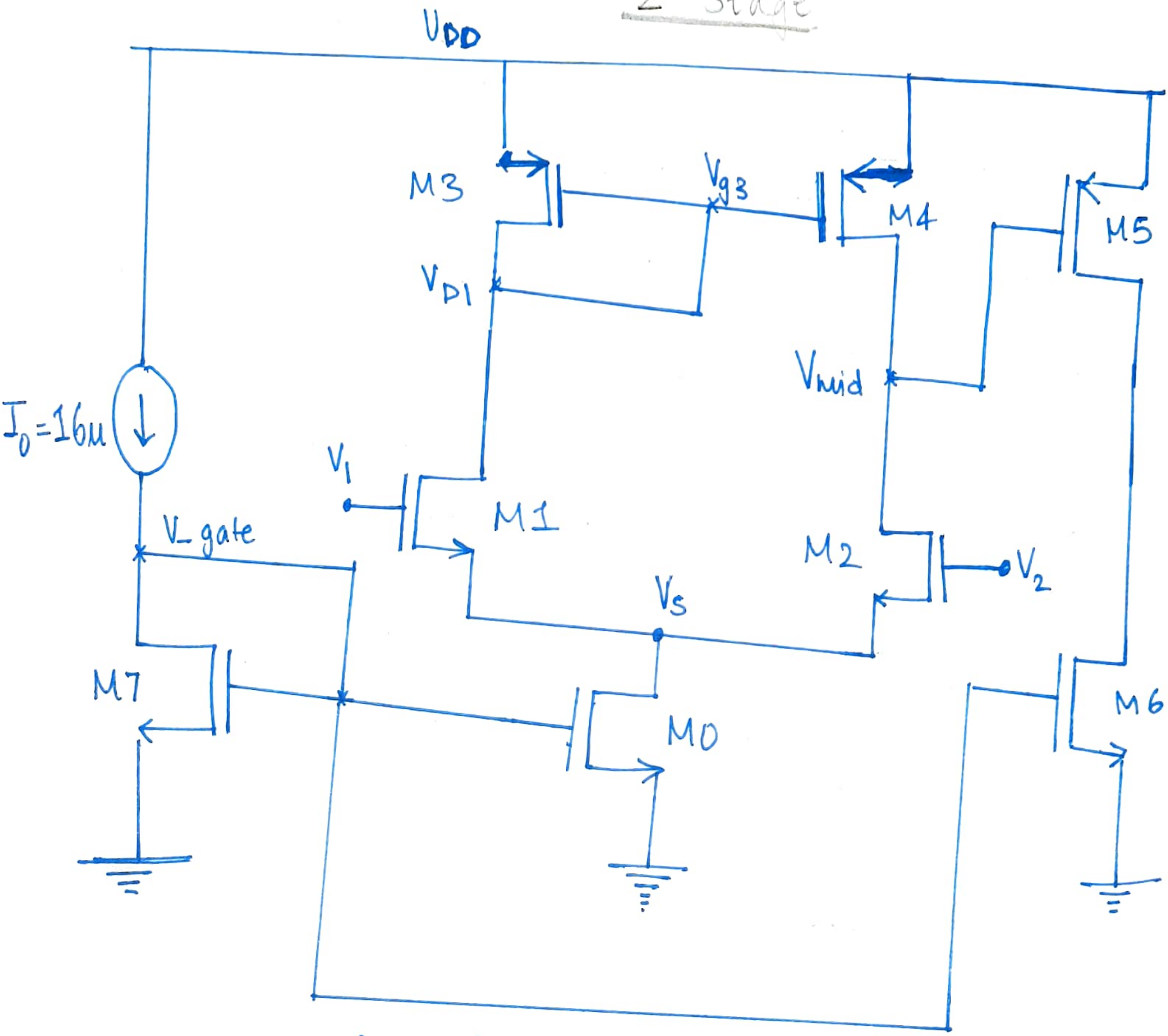
EE206 : OTA-Design Assignment

- Name :→ PRANAV VISHAL DESHMUKH
- Roll Number :→ 23010273

- CIRCUIT-DIAGRAM :→

"OPEN LOOP"
2-Stage



V_2 : AC Signal of input (0.1mV amplitude) + 0.9V DC bias

V_1 : 0.9V DC bias

CALCULATIONS

Let us begin the design of the OTA from the current mirror's transistor M7. Assuming an overdrive of 0.2V for M_7 and $I_{ref} = 16u$.

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_7 (V_{GS} - V_{th})^2$$

plugging in all the values gives us,

$$16 = \frac{1}{2} \times 230 \times \left(\frac{W}{L}\right)_7 \times 0.2^2$$

$$\rightarrow \left(\frac{W}{L}\right)_7 = 3.478$$

Taking $L = 900n$ $\rightarrow \left(\frac{W}{L}\right)_7 \simeq \frac{3200n}{900n} = \frac{3130.434}{900n}$

Since I wanted to provide a constant current source of 160uA for the differential pair, I had chosen to take $I_{ref} = 16uA$ in M7's drain.

Since, M_7 and M_0 have the same overdrive, and M_0 needs to flow 10x more current through it's drain.

$$\left(\frac{W}{L}\right)_0 = \frac{32000n}{900n}$$

Since the current splits in half across the differential pair,

$$(I_D)_{M1} = 80\mu A = (I_D)_{M2}$$

Assuming an overdrive of around 0.1V for M1, (NMOS)

$$80\mu A = \frac{1}{2} \times 230\,\mu A/V^2 \times \left(\frac{W}{L}\right)_1 \times (0.1)^2$$

$$\rightarrow \left(\frac{W}{L}\right)_1 = 69.5652 \rightarrow \left(\frac{W}{L}\right)_1 = \frac{62{,}608.69n}{900n}$$

Approximately, $\left(\frac{W}{L}\right)_1 = \frac{62{,}600n}{900n}$

The same calculations hold true for M2, $\left(\frac{W}{L}\right)_2 = \frac{62{,}600n}{900n}$

For transistor M3 and M4, assume an overdrive of 0.4V,

$$80 = \frac{1}{2} \times 100 \times \left(\frac{W}{L}\right) \times (0.4)^2$$

$$\boxed{\rightarrow \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 10 = \frac{9000n}{900n}}$$

Now that we have determined the $\left(\frac{W}{L}\right)$ ratios for all transistors in the first-stage of the operational transconductance-amplifier, we can check if all are operating in the desired saturation mode.

For M_7, $V_D = V_G \rightarrow \underbrace{V_{DS} > V_{GS} - V_{Th,n}}$

always in saturation given $\underline{V_{GS} > V_{Th,n}}$ $\} \rightarrow$ M7 remains in saturation

and $V_{GS} - V_{Th,n} = 0.2$

$\rightarrow \boxed{V\_gate = 0.57\,V}$

Let us now look at the condition for M0 to remain in saturation,

$\rightarrow V_S > V\_gate - 0 - V_{Th,N}$

$\rightarrow V_S > 0.57 - 0.37$

$\rightarrow \boxed{V_S > 0.2\,V}$

Since, $(V_G)_{M1} = 0.9\,V$ and $V_{GS} - V_{Th,N} = 0.1$ for M1

$\rightarrow V_S = 0.9 - 0.37 - 0.1$

$\rightarrow V_S = 0.43\,V$

Since, $V_S > 0.2 \rightarrow$ "M0 remains in saturation"

for M1 to remain in saturation,

$V_{D1} > (V_{GS})_{M1} - V_{Th,n}$

$\rightarrow V_{D1} > 0.1\,V$

For an overdrive of 0.4V for M3 we get that,

$V_{sg3} - |V_{Th,p}| = 0.4\,V$

$\rightarrow 1.8 - V_{g3} - 0.39 = 0.4$

$\rightarrow V_{g3} = V_{D1} = \underbrace{1.01V > 0.1\,V}$

Hence, M~~3~~1 remains in saturation,

By principle of argument, we show that,

$$\boxed{V_{D1} = V_{mid}}$$

This results in identical calculations for M2, which also remains in saturation.

For M3 to remain in saturation,

$$(V_{SD})_3 > (V_{SG})_3 - |V_{Th,p}|$$

$$\rightarrow 1.8 - 1.01 > 1.8 - 1.01 - 0.39$$

i.e M3 remains in saturation as long as $(V_{SG})_3 > |V_{Th,p}|$

$$\rightarrow 1.8 - 1.01 > 0.39$$

$$\rightarrow 0.79 > 0.39$$

- Hence M3 also remains in saturation

Since, $V_{G3} = V_{D3} = V_{D1} = V_{mid}$,

Similar argument holds for M4, which remains in saturation.

$V_{..} > V_{GS} - V_{Th,n}$

- Now that the calculations for the first-stage have been completed, we can simulate the circuit on LTSpice.

The gain-expected from the first-stage from theoretical calculations $= g_{m1} (r_{ON2} \parallel r_{OP4})$

$$g_{m1} = \frac{2(I_D)_{M1}}{(V_{gs} - V_{Th,N})_{M1}} = \frac{2 \times 80uA}{0.1}$$

$\Rightarrow$ $g_{m1} = 1.6 \times 10^{-3}$

Taking g_{m1} from the LOG Files,
$(g_{m1}) = 1.33 \times 10^{-3}$

Taking value of $(G_{DS})_2$ and $(G_{DS})_4$ from the simulated LOG File on LTspice, we get that,

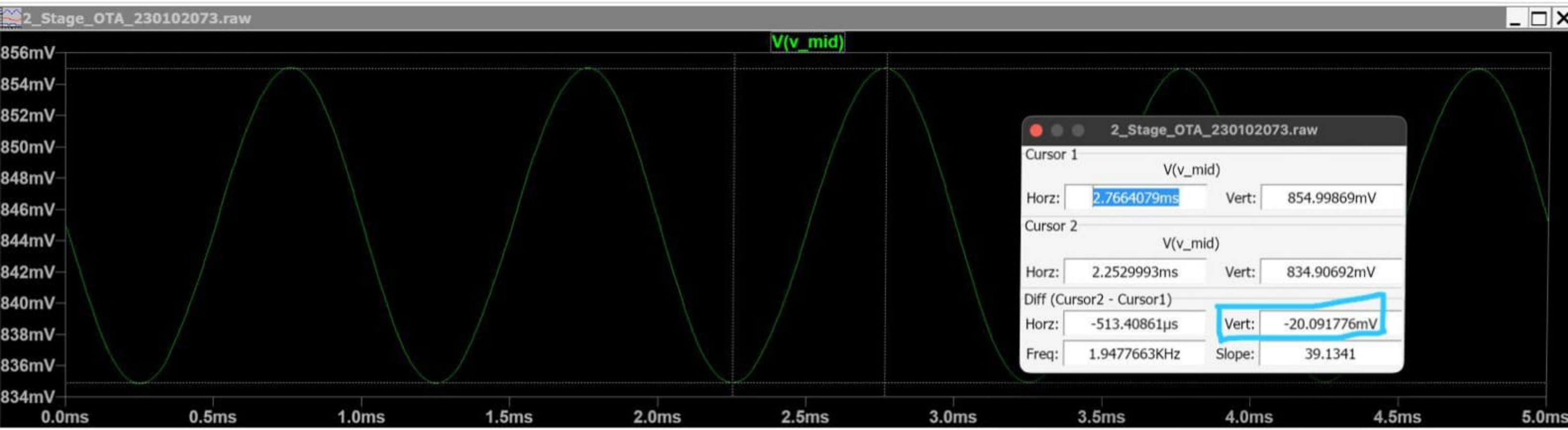
$$r_{ON2} = \frac{1}{\cancel{3.49}\ 9.53 \times 10^{-6}} = 1.04931 \times 10^5$$

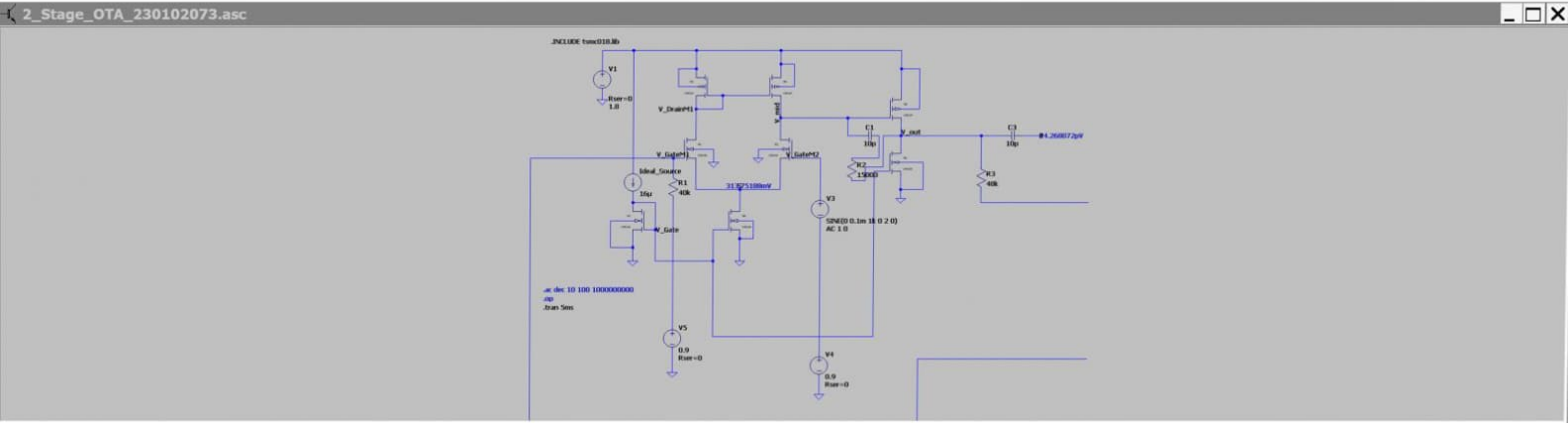
$$r_{OP4} = \frac{1}{3.49 \times 10^{-6}} = 2.86532 \times 10^5$$

$\Rightarrow$ $r_{ON2} \parallel r_{OP4} = 76805.258\ \Omega$

So $A_{1st\ stage} = g_{m1} \times (r_{ON2} \parallel r_{OP4})$

$A_{1st\ stage} = 102.15$


2_Stage_OTA_230102073.raw
V(v_mid)
856mV
854mV
852mV
850mV
848mV
846mV
844mV
842mV
840mV
838mV
836mV
834mV
0.0ms
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
5.0ms
2_Stage_OTA_230102073.raw
Cursor 1
V(v_mid)
Horz: 2.7664079ms
Vert: 854.99869mV
Cursor 2
V(v_mid)
Horz: 2.2529993ms
Vert: 834.90692mV
Diff (Cursor2 - Cursor1)
Horz: -513.40861µs
Vert: -20.091776mV
Freq: 1.9477663KHz
Slope: 39.1341


2_Stage_OTA_230102073.asc
.INCLUDE tsmc018.lib
V1
V_DrainM1
V_GateM1
V_GateM2
Ideal_Source
R1
40k
C1
10p
V_out
C3
10p
R2
R3
40k
V3
SINE(0 0.1m 1k 0 2 0)
AC 1 0
V_Gate
.ac dec 10 100 1000000000
.op
.tran 5ms
V5
0.9
Rser=0
V4
0.9
Rser=0

Running Simulation on LTSpice,

$$\boxed{A_{v,\,1^{st}\,stage} = 100.45}$$

Attached is the respective plots,

$$\text{Percentage error } (\%) = \frac{100.45 - 102.15}{102.15} \times 100\%$$

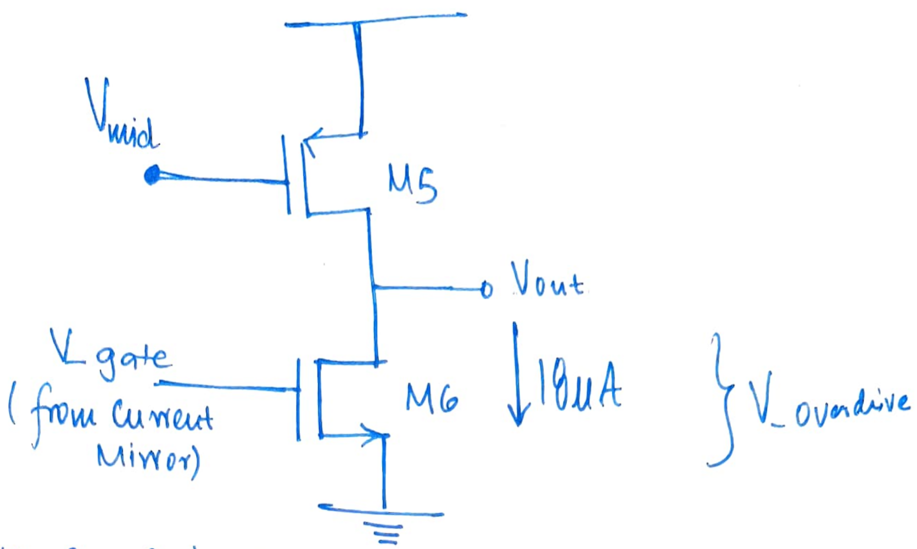
$$= -1.664\%$$

This error is due to several practical difficulties associated with this design. Some are enlisted below,

1) The Current mirror configuration has a finite r_o and hence does not mirror the current perfectly. Practically a smaller value of current is mirrored into the tail of the differential pair compared to our theoretical expectations which can lead to lower gain.

2) The threshold-voltage of M_1 and M_2 are affected by Body-effect since their source and substrate are not at the same-potential.

The 2nd Stage of the OTA is a Common Source Amplifier,



- To achieve a gain via the second stage, I must choose a value of $I_D = 18uA$

- By current Mirror,

$$\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_7} = \frac{18uA}{16uA}$$

$$\Rightarrow \left(\frac{W}{L}\right)_6 = 4 = \frac{3600n}{900n}$$

for M6 to remain in saturation,

$$V_{out,DC} > V\_gate - V_{TH,N}$$

$$\Rightarrow V_{out,DC} > 0.57 - 0.37 \text{ V}$$

$$\Rightarrow V_{OUT,DC} > 0.2 \text{ V}$$

Similarly for transistor M5,

$$(I_D)_{M5} = 18uA$$

Assuming an overdrive of 0.4V for M5,

$$I_D = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_5 (V_{gs} - V_{THp})^2$$

$$\Rightarrow \left(\frac{W}{L}\right)_5 = \frac{2 \times 18}{100 \times 0.16} \simeq 2.222..$$

$$\Rightarrow \left(\frac{W}{L}\right)_5 = \frac{2000n}{900n}$$ {For practical reason I have taken, $\frac{2150n}{900n}$}

Since, we have calculated all W/L values required for our system, let's check if M5 and M6 also remain in saturation.

For M5, $V_{SD5} > V_{sg5} - |V_{TH,p}|$

$$\Rightarrow 1.8 - V_{out} > 1.8 - \cancel{V_{mid}}^{1.01} - 0.39$$

$$\Rightarrow V_{out} < 1.4V$$ for M5 to remain in saturation

and, $V_{out} > 0.2V$ for M6 to remain in saturation.

From LTSpice Simulations, $V_{out} = 0.33V$

so hence, both M5 and M6 also remain in saturation.

Now the 2nd stage gain can be calculated as,

$$A_{v_{2nd\,stage}} = g_{m5}\left(r_{op5} \parallel r_{on6}\right)$$

Taking values from LOG file on LTSpice after running .op simulation yields us that,

$g_{m5} = \cancel{5.89}\ 6.21 \times 10^{-5}$; $r_{ON6} = \frac{1}{G_{ds6}} = \cancel{3.5...}\ 7.93650 \times 10^{5}$; $r_{OP5} = \frac{1}{G_{ds5}} = \cancel{1.69...}\ 1.14164 \times 10^{6}$

$$A_{v,2nd\,stage} = g_{m5}\left(r_{ON6} \parallel r_{OP5}\right)$$

$$\Rightarrow A_{v,2nd\,stage} = 6.21 \times 10^{-5} \times 4.68603 \times 10^{5}$$

$$\Rightarrow \boxed{A_{v,2nd\,stage} = \cancel{17.477}\ 29.10025}$$

Expected Theoretically.

Comparing against the simulated values,

$$\boxed{A_{v,2nd\,stage} = 28}$$

From LTSpice Simulation

Percentage % error in $A_{v,2nd\,stage} = \frac{28 - 29.10025}{29.10025} \times 100\%$

$= -3.78\ \%$

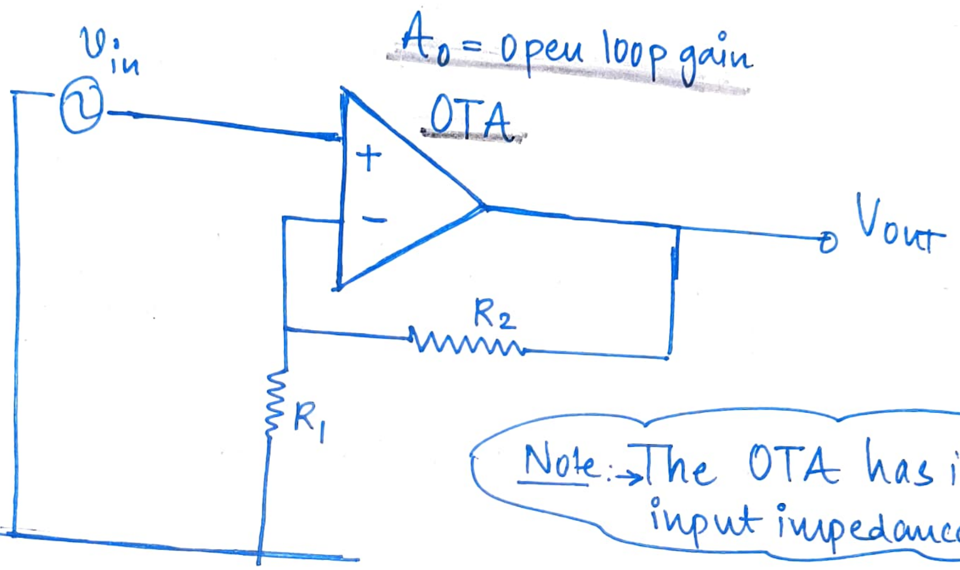
$$\text{Total Open-Loop Gain} = A_{v_{1^{st}\,stage}} \times A_{v_{2^{nd}\,stage}}$$

$$\Rightarrow A_0 = 28 \times 100.45$$

$$\rightarrow \boxed{A_0 = 2812.6}$$

FEEDBACK CONNECTION

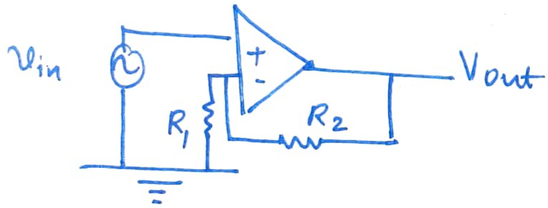
Now, connecting the OTA in non-inverting feedback configuration,



Note: → The OTA has infinite input impedance

for finite open loop gain, $V_{OUT} = A_0 (V_+ - V_-)$

in small-signal-configuration, the circuit looks like the following,



$$V_+ = v_{in}$$

$$v_- = \frac{V_{out} R_1}{R_1 + R_2}$$

So, $A_0\left(v_{in} - \frac{v_{out} R_1}{R_1+R_2}\right) = v_{out}$

$$\Rightarrow \quad A_0 v_{in} = \left(\frac{A_0 R_1 + 1}{R_1+R_2}\right) v_{out}$$

$$\Rightarrow \quad \frac{v_{out}}{v_{in}} = \frac{A_0}{1 + \frac{A_0 R_1}{R_1+R_2}} = \frac{A_0(R_1+R_2)}{R_1+R_2+A_0 R_1}$$

$$\rightarrow \quad \frac{v_{out}}{v_{in}} = \left(1+\frac{R_2}{R_1}\right) \frac{A_0(R_1+R_2)}{(1+A_0)R_1+R_2} \quad \frac{R_1}{(R_1+R_2)}$$

$$\Rightarrow \quad \frac{v_{out}}{v_{in}} = \left(1+\frac{R_2}{R_1}\right)\left\{\frac{R_1}{\left(1+\frac{1}{A_0}\right)R_1 + \frac{R_2}{A_0}}\right\}$$

non-ideality term

$$\rightarrow \quad \frac{v_{out}}{v_{in}} = \left(1+\frac{R_2}{R_1}\right) \frac{1}{\left(1+\frac{1}{A_0}\right) + \frac{1}{A_0}\frac{R_2}{R_1}}$$

for large-enough forward loop gain (A_0); $\frac{v_{out}}{v_{in}} \approx 1 + \frac{R_2}{R_1}$

To get a closed loop feedback gain of 2; sufficient to choose $R_2 \cong R_1$. However due to the non-ideality term $\frac{1}{\left(1+\frac{1}{A_0}\right)+\frac{1}{A_0}\frac{R_2}{R_1}}$; R_2 must be slightly larger than R_1 to compensate for the drop caused by that term.

From practical iterations / solving the equation we choose,

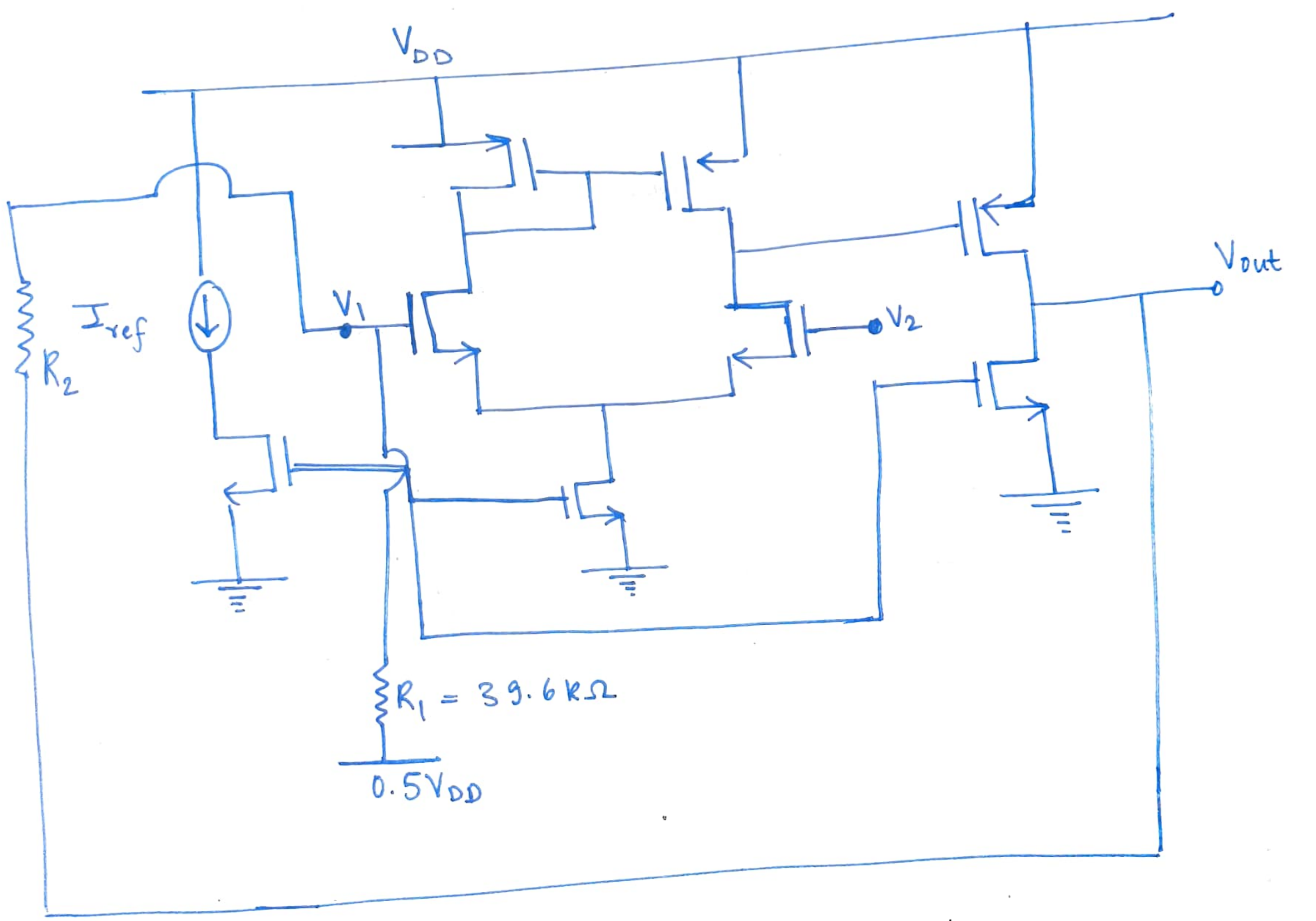
$$\frac{R_2}{R_1} = 1.001429593$$

But for practical-reasons, we find,

$R_2 = 43.053 k\Omega$ and $R_1 = 39.6 k\Omega$

are suitable values, for getting a closed loop gain of 2.

CLOSED Loop Feedback Connection

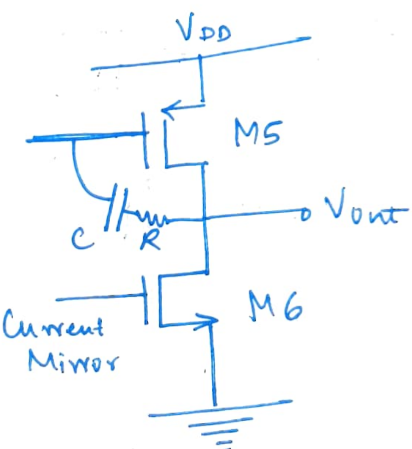


Now we must adjust the values of C_c and R_Z according to the desired phase-margin (P.M) and bandwidth of the circuit.

around 60°

I initially placed only a capacitor $C = 3pF$ between the gate and the drain of the transistor M5 of the Common-Source-amplifier. However even though this helps in seperating the two poles of the common-Source-amplifier, I observed a R.H.P zero (of the Common Source Amplifier) which degrades the phase-margin and causes the gain to abruptly shoot up.

The location of this zero for the common-Source amplifier compensated in the shown manner is $Z = \dfrac{-g_{m5}}{C(g_{m5}R-1)}$



We choose R very close to the value of $1/g_{m5}$ for the zero to shift to either $+\infty$ or $-\infty$ and removing its effect on the Bode-plot for reasonable-frequencies.

From Log-Files, $g_{m5} = 6.21 \times 10^{-5}$
(g_{m5} was determined)

So I choose $R = \frac{1}{g_{m5}} = 16{,}103.059\,\Omega$

$\Rightarrow R \simeq 16\,k\Omega$ as a starting point.

I initially started with $C = 3\,pF$ and $R = 16\,k\Omega$. However I was not able to obtain a desired-phase-margin around 60°.

#By carefully changing the values of C and R for obtaining the desired characteristics (Large Bandwidth and Phase-Margin = 60°)

$$\boxed{C = 10\,pF \text{ and } R = 15.875\,k\Omega}$$

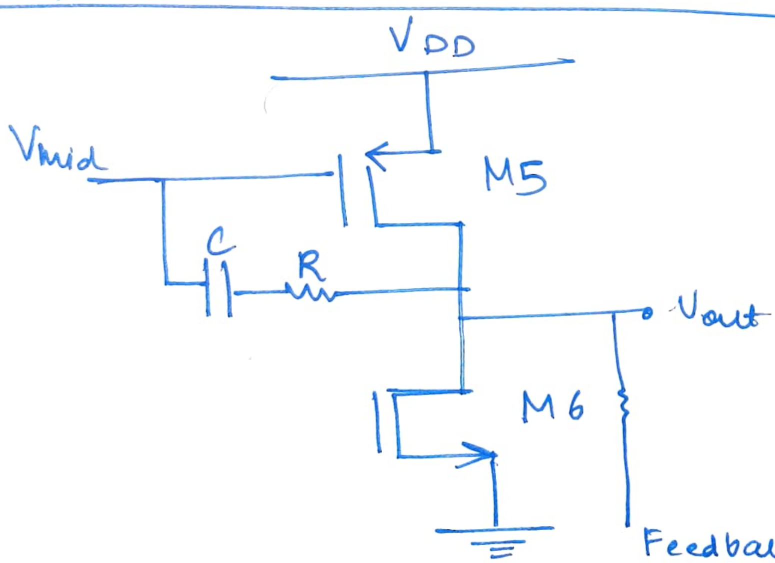


Fig. 2nd Stage of OTA with Miller Compensation.