CO200 - Computer Organization and Architecture

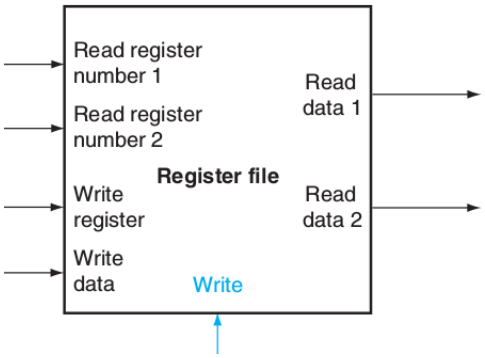
A2 - ALU and Register File Design in SystemC or Verilog

Points to Note

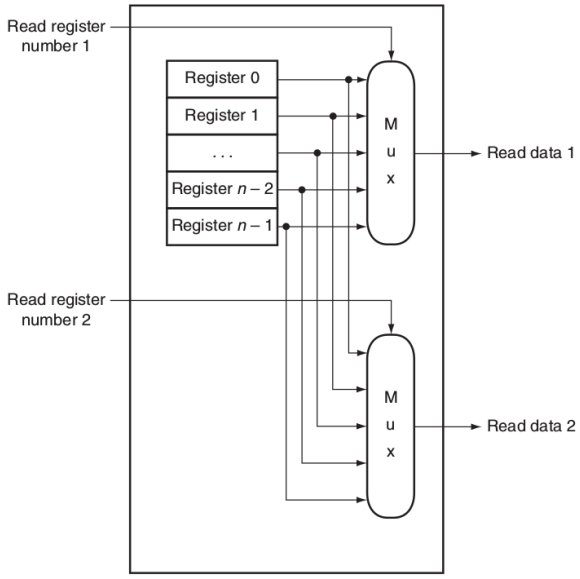
- Design and test each of the listed hardware modules in the SystemC or Verilog.
- In the comments section of the code, include a short description of the program, your name, roll number, date of writing the program and other information you deem relevant.
- (a) Report: Every question can have a corresponding answer containing block diagrams/ microarchitecture, brief explanation, other relevant info. (b) Auxilary files to submit: Per question, include the following files along with the report: Code, the testbench including the monitor and stimulus, execution screenshots, VCD dump, gtkwave screenshots. (c) Archive: Organize your submission into directories per question.
- This is a team assignment. One submission per team.
- (a) Submission is due Oct. 31, midnight. Pack your report, code, screenshots and other files in an archive and mail to `co200.nitk@gmail.com`.

Modules

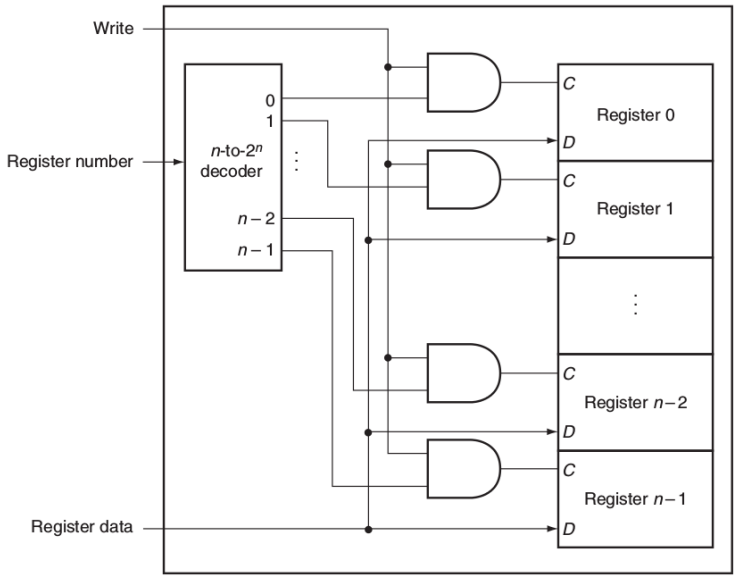
1. **1-bit ALU**. Build a 1-bit ALU that can perform the following logical and arithmetic operations: AND, OR, NAND, NOR, ADD, SUBTRACT. Include two additional flags: (a) a flag to indicate if the result of the ALU operation is zero (Z), (b) a flag to indicate if the first input is greater than the second input. *Hint:* Reference implementation is described in Appendix B.5 in *Patterson and Hennesy, Computer Organization and Design, 5e, MK*.
2. **Register File**. Use the register designed above to implement a 32 register Register file with two read ports and one write port (Fig. shown below is the Figure B.8.7 from PH-COD-5e). The block diagrams of the two read ports and the write port are shown separately (Figures B.8.8 and B.8.9).



3 Port Register File



(a) Register File with two read ports.



(b) Write port implementation in the Register File.

Hint: For the block diagrams and design of the Register File refer Section B.8 of *Patterson and Hennesy, Computer Organization and Design, 5e, MK*.