Vineet Panchbhaiyye

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Education

- **Santa Clara University** — Santa Clara, USA
  MS in Electrical Engineering; GPA 4.0 — *April 2018 - April 2020*
- **Indian Institute of Technology, Madras** — Chennai, India
  Bachelor of Technology in Electrical Engineering — *July 2002 – July 2006*

Academics

- **Relevant Coursework**: Robotics, Computer Vision, Computer Architecture, Advanced Computer Architecture, Digital Signal Processing, Design and Analysis of Algorithms
- **Teaching Assistant**: Logic Design & Advanced Logic Design(Fall '18), Logic Design & Electric Circuits(Winter '19).
- **IEEE Global Humanitarian Technology Conference 2018**: Presented a poster paper on "Experimental results on using deep learning to identify agricultural pests" at IEEE GHTC 2018.

Projects

- **Efficient Deep Neural Network Architectures (In progress Winter '19)**: An ongoing project on implementing efficient deep neural network architectures under the guidance of Dr. Tokunbo Ogunfunmi.
- **A Study on Effect of Dataset size on CNN Accuracy**: Implemented VGG16, ResNet and GoogleNet(Inception) from scratch in Python using Keras. Trained these CNNs on CIFAR10, CIFAR100 and a small custom dataset to understand the effect of dataset size on accuracy.
- **Performance Analysis of Branch Prediction Algorithms**: Simulated and analyzed the performance of 2-bit predictor, gshare, correlating predictor and the tournament predictor branch prediction algorithms on SPEC benchmarks.

Certification

- **Deep Learning specialization**: Specialization by deeplearning.ai on Coursera. Completed the Neural Networks and Deep Learning, Improving Deep Neural Networks: Hyperparameter tuning, Regularization and Optimization courses.
- **Machine Learning specialization**: Specialization by University of Washington on Coursera. Completed the Foundation, Regression and Classification courses.

Experience

- **Qualcomm** — Bangalore, India
  Senior Lead Engineer — *Jan 2016 - Mar 2018*
  - **Network On Chip (NOC) interconnect verification**: Led a team of 3 Design Verification engineers to verify the NOC interconnects for Camera, Display, Video and Audio modules in Snapdragon System on Chips(SoCs). Responsible for planning and executing test plan to achieve verification goals.
- **WWStay Services** — Bangalore, India
  Senior Engineer — *Feb 2014 - Aug 2015*
  - **Extended Stay App**: Designed and implemented a App from scratch with 3 developers. The app connected travellers to 5000+ serviced apartments worldwide. This app was demonstrated to more than 100 potential clients at Global Business Travel Association (GBTA) convention 2015, Orlando, Florida.
- **Qualcomm** — Bangalore, India
  Senior Engineer — *Mar 2013 - Feb 2014*
  - **Video stream parser (VSP) verification**: VSP decodes and encodes the headers for the various video formats supported. Upgraded the OVM verification environment for changes in the CABAC/CAVLC functionality.
- **Mirafra Technologies** — Bangalore, India
  Consultant at Qualcomm India — *June 2010 - Feb 2013*
  - **Video Codec verification**: Verified the integration of multi-format video codec module and pixel cache in 3 versions of Snapdragon processor which were part of Google Nexus 4 and Nexus 5.

- **JPEG Decoder & Video Pre-processing Engine (VPE) verification**: Verified the JPEG-D and VPE modules with 100% functional and code coverage. Provided support for Gate-Level Simulation and Post Silicon validation setup.

- **Samsung Electronics** Bangalore, India/Gihueng, South Korea
  Senior Software Engineer *July 2006 - June 2010*
  - **H.264 Encoder & DMA controller verification**: Verified DMA controller and H.264 Encoder critical for the multimedia functionality in processors powering iPhone 3G and iPod. Got Business Contribution Award for above projects. This project was executed from Bangalore and Giheung, South Korea.

Programming Skills

- **Languages**: Python, Verilog, SystemVerilog, Matlab, C++(beginner)
- **Frameworks**: Django, Keras, Tensorflow(Beginner), UVM